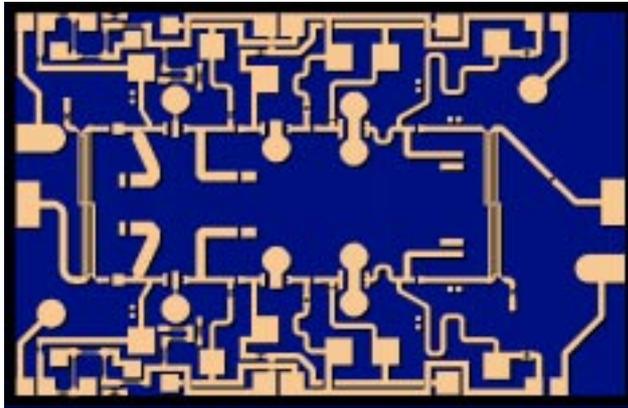


30-38 GHz Balanced Low Noise Amplifier

TGA4511-EPU

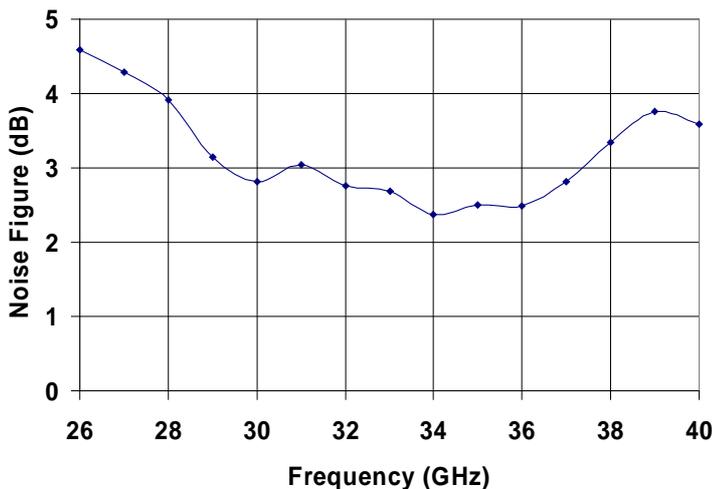


Key Features

- 0.15 um pHEMT Technology
- 15 dBm Nominal Pout @ 35 GHz
- 17 dB Nominal Gain @ 35 GHz
- 2.5 dB Noise Figure @ 35 GHz
- Bias Conditions: 3.5V, 110 mA
- Chip Dimensions: 2.7mm x 1.8mm

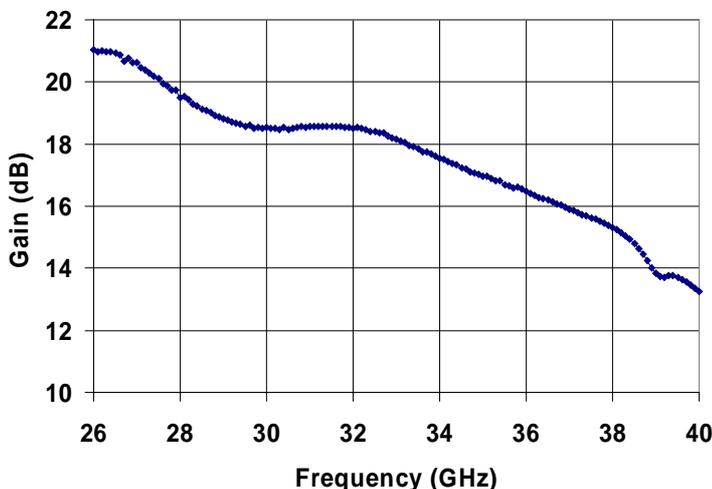
Preliminary Measured Data

Bias Conditions: Vd = 3.5 V, Id = 110 mA



Primary Applications

- Point-to-Point Radio
- Point-to-Multipoint Radio



Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice

TABLE I
MAXIMUM RATINGS 5/

SYMBOL	PARAMETER	VALUE	NOTES
V ⁺	Positive Supply Voltage	6 V	4/
V ⁻	Negative Supply Voltage Range	-2 to 0 V	
I ⁺	Positive Supply Current (Quiescent)	400 mA	4/
I _G	Gate Supply Current	40 mA	
P _{IN}	Input Continuous Wave Power	TBD	
P _D	Power Dissipation	TBD	3/ 4/
T _{CH}	Operating Channel Temperature	150 °C	1/ 2/
T _M	Mounting Temperature (30 Seconds)	320 °C	
T _{STG}	Storage Temperature	-65 to 150 °C	

- 1/ These ratings apply to each individual FET.
- 2/ Junction operating temperature will directly affect the device median time to failure (T_M). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.
- 3/ When operated at this bias condition with a base plate temperature of TBD, the median life is reduced from TBD to TBD.
- 4/ Combinations of supply voltage, supply current, input power, and output power shall not exceed P_D.
- 5/ These ratings represent the maximum operable values for this device.

TABLE II
ELECTRICAL CHARACTERISTICS

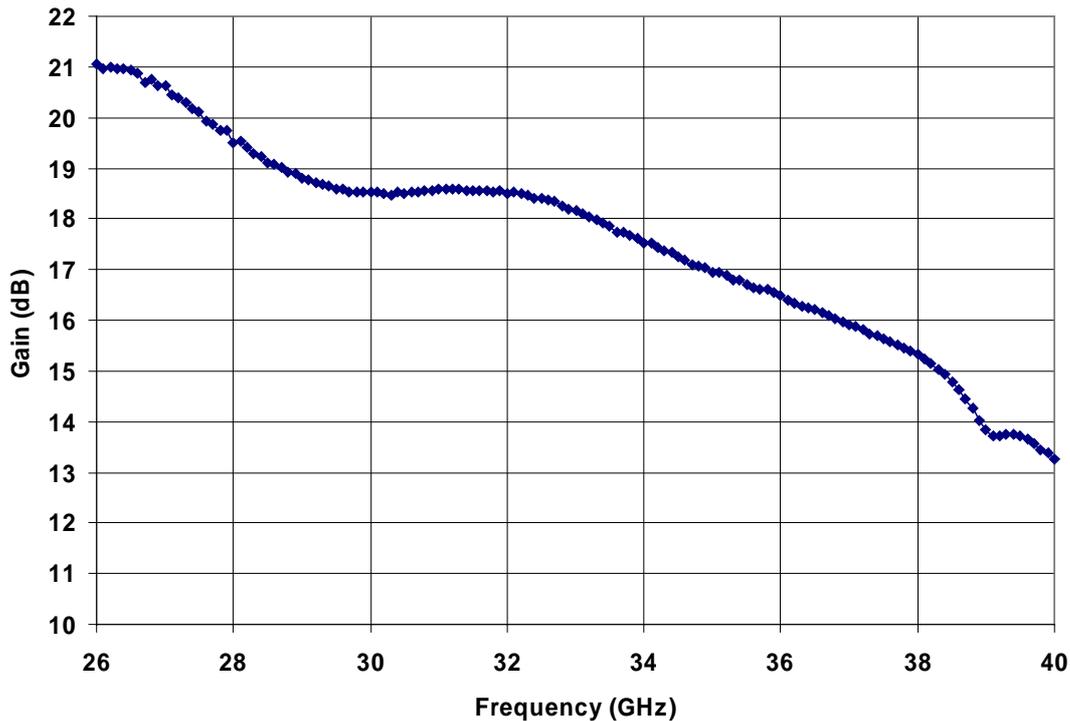
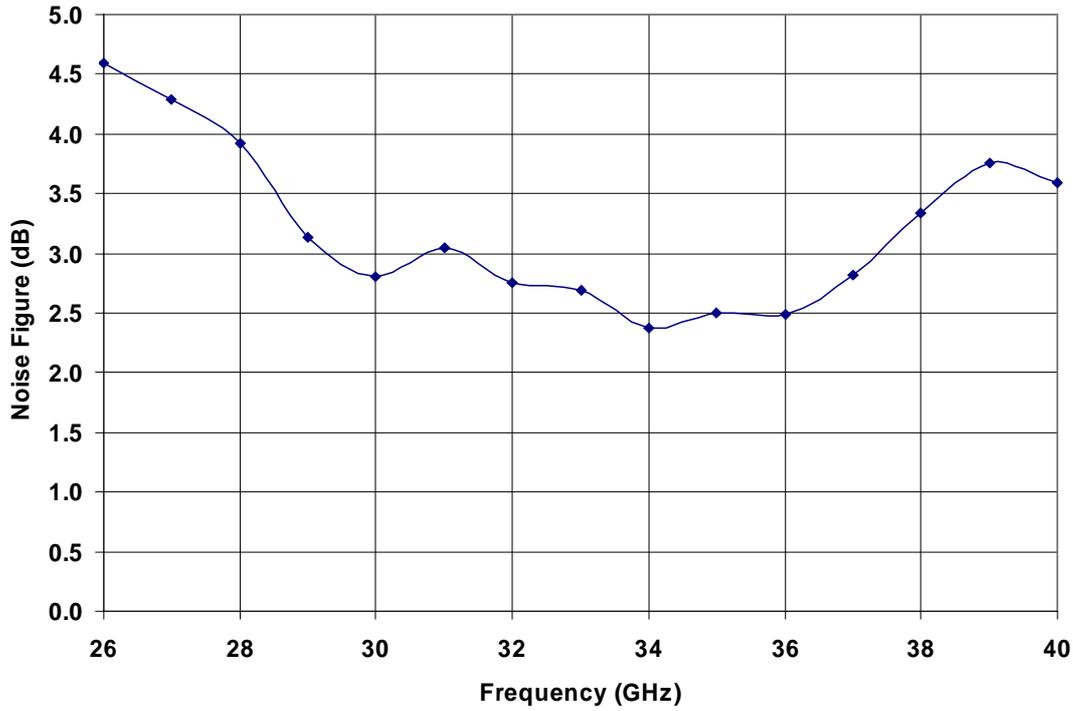
(T_a = 25°C ± 5°C)

PARAMETER	TYPICAL	UNITS
Drain Operating	3.5	V
Quiescent Current	110	mA
Small Signal Gain	17	dB
Input Return Loss (Linear Small Signal)	18	dB
Output Return Loss (Linear Small Signal)	18	dB
Output Power @ 1 dB Compression Gain	15	dBm
Third Order Intercept Point @ -12 dBm @ 35GHz	25	dBm

Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice

Preliminary Measured Data

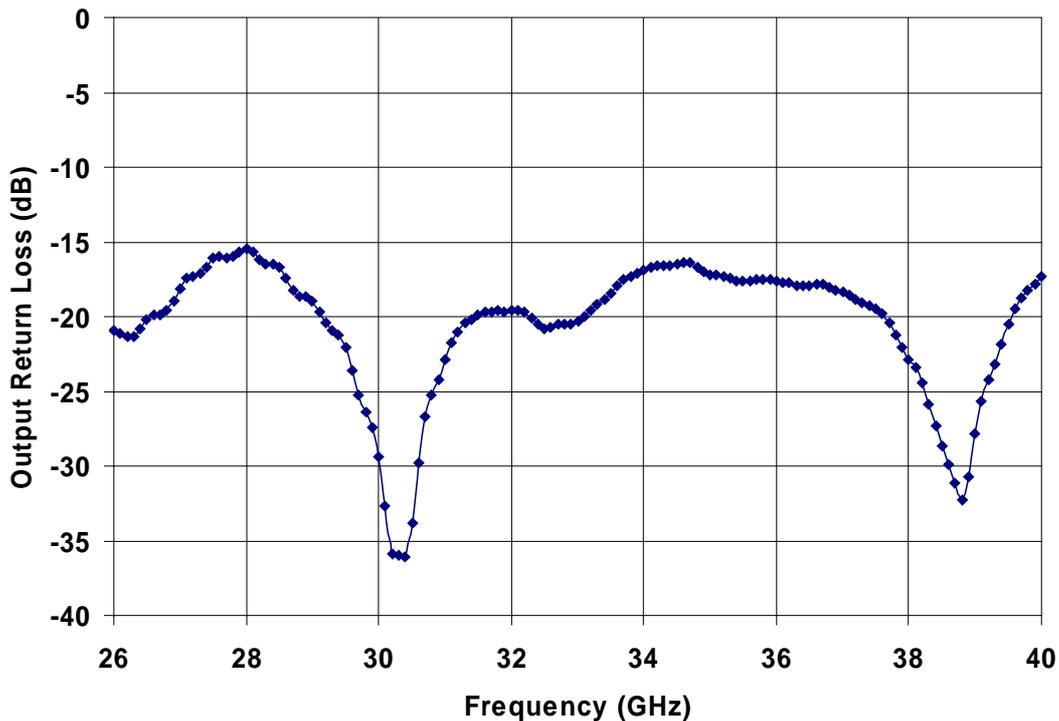
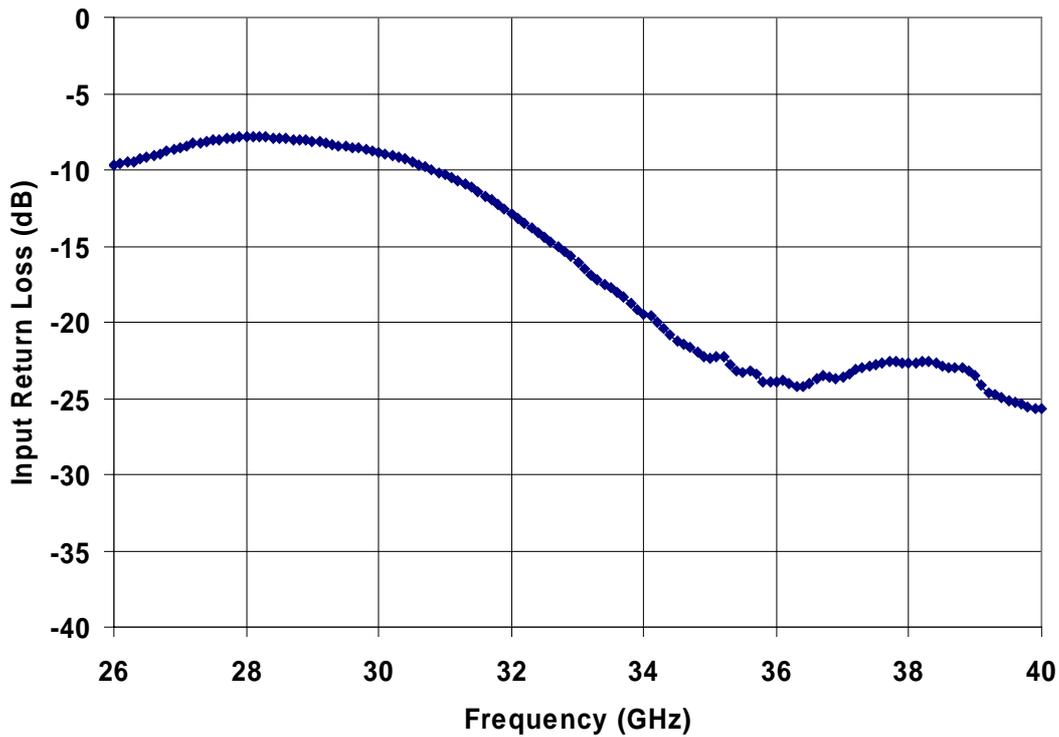
Bias Conditions: $V_d = 3.5\text{ V}$, $I_d = 110\text{ mA}$



Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice

Preliminary Measured Data

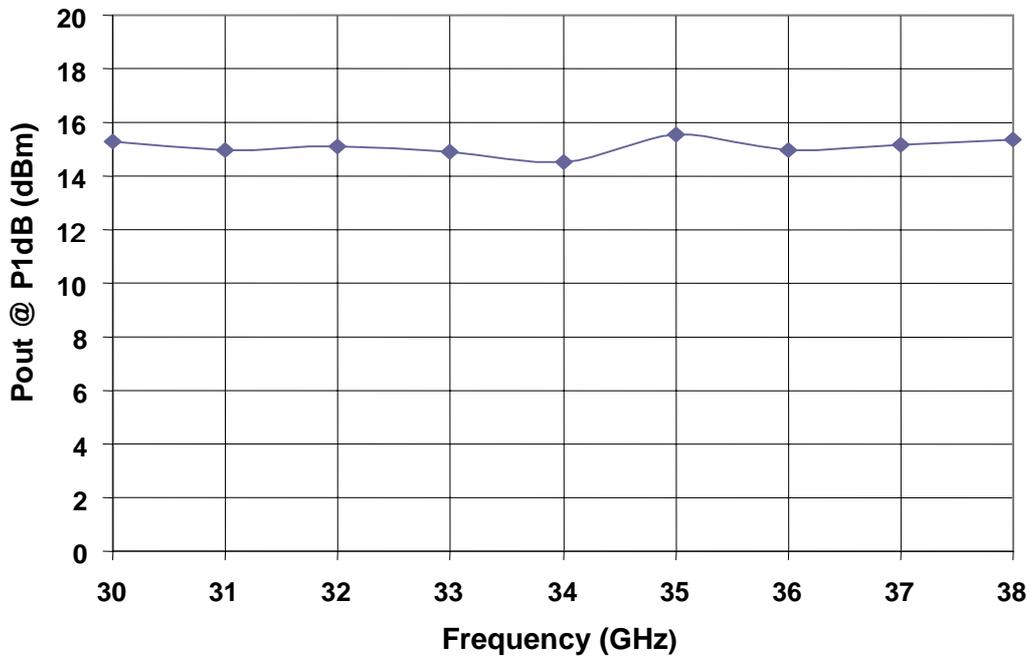
Bias Conditions: $V_d = 3.5\text{ V}$, $I_d = 110\text{ mA}$



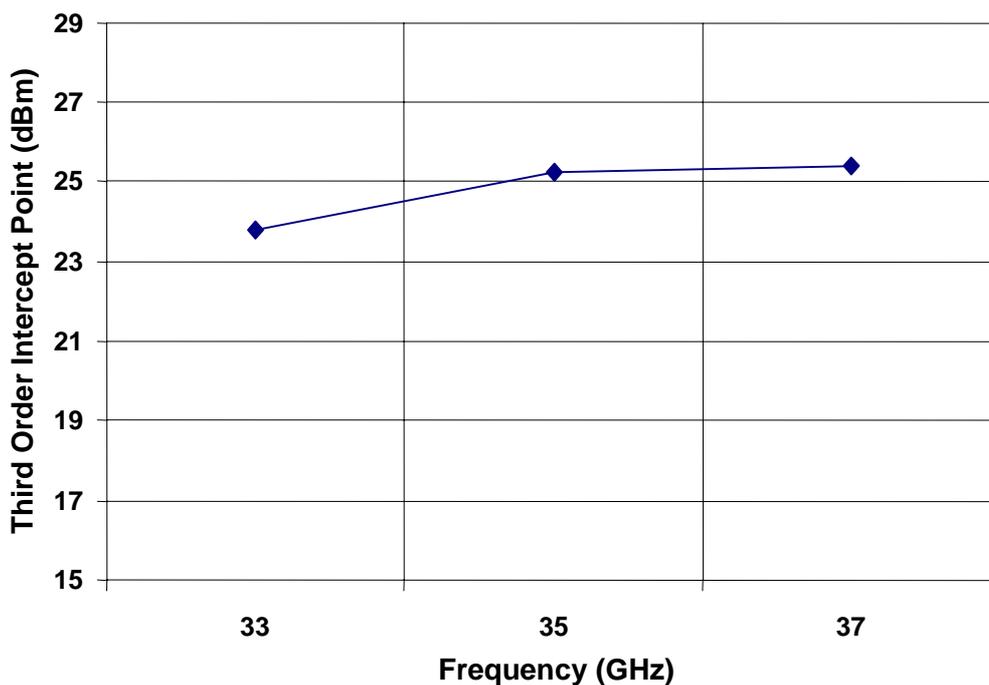
Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice

Preliminary Measured Data

Bias Conditions: $V_d = 3.5\text{ V}$, $I_d = 110\text{ mA}$

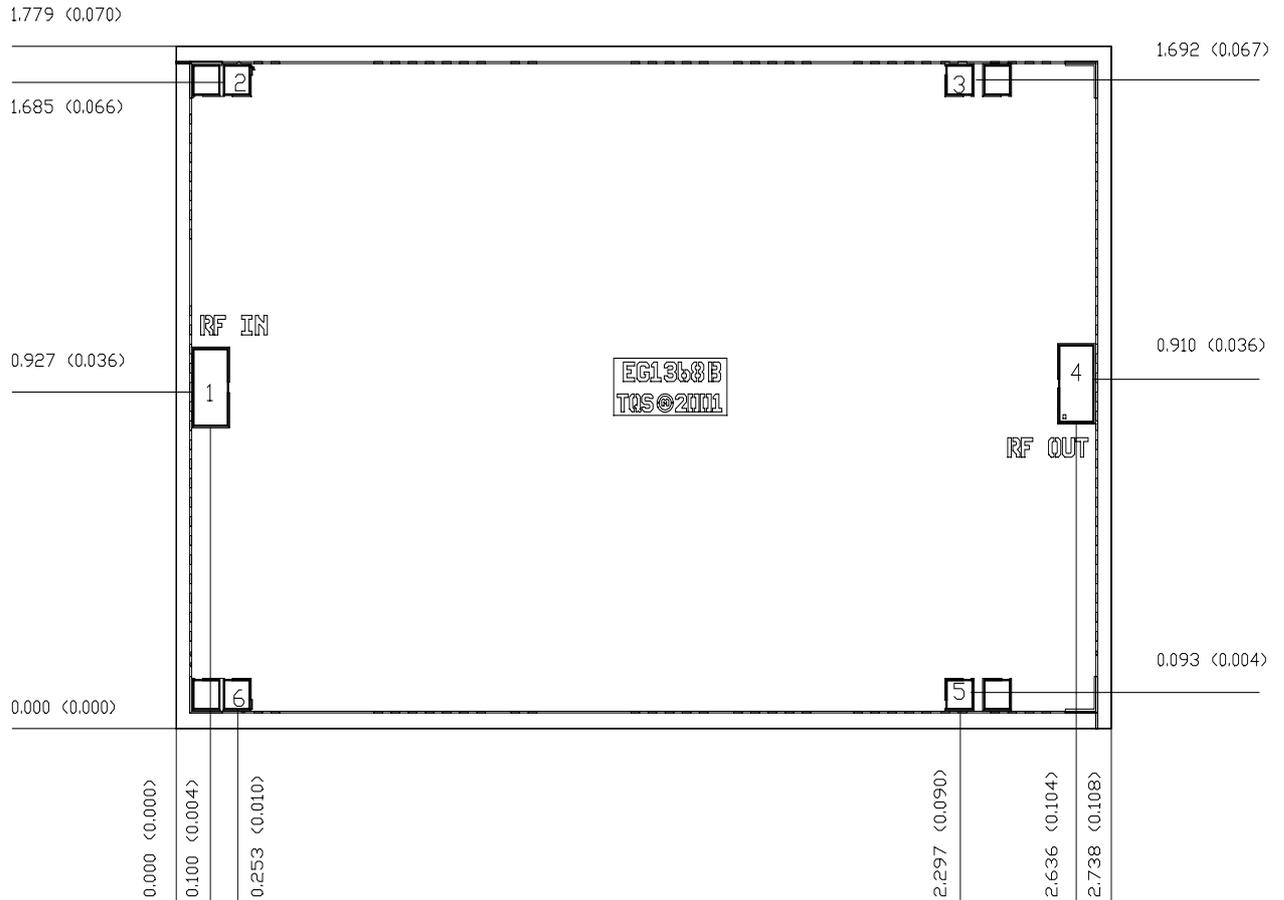


**TOI at -12 dBm Input Power
(P1dB - 10 dB)**



Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice

Mechanical Drawing



Units: millimeters (inches)

Thickness: 0.1016 (0.004)

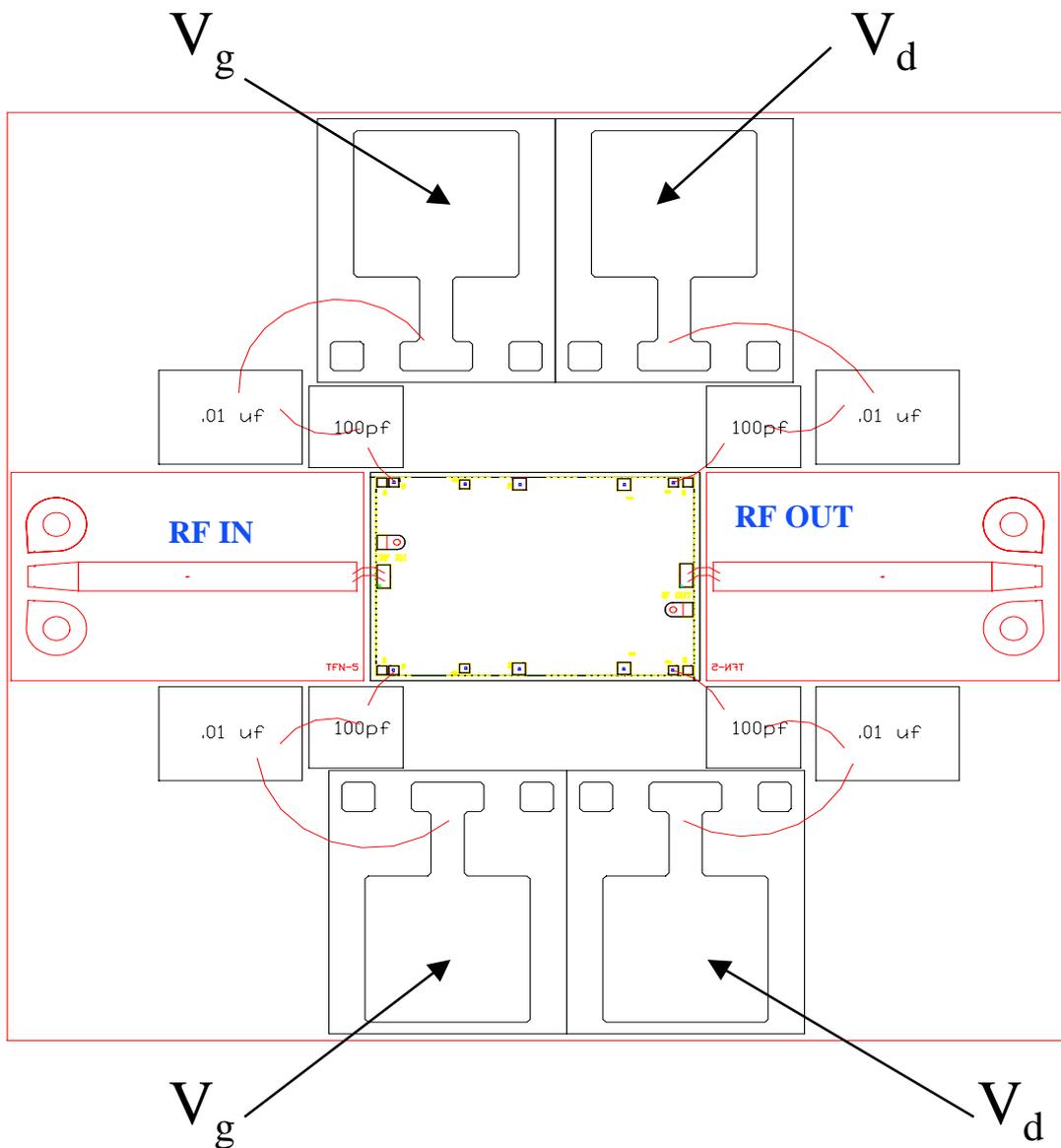
Chip edge to bond pad dimensions are shown to center of bond pad

Chip size tolerance: +/- 0.051 (0.002)

Bond pad #1	(RF In)	0.100 x 0.200 (0.004 x 0.008)
Bond pad #2	(Vg)	0.085 x 0.085 (0.003 x 0.003)
Bond pad #3	(Vd)	0.085 x 0.085 (0.003 x 0.003)
Bond pad #4	(RF Out)	0.100 x 0.200 (0.004 x 0.008)
Bond pad #5	(Vd)	0.085 x 0.085 (0.003 x 0.003)
Bond pad #6	(Vg)	0.085 x 0.085 (0.003 x 0.003)

Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice

Chip Assembly Diagram



GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

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Assembly Process Notes

Reflow process assembly notes:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300°C.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- No fluxes should be utilized.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.
- Microwave or radiant curing should not be used because of differential heating.
- Coefficient of thermal expansion matching is critical.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Discrete FET devices with small pad sizes should be bonded with 0.0007-inch wire.
- Maximum stage temperature is 200°C.

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