PAM8902

30-Vpp Mono Class-D Audio Amplifier for Piezo/Ceramic Speakers

Key Features

- Supply Voltage Range From 2.5 V to 5.5 V
- 30 Vpp Output Load Voltage From a 2.5 V Supply
- Integrated Boost Converter Generates 17.5V Supply
- Programmable softstart
- Small Boost Converter Inductor
- Selectable Gain of 18 dB, 22 dB, and 26 dB
- Selectable Boost output voltage of 8V, 12V, and 17.5V
- Low Shutdown Current: <1uA
- Build in Thermal , OCP ,OVP,Short protection
- Available in Space Saving Packages:
  16-ball 1.95mmx1.95mm CSP package
  16-pin QFN4x4 package

Applications

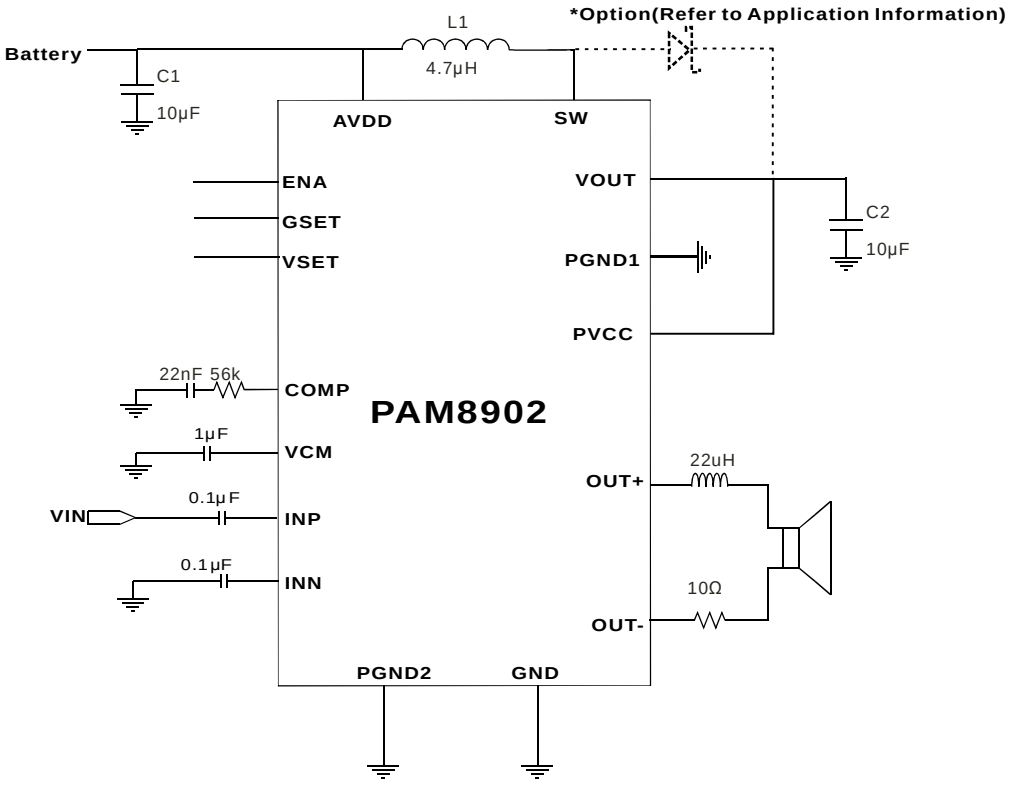
- Wireless or Cellular Handsets
- Por t able DVD Player
- Personal Digital Assistants (PDAs)
- Electronic Dictionaries
- Digital Still Cameras

General Description

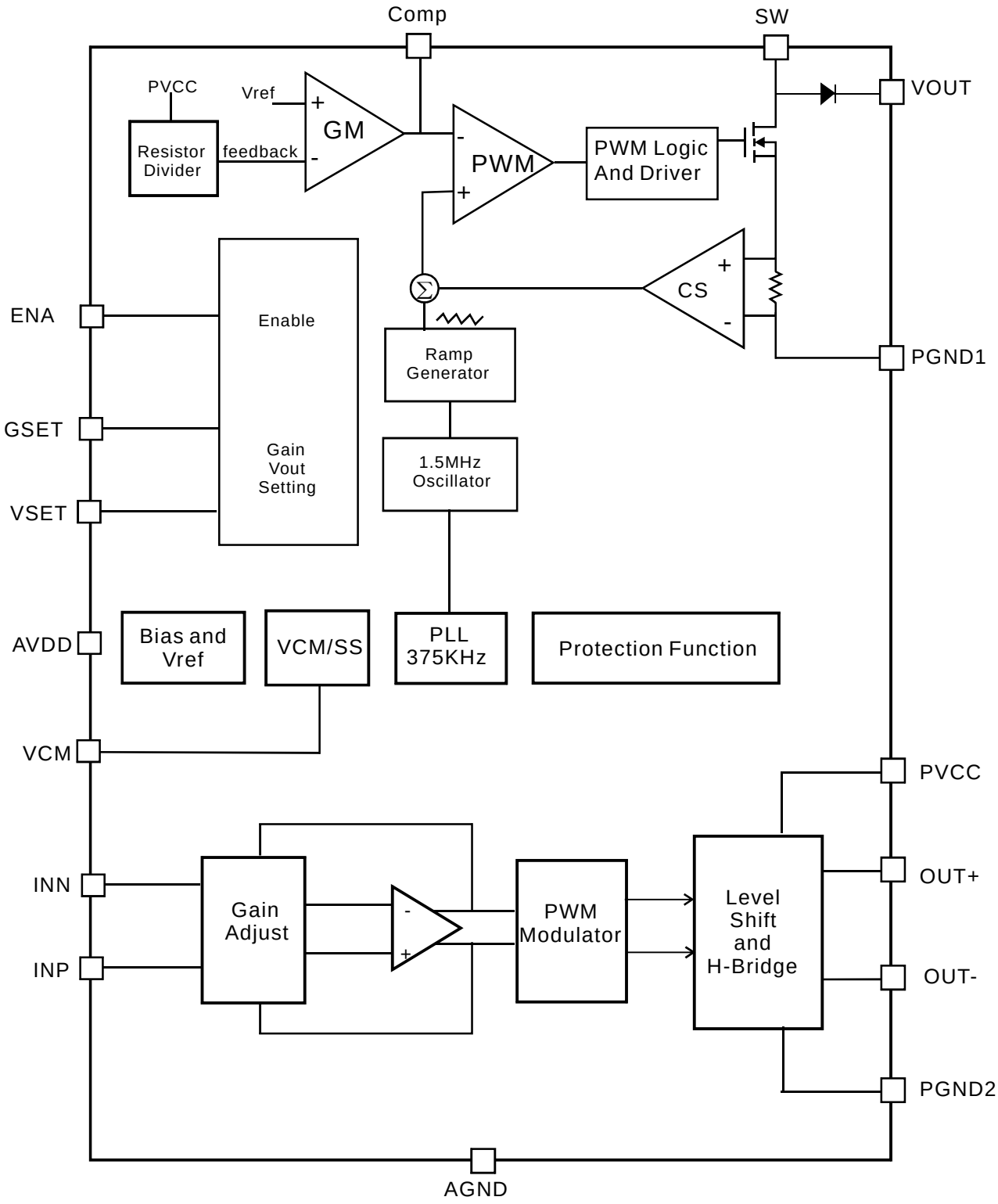
The PAM8902 is a mono, Class-D audio amplifier with integrated boost convertor designed for piezo and ceramic speakers.The PAM8902 is capable of driving a ceramic/piezo speaker with 30Vpp(10.6Vrms) from a 3.6V power supply.The PAM8902's Boost converter operates at a fixed frequency of 1.5MHz , and provides a 17.5V supply with a minimum number of external components. PAM8902 features an integrated audio low pass filter that rejects high frequency noise thus improving audio fidelity. And three gain modes of 18dB, 22dB and 26dB easy for using.PAM8902 also provides thermal ,short, under and over voltage protection.

The PAM8902 is available in a 16-ball 1.95mmx1.95mm CSP package and 16-pin QFN4x4 package.

Typical Application Circuit

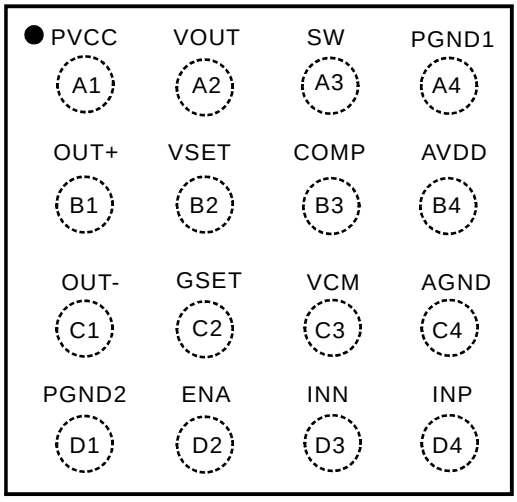


Block Diagram



Pin Configuration & Marking Information

16 Ball CSP
Top View

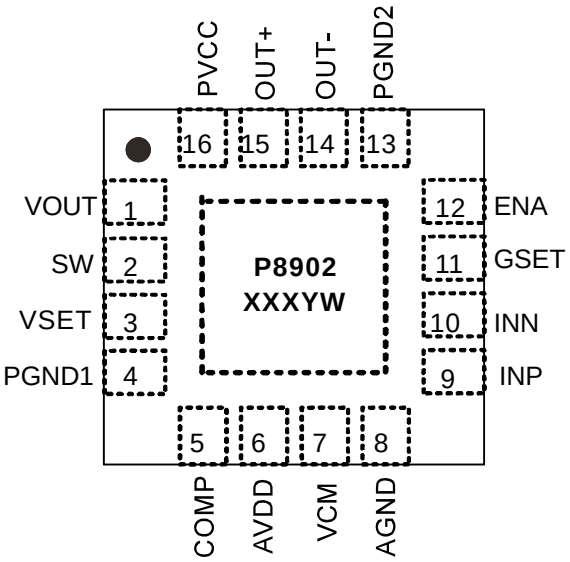


Marking

BG
YW

BG: Product Code of PAM8902
Y: Year
W: Week

Top View
QFN 4X4 16L



Y: Year
W: Week
X: Internal Code

● : Pin 1 Indicator

Pin Configuration

Bump(CSP)	Pin NO.(QFN)	Name	Description
A1	16	PVCC	Audio Amplifier Power Supply
A2	1	VOUT	Boost Convertor Output
A3	2	SW	Boost Convertor Switching Node
A4	4	PGND1	Boost Convertor Power Ground
B1	15	OUT+	Positive Differential Audio Output
B2	3	VSET	Boost Convertor Output Voltage Setting(8V,12V,17.5V)
B3	5	COMP	Boost Convertor compensation
B4	6	AVDD	Power Supply
C1	14	OUT-	Negative Differential Audio Output
C2	11	GSET	Amplifier Gain setting (18dB , 22dB , 26dB)
C3	7	VCM	Common Mode bypass Cap
C4	8	AGND	Analog Ground
D1	13	PGND2	Class D Power Ground
D2	12	ENA	Whole chip Enable
D3	10	INN	Negative Differential Audio Input
D4	9	INP	Positive Differential Audio Input

Absolute Maximum Ratings

These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability. All voltages are with respect to ground.

Supply Voltage 6.0V
Input Voltage.....-0.3V to V_{DD}+0.3V
Storage Temperature.....-65°C to 150°C
Maximum Junction Temperature.....150°C
Soldering Temperature.....250°C,10 sec

Recommended Operating Conditions

Supply voltage Range.....2.5V to 5.5V
Ambient Temperature Range.....-40°C to 85°C
Junction Temperature Range.....-40°C to 125°C

Thermal Information

Parameter	Symbol	Package	Maximum	Unit
Thermal Resistance (Junction to ambient)	θ_{JA}	CSP	90	°C/W
		QFN4X4-16	52	
Thermal Resistance (Junction to case)	θ_{JC}	CSP	75	°C/W
		QFN4X4-16	30	

Electrical Characteristic

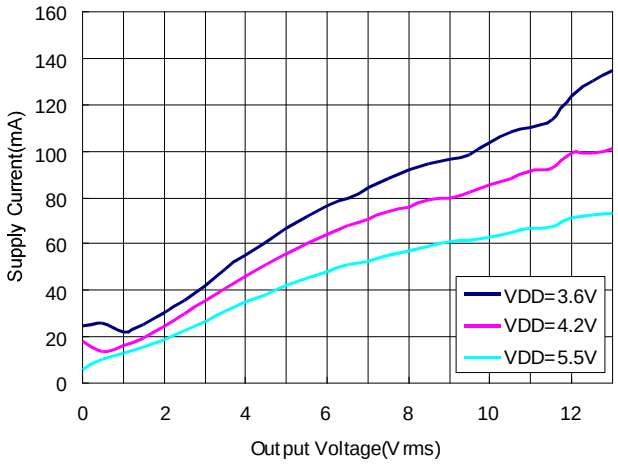
T_A=25°C, V_{DD}=3.6V,C_L=1uF,Vset float, unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage	Vdd		2.5		5.5	V
Quiescent Current	Iq	EN>1.2V, VSET = High		30	48	mA
		EN>1.2V, VSET = Floating		10	18	
		EN>1.2V, VSET = GND		5	12	
Shutdown Current	Isd	EN=0V		0.1	1	uA
Wake-Up time	Twu	EN from low to high		40		mS
Chip Enable	Veh		1.2			V
Chip Disable	Vel				0.4	
GSET/VSET High	Vh		Vdd-0.5		Vdd	V
GSET/VSET Floating	Vf		1		Vdd-1	
GSET/VSET Low	Vl		0		0.5	
Under Voltage lockout threshold	UVLO	Vdd from high to low		2.2		V
Under Voltage lockout Hysteresis	UVLOh	Vdd from low to high		0.2		
Thermal shutdown threshold	OTP			150		℃
Thermal shutdown lockout Hysteresis	OTPh			30		℃
Boost Convertor						
Output Voltage	Vo1	VSET=GND , No load	7.2	8	8.8	V
	Vo2	VSET=NC , No load	10.8	12	13.2	V
	Vo3	VSET=AVDD , No load	16	17.5	19	V
Current Limit	Cl	Average input current		0.8		A
Low Side Mosfet Rdson	Rls	Io=50mA		0.5		Ω
Boost switching frequency	Foscb		1.1	1.5	1.9	MHz
Class D						
Class D Amplifier Switching Frequency	Foscd	Input AC-GND	225	375	475	KHz
Common mode reject ratio	CMRR	Vin=+-100mV, Vdd=3.6V		60		dB
Ouput offset voltage	Vos	output offset voltage		5	50	mV
Rds on	Rp	High side		1.5		Ω
		Low side		0.6		Ω
Closed-loop voltage gain	Av1	Gset=AVDD,Vo=1Vrms	25	26	27	dB
	Av2	Gset=NC,Vo=1Vrms	21	22	23	
	Av3	Gset=GND,Vo=1Vrms	17	18	19	
Power supply reject ratio	PSRR	200mVpp supply ripple at 217Hz		70		dB
Total harmonic distortion plus noise	THD+N	Vo=5Vrms		0.3		%
Signal to noise ratio	SNR	Input AC Ground,A-weighting		90		dB

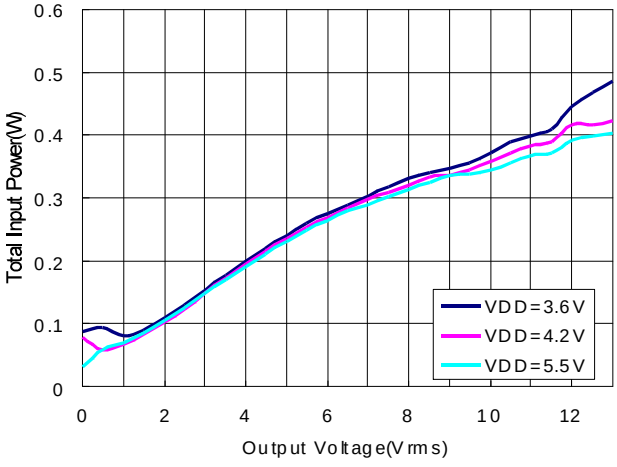
Typical Operating Characteristics

T_A=25°C, V_{DD}=4.2V,Gain=26dB,Cin=1uF,Cload=1uF, unless otherwise noted.

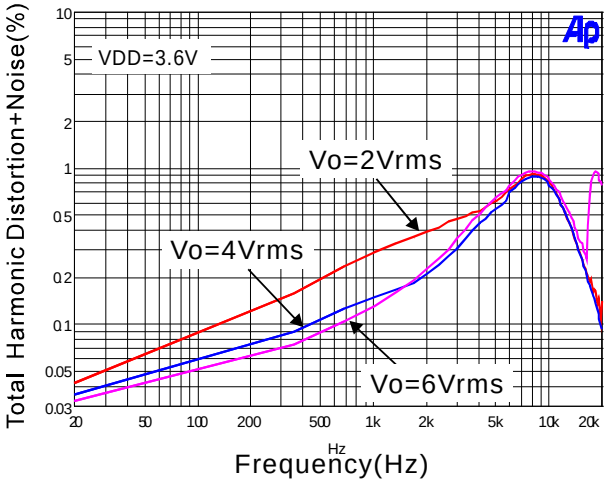
1. Total Supply Current VS Output Voltage



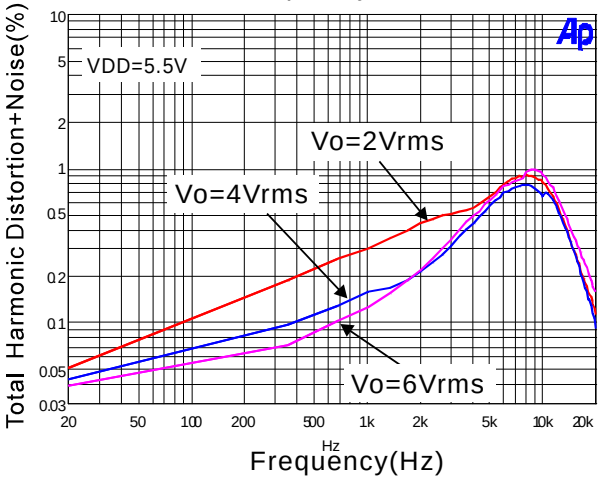
2. Total Input Power VS Output Voltage



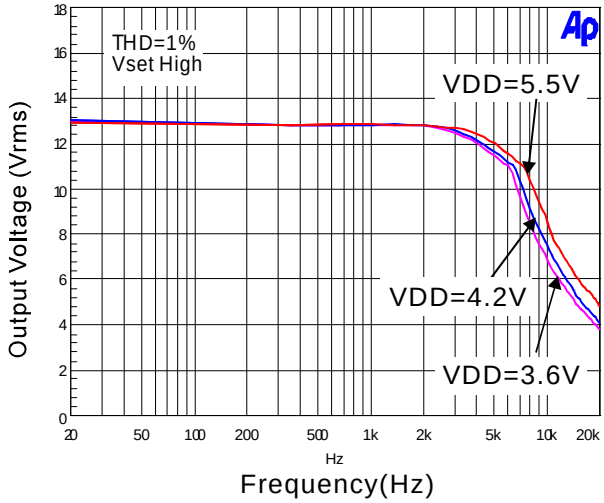
3. THD+N VS Frequency



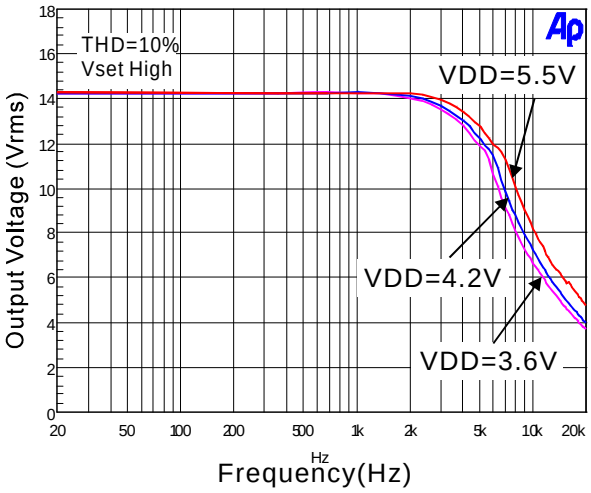
4. THD+N VS Frequency



5. Output Voltage RMS VS Frequency



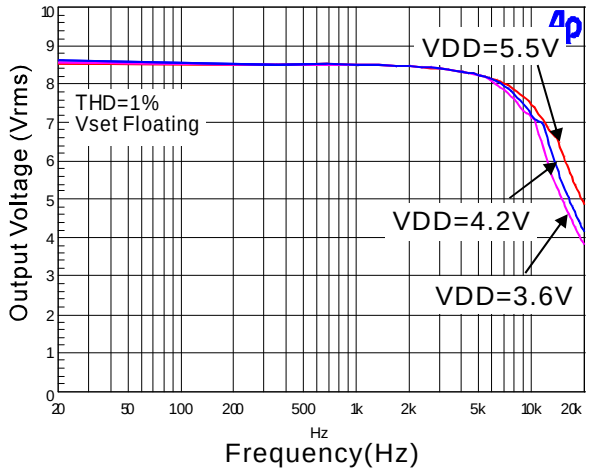
6. Output Voltage RMS VS Frequency



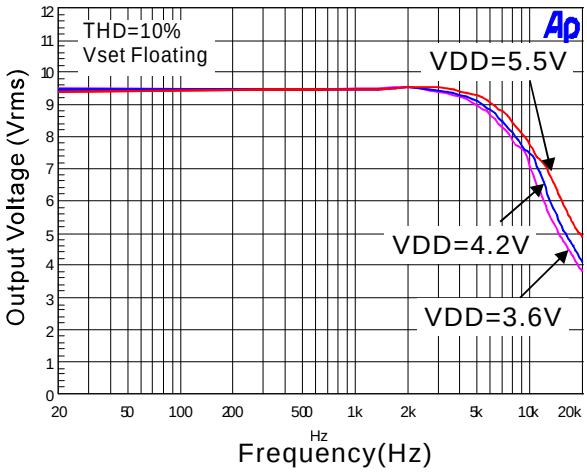
Typical Operating Characteristics

T_A=25°C, V_{DD}=5V,Gain=18dB, unless otherwise noted.

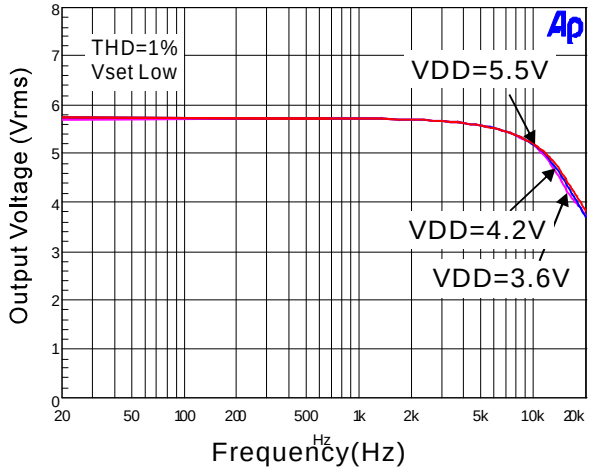
7. Output Voltage RMS VS Frequency



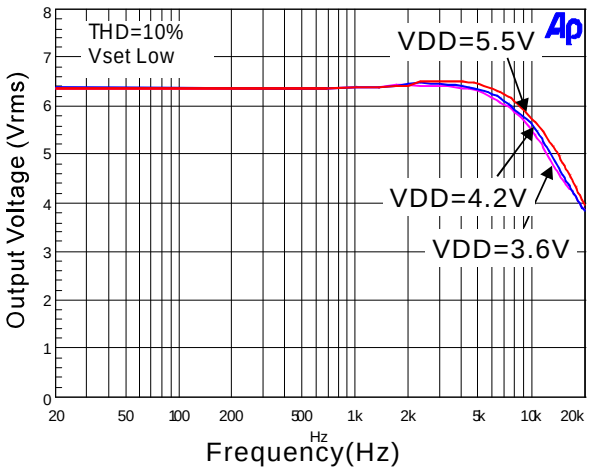
8. Output Voltage RMS VS Frequency



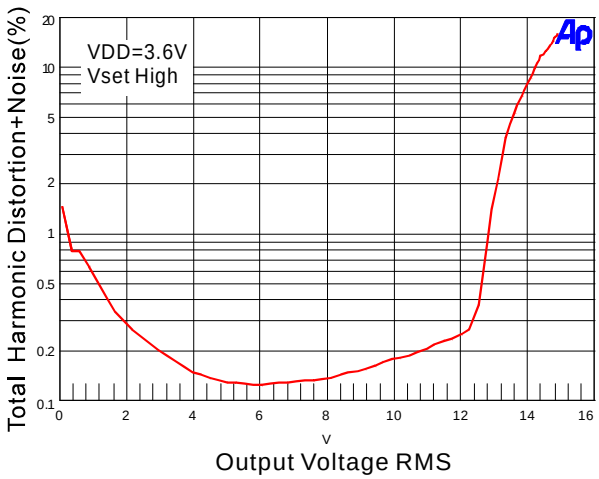
9. Output Voltage RMS VS Frequency



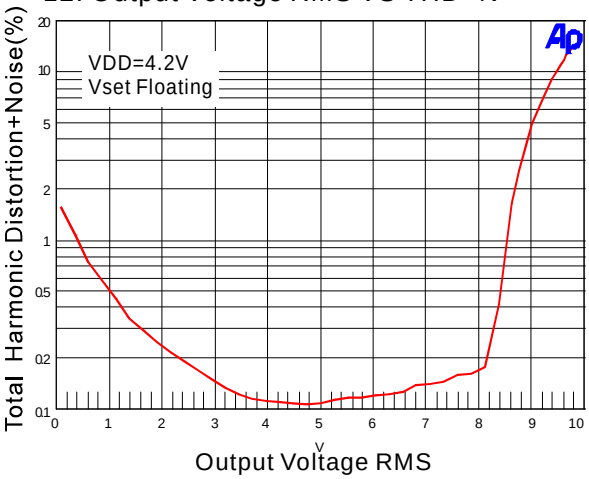
10. Output Voltage RMS VS Frequency



11. Output Voltage RMS VS THD+N



12. Output Voltage RMS VS THD+N



Application Information

Select Boost Convertor Output Voltage

Customer can use Vset pin to set boost converor output voltage between 8V,12V and 17.5V.
Vset pin configuration table as below:

Vset pin configuration	Min	Max	PVCC Voltage	Audio amplifier maximum output voltage
Connect to AVDD	AVDD - 0.5V	AVDD	17.5V	11Vrms (Vpp=31.1V)
Floating	1V	AVDD - 1V	12V	8Vrms(Vpp=22.6V)
Connect to GND	GND	0.5V	8V	5Vrms(Vpp=14.1V)

Input Resistance (Ri)

The input resistors (Ri=Rin+Rex) set the gain of the amplifier according to Equation 1 when anti-saturation is inactive.

G=20 Log [12.8*Rf/(Rin+Rex)] (dB)

Gset	Rin	Rfb
Gset=Vdd	77.4kΩ	122.6kΩ
Gset=Floating	100kΩ	100kΩ
Gset=GND	122.6kΩ	77.4kΩ

Where Rin is a 77.4KΩ internal resistor, Rex is the external input resistor,Rf is a 122.6KΩ internal resistor. Resistor matching is very important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and cancellation of the second harmonic distortion diminish if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized. Matching is more important than overall tolerance. Resistor arrays with 1% matching can be used with a tolerance greater than 1%.
Place the input resistors very close to the PAM8902 to limit noise injection on the high-impedance nodes.
For optimal performance the gain should be set to lower. Lower gain allows the PAM8902 to operate at its best, and keeps a high voltage at the input making the inputs less susceptible to noise. In addition to these features, higher value of Ri minimizes pop noise.

Input Capacitors (Ci)

In the typical application, an input capacitor, Ci, is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, Ci and the minimum input impedance Ri form is a high-pass filter with the corner frequency determined in the follow equation:

$$fc = \frac{1}{2\pi RiCi}$$

It is important to consider the value of Ci as it directly affects the low frequency performance of the circuit. For example, when Ri is 150kΩ and the specification calls for a flat bass response are down to 150Hz.
Equation is reconfigured as followed:

$$Ci = \frac{1}{2\pi Rifc}$$

When input resistance variation is considered, the Ci is 7nF, so one would likely choose a value of 10nF. A further consideration for this capacitor is the leakage path from the input source through the input network (Ci, Ri + Rf) to the load. This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the DC level is held at $V_{DD}/2$, which is likely higher than the source DC level. Please note that it is important to confirm the capacitor polarity in the application.

Decoupling Capacitor

The PAM8902 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) as low as possible.
The optimum decoupling is achieved by using two different types of capacitors that target on different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a

Application Information

good low equivalentseries-resistance (ESR) ceramic capacitor, typically 1μF, is placed as close as possible to the device AVDD pin for the best operation. For filtering lower frequency noise signals, a large ceramic capacitor of 10μF or greater placed near the AVDD supply trace is recommended.

External Schottky Diode
Use external schottky diode can get the best driving capability and efficiency.
Since internal power diode has limited driving capability ,only in following conditions customer can remove the external schottky diode to reduce the cost.
1. Vset = GND or Floating and C_L less than 1uF.
2. The signal frequency less than 4KHz.
3. Haptic application (50-500Hz)

Shutdown operation
In order to reduce power consumption while not in use, the PAM8902 contains shutdown circuitry amplifier off when a logic low is placed on the ENA pin. By switching the ENA pin connected to GND, the PAM8902 supply current draw will be minimized in idle mode.

Under Voltage Lock-out (UVLO)
The PAM8902 incorporates circuitry designed to detect supply voltage. When the supply voltage drops to 2.2V or below, the PAM8902 goes into a state of shutdown, and the device comes out of its shutdown state and restore to normal function only when reset the power supply or ENA pin.

Short Circuit Protection (SCP)
The PAM8902 has short circuit protection circuitry on the outputs to prevent the device from damage when output-to-output shorted or output-to-GND shorted occurs. When a short circuit occurs, the device goes into a latch state and must be reset by cycling the voltage on the ENA pin to a logic low and then back to the logic high state for normal operation. This will clear the short-circuit flag and allow for normal operation if the short was removed. If the short was not removed, the protection circuitry will again activate.

Over Temperature Protection (OTP)
Thermal protection on the PAM8902 prevents the device from damage when the internal die temperature exceeds 150°C. There is a 15°C tolerance on this trip point from device to device. Once the die temperature exceeds the set point, the device will enter the shutdown state and the outputs are disabled,in this condition both OUT+ and OUT- will become high impedance. This is not a latched fault. The thermal fault is cleared once the temperature of the die decreased by 30°C. This large hysteresis will prevent motor boating sound well and the device begins normal operation at this point with no external system interaction.

Ordering Information

PAM8902 X X X - P

- P: PAM Confidential
- X: Number of pins
- X: Package Type
- X: Pin Configuration

Part Number	Marking	Package Type	MOQ
PAM8902ZER-P	BG YW	CSP-16L	3,000 Units/ Tape & Reel
PAM8902KER-P	P8902 XXXYW	QFN4X4-16L	3,000 Units/ Tape & Reel

Marking Instruction

Y : Last Digital of Manufacturing Year

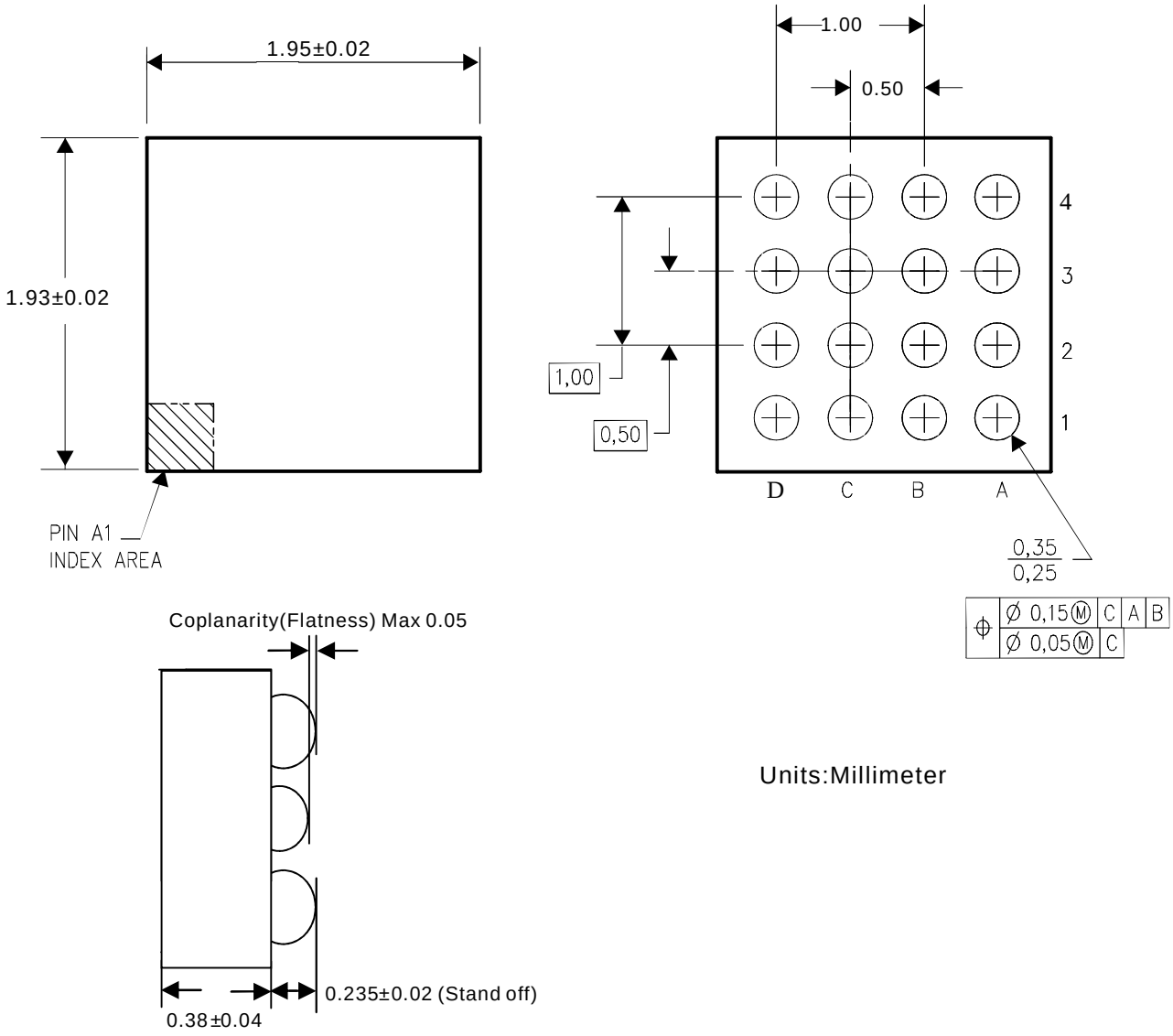
6: 2006
7: 2007
8: 2008
9: 2009
0: 2010
1: 2011

W : Week Code

Item	Week code	Item	Week code	Item	Week code	Item	Week code
1	A	14	N	27	A	40	N
2	B	15	O	28	B	41	O
3	C	16	P	29	C	42	P
4	D	17	Q	30	D	43	Q
5	E	18	R	31	E	44	R
6	F	19	S	32	F	45	S
7	G	20	T	33	G	46	T
8	H	21	U	34	H	47	U
9	I	22	V	35	I	48	V
10	J	23	W	36	J	49	W
11	K	24	X	37	K	50	X
12	L	25	Y	38	L	51	Y
13	M	26	Z	39	M	52	Z

Outline Dimensions

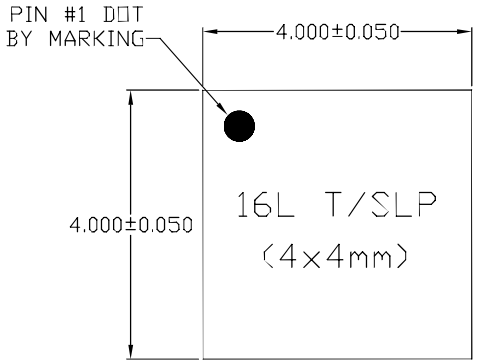
CSP-16



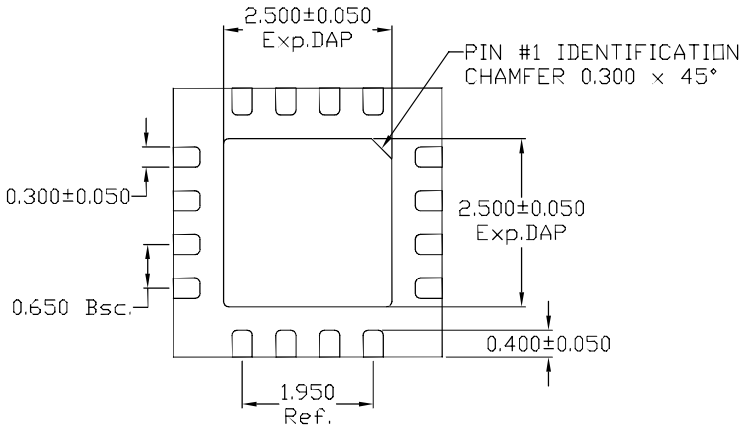
Units:Millimeter

Outline Dimensions

QFN4X4-16



TOP VIEW



BOTTOM VIEW

NOTE:
1) TSLP AND SLP SHARE THE SAME EXPOSE OUTLINE BUT WITH DIFFERENT THICKNESS:

		TSLP	SLP
A	MAX.	0.800	0.900
	NOM.	0.750	0.850
	MIN.	0.700	0.800

SIDE VIEW

A

Datasheet Revision History

Date	Revision	Description	Comment
03/03/2011	Advanced	Change product code from "BH" to "BG"	
04/07/2011	Preliminary	Update "Block Diagram"	
05/25/2011	Rev1.0	Initially released	
11/22/2011	Rev1.1	Add "Application Information"	
12/15/2011	Rev1.2	Add "-P" to the part number in "Ordering Information"	
12/22/2011	Rev1.3	Add "Pin1 Indicator" on page3 and add "Marking Instruction" on page10 Update "Thermal Information" and"Electrical Charateristic"	
12/28/2011	Rev1.3	Add "Coplanarity(Flatness)" value in the outline dimension	
01/05/2012	Rev1.4	Add "PSRR, THD+N, SNR" parameters to spec	