Integrated Device Technology, Inc.

# 64K x 16 BiCMOS/CMOS STATIC RAM MODULE

**IDT7MP4027**

T-46-23-14

## FEATURES:

- High density 1 megabit static RAM module
- Low profile 40 pin DSIP (Dual Single In-line vertical Package)
- Ultra fast access time: 10ns (max.)
- Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible
- Multiple GND pins for maximum noise immunity

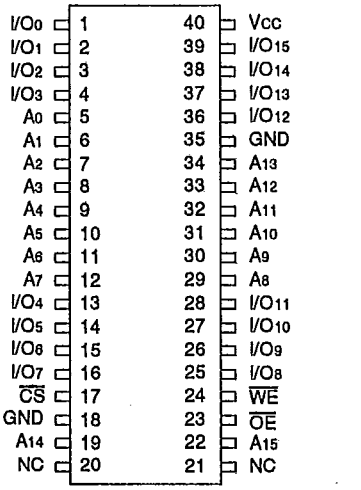
## DESCRIPTION:

The IDT7MP4027 is a 64K x 16 static RAM module constructed on an epoxy laminate (FR-4) substrate using 4 64K x 4 static RAMs in plastic SOJ packages. The IDT7MP4027 is available with access time as fast as 10ns with minimal power consumption.

The IDT7MP4027 is packaged in a 40 pin DSIP (Dual Single In-line vertical Package). This configuration allows 40 pins to be placed on a package 2 inches long, 0.35 inches thick and 0.5 inches tall.

All inputs and outputs of the IDT7MP4027 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

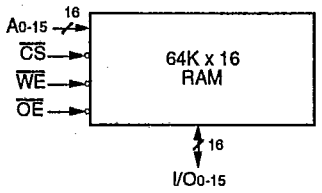
## PIN CONFIGURATION




2843 drw 01

**DSIP**
**TOP VIEW**

## FUNCTIONAL BLOCK DIAGRAM




2843 drw 02

## PIN NAMES

| | |
|---|---|
| A0-15 | Addresses |
| I/O0-15 | Data Inputs/Outputs |
| $\overline{CS}$ | Chip Select |
| $\overline{WE}$ | Write Enable |
| $\overline{OE}$ | Output Enable |
| NC | No Connect |
| Vcc | Power |
| GND | Ground |

2843 tbl 01

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## CAPACITANCE (TA = +25°C, F = 1.0MHZ)

| Symbol | Parameter[1] | Conditions | Max. | Unit |
|---|---|---|---|---|
| CI/O | Data I/O Capacitance | V(IN) = 0V | 15 | pF |
| CIN | Input Capacitance (Address and Control) | V(IN) = 0V | 40 | pF |

NOTE: 2843 tbl 02
1. This parameter is guaranteed by design but not tested.

## TRUTH TABLE

| Mode | $\overline{CS}$ | $\overline{OE}$ | $\overline{WE}$ | Output | Power |
|---|---|---|---|---|---|
| Standby | H | X | X | High Z | Standby |
| Read | L | L | H | DATAOUT | Active |
| Write | L | X | L | DATAIN | Active |
| Read | L | H | H | High-Z | Active |

2843 tbl 05

## RECOMMENDED DC OPERATING CONDITIONS

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| VCC | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| GND | Supply Voltage | 0 | 0 | 0 | V |
| VIH | Input High Voltage | 2.2 | — | 6.0 | V |
| VIL | Input Low Voltage | –0.5[1] | — | 0.8 | V |

NOTE: 2843 tbl 03
1. VIL (min) = –1.5V for pulse width less than 10ns.

## ABSOLUTE MAXIMUM RATINGS[1]

| Symbol | Rating | Value | Unit |
|---|---|---|---|
| VTERM | Terminal Voltage with Respect to GND | –0.5 to +7.0 | V |
| TA | Operating Temperature | 0 to +70 | °C |
| TBIAS | Temperature Under Bias | –10 to +85 | °C |
| TSTG | Storage Temperature | –55 to +125 | °C |
| IOUT | DC Output Current | 50 | mA |

NOTE: 2843 tbl 06
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

| Grade | Ambient Temperature | GND | Vcc |
|---|---|---|---|
| Commercial | 0°C to +70°C | 0V | 5.0V ± 10% |

2843 tbl 04

## DC ELECTRICAL CHARACTERISTICS

(VCC = 5.0V ±10%, TA = 0°C to +70°C)

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| \|ILI\| | Input Leakage | VCC = Max.; VIN = GND to VCC (Address and Control) | — | 40 | µA |
| \|ILI\| | Input Leakage (Data) | VCC = Max.; VIN = GND to VCC | — | 10 | µA |
| \|ILO\| | Output Leakage | VCC = Max.; CS = VIH, VOUT = GND to VCC | — | 10 | µA |
| VOL | Output Low | VCC = Min., IOL = 8mA | — | 0.4 | V |
| VOH | Output High | VCC = Min., IOH = –4mA | 2.4 | — | V |

2843 tbl 07

| Symbol | Parameter | Test Conditions | 7MP4027B Max. | 7MP4027S Max. | Unit |
|---|---|---|---|---|---|
| ICC | Dymanic Operating Current | f = fMAX; CS = VIL VCC = Max.; Output Open | 720 | 640 | mA |
| ISB | Standby Supply Current | $\overline{CS}$ ≥ VIH, VCC = Max. Outputs Open, f = fMAX | — | 160 | mA |
| ISB1 | Full Standby Supply Current | $\overline{CS}$ ≥ VCC – 0.2V; f = 0 VIN > VCC – 0.2V or < 0.2V | — | 120 | mA |

2843 tbl 08

## AC TEST CONDITIONS

| | |
|---|---|
| Input Pulse Levels | GND to 3.0V |
| Input Rise/Fall Times | 5ns |
| Input Timing Reference Levels | 1.5V |
| Output Reference Levels | 1.5V |
| Output Load | See Figures 1-4 |

2843 tbl 09

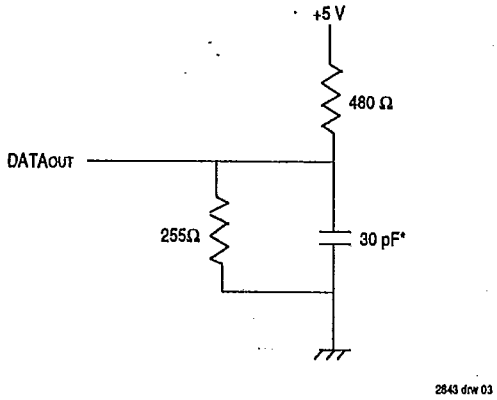


Figure 1. Output Load.

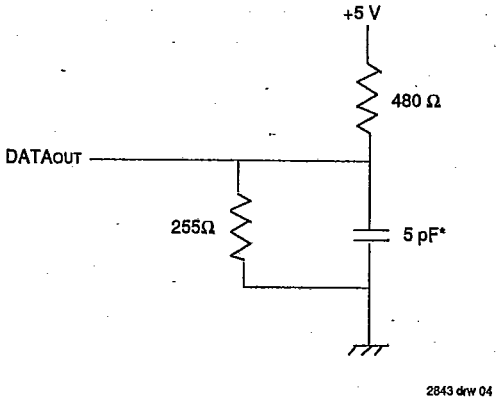


Figure 2. Output Load
(for tCLZ, tOLZ, tCHZ, tOHZ, tWHZ, and tOW)

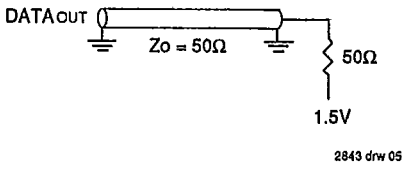


Figure 3. Alternate Output Load.

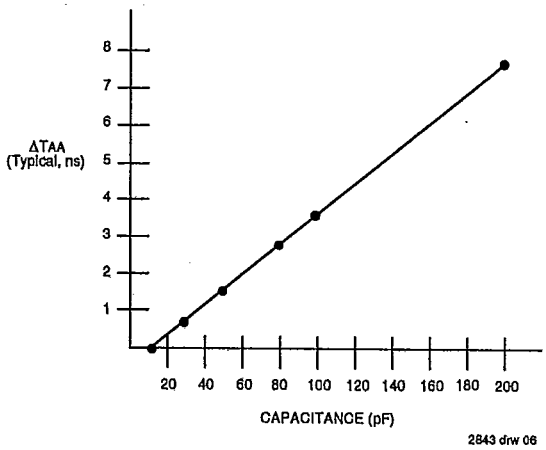


Figure 4. Alternate Lumped Capacitive Load, Typical Derating.

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## AC ELECTRICAL CHARACTERISTICS

($V_{CC}$ = 5V ±10%, $T_A$ = 0°C to +70°C)

| Symbol | Parameter | 7MP4027BxxV | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | -10[2] | | -12[2] | | -15 | | -17 | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Read Cycle** | | | | | | | | | | |
| $t_{RC}$ | Read Cycle Time | 10 | — | 12 | — | 15 | — | 17 | — | ns |
| $t_{AA}$ | Address Access Time | — | 10 | — | 12 | — | 15 | — | 17 | ns |
| $t_{ACS}$ | Chip Select Access Time | — | 4 | — | 5 | — | 6 | — | 8 | ns |
| $t_{CLZ}$[1] | Chip Select to Output in Low Z | 2 | — | 2 | — | 2 | — | 2 | — | ns |
| $t_{OE}$ | Output Enable to Output Valid | — | 4 | — | 5 | — | 6 | — | 8 | ns |
| $t_{OLZ}$[1] | Output Enable to Output in Low Z | 2 | — | 2 | — | 2 | — | 2 | — | ns |
| $t_{CHZ}$[1] | Chip Deselect to Output in High Z | — | 6 | — | 7 | — | 8 | — | 10 | ns |
| $t_{OHZ}$[1] | Output Disable to Output in High Z | — | 3 | — | 4 | — | 5 | — | 6 | ns |
| $t_{OH}$ | Output Hold from Address Change | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| **Write Cycle** | | | | | | | | | | |
| $t_{WC}$ | Write Cycle Time | 10 | — | 12 | — | 15 | — | 17 | — | ns |
| $t_{CW}$ | Chip Select to End of Write | 7 | — | 8 | — | 9 | — | 10 | — | ns |
| $t_{AW}$ | Address Valid to End of Write | 8 | — | 9 | — | 10 | — | 12 | — | ns |
| $t_{AS}$ | Address Set-up Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{WP}$ | Write Pulse Width | 8 | — | 9 | — | 10 | — | 12 | — | ns |
| $t_{WR}$ | Write Recovery Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{WHZ}$[1] | Write Enable to Output in High Z | — | 4 | — | 5 | — | 6 | — | 7 | ns |
| $t_{DW}$ | Data to Write Time Overlap | 4 | — | 5 | — | 6 | — | 8 | — | ns |
| $t_{DH}$ | Data Hold from Write Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{OW}$[1] | Output Active from End of Write | 2 | — | 2 | — | 2 | — | 2 | — | ns |

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**NOTES:**
1. This parameter is guaranteed by design, but not tested.
2. Preliminary specifications only.

## AC ELECTRICAL CHARACTERISTICS

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($V_{CC}$ = 5V ±10%, $T_A$ = 0°C to +70°C)

| Symbol | Parameter | 7MP4027SxxV -20 Min. | -20 Max. | -25 Min. | -25 Max. | -30 Min. | -30 Max. | -35 Min. | -35 Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| **Read Cycle** | | | | | | | | | | |
| $t_{RC}$ | Read Cycle Time | 20 | — | 25 | — | 30 | — | 35 | — | ns |
| $t_{AA}$ | Address Access Time | — | 20 | — | 25 | — | 30 | — | 35 | ns |
| $t_{ACS}$ | Chip Select Access Time | — | 20 | — | 25 | — | 30 | — | 35 | ns |
| $t_{CLZ}$[1] | Chip Select to Output in Low Z | 4 | — | 4 | — | 4 | — | 4 | — | ns |
| $t_{OE}$ | Output Enable to Output Valid | — | 12 | — | 12 | — | 15 | — | 20 | ns |
| $t_{OLZ}$[1] | Output Enable to Output in Low Z | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{CHZ}$[1] | Chip Deselect to Output in High Z | — | 10 | — | 15 | — | 20 | — | 20 | ns |
| $t_{OHZ}$[1] | Output Disable to Output in High Z | — | 10 | — | 15 | — | 20 | — | 20 | ns |
| $t_{OH}$ | Output Hold from Address Change | 3 | — | 3 | — | 3 | — | 3 | — | ns |
| $t_{PU}$[1] | Chip Select to Power-Up Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{PD}$[1] | Chip Deselect to Power-Down Time | — | 20 | — | 25 | — | 30 | — | 35 | ns |
| **Write Cycle** | | | | | | | | | | |
| $t_{WC}$ | Write Cycle Time | 20 | — | 25 | — | 30 | — | 35 | — | ns |
| $t_{CW}$ | Chip Select to End of Write | 15 | — | 20 | — | 25 | — | 30 | — | ns |
| $t_{AW}$ | Address Valid to End of Write | 15 | — | 20 | — | 25 | — | 30 | — | ns |
| $t_{AS}$ | Address Set-up Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{WP}$ | Write Pulse Width | 15 | — | 20 | — | 25 | — | 30 | — | ns |
| $t_{WR}$ | Write Recovery Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{WHZ}$[1] | Write Enable to Output in High Z | — | 10 | — | 15 | — | 20 | — | 20 | ns |
| $t_{DW}$ | Data to Write Time Overlap | 12 | — | 15 | — | 17 | — | 20 | — | ns |
| $t_{DH}$ | Data Hold from Write Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{OW}$[1] | Output Active from End of Write | 0 | — | 0 | — | 0 | — | 0 | — | ns |

**NOTE:**
1. This parameter is guaranteed by design, but not tested.

2643 tbl 11

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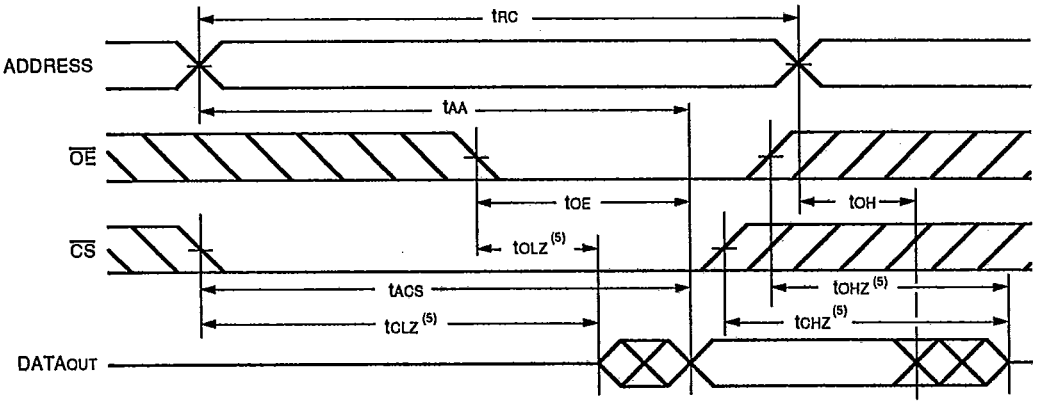
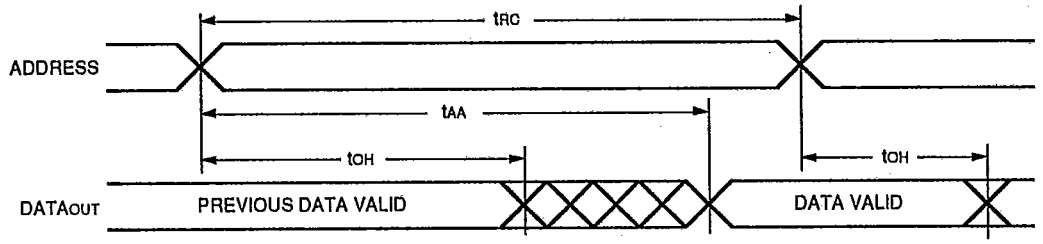
## TIMING WAVEFORM OF READ CYCLE NO. 1(1)



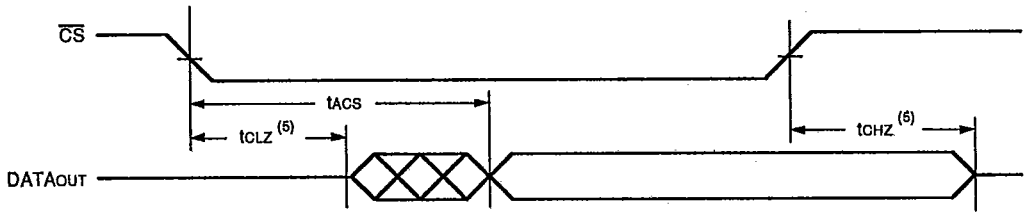

2843 drw 07

## TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)




2843 drw 08

## TIMING WAVEFORM OF READ CYCLE NO. 3(1,3,4)

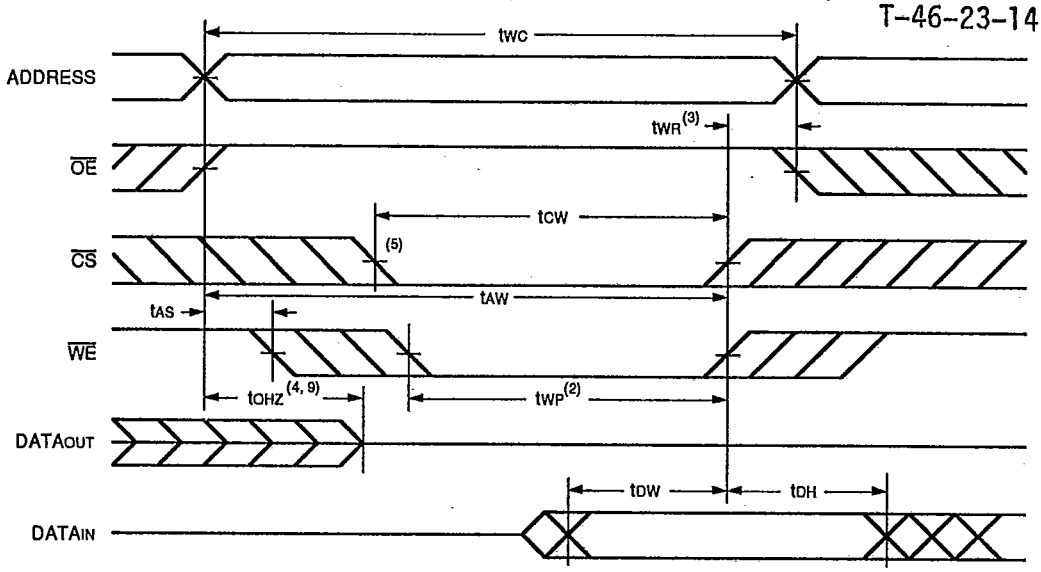



2843 drw 09

**NOTES:**
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected. $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

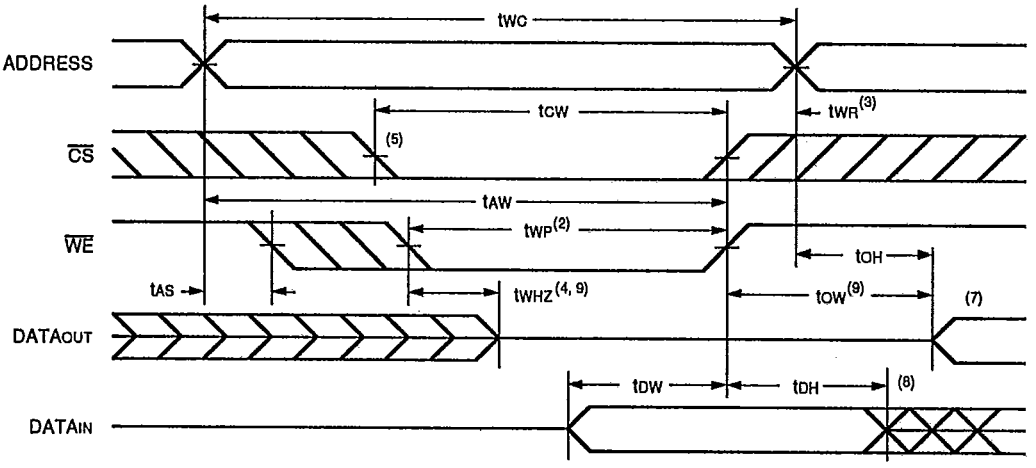
## TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)

T-46-23-14




2843 drw 10

## TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)

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**NOTES:**
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse ((tWP) > tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

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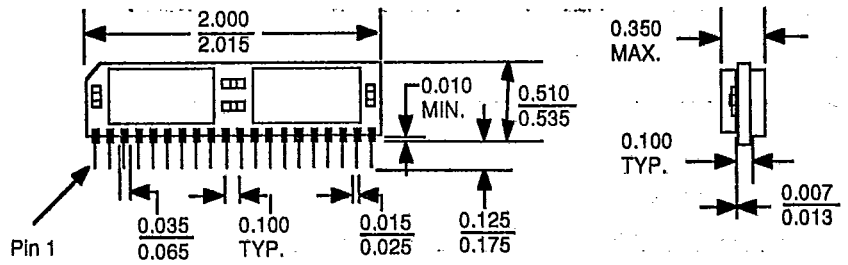
## PACKAGE DIMENSIONS




FRONT VIEW SIDE VIEW

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