SSI 78Q8392
Ethernet Coaxial Transceiver

silicon systems®
A TDK Group Company

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DESCRIPTION

The SSI 78Q8392 Ethernet Transceiver is a high speed, bipolar coax line transmitter/receiver. The device includes analog transmit and receive buffers, a 10 MHz on-board oscillator, timing logic for jabber and heartbeat functions, output drivers and bandgap reference, in addition to a current reference and collision detector.

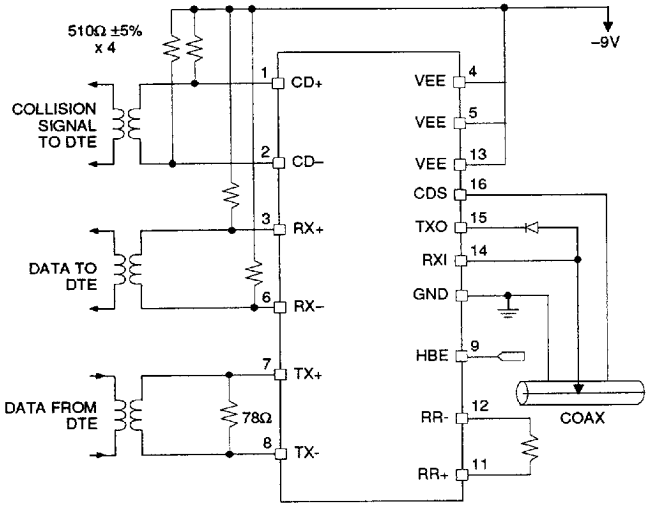
This transceiver provides the interface between the single-ended coaxial cable signals and the Manchester-encoded differential logic signals. Primary functional blocks include the receiver, transmitter, collision detection and jabber timer. This IC may be used in either internal or external MAU environments.

The SSI 78Q8392 is available in 16-pin plastic DIP and 28-pin PLCC packages.

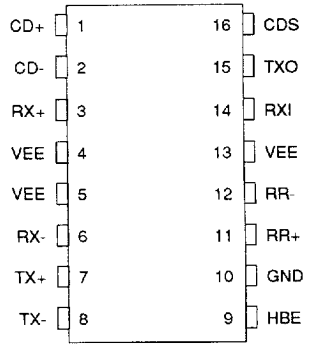
FEATURES

- **Compliant with Ethernet II, IEEE 802.3 10Base5 and 10Base2 (Cheapernet)**
- **Integrates all transceiver functions except signal and power isolation**
- **Innovative design minimizes external components count and power consumption**
- **Jabber timer function integrated on chip**
- **Externally selectable CED heartbeat allows operation with IEEE 802.3 compatible repeaters**
- **Squelch circuitry at all inputs rejects noise**

SSI 78Q8392 CONNECTION DIAGRAM



PIN DIAGRAM



16-Pin DIP

CAUTION: Use handling procedures necessary for a static sensitive component.

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FUNCTIONAL DESCRIPTION

The SSI 78Q8392 incorporates six basic functions of the Ethernet Transceiver, including receiving, transmitting, collision signaling, collision detection, jabber timing, and the heartbeat function. Refer to Figure 1 for a general system block diagram.

RECEIVER FUNCTIONS

The receiver senses signals through the RXI input, which minimizes reflections on the transmission media using a low capacitance, high resistance input buffer amplifier. The CDS ground input attaches directly to the input buffer from the coaxial shield to eliminate ground loop noise.

In addition to the input buffer, the receiver data path consists of an equalizer, data slicer, receiver squelch circuitry, and an output line driver.

The equalizer improves the jitter margin; the data slicer restores equalized received signals to fast transition signals with binary levels to drive the receiver line driver; and the receiver line driver drives the AUI cable through an isolation transformer that connects to the AUI interface.

Noise on the transmission media is rejected by the receiver squelch circuitry, which determines valid data via two criteria: DC level and pulse width. The DC voltage level is detected and compared to a set level in the receiver comparator circuit. The pulse width must be greater than 20 ns and repeat at valid data rates. It is detected using a pulse detector operating like a retriggerable one-shot that resets at approximately two signal bit times. The pulse width detector disables the receiver line driver at the end of a transmission (Figure 3).

TRANSMITTER FUNCTIONS

The transmitter data path consists of a transmit input buffer, pulse-shaping network (ramp generator), transmit squelch circuitry, a transmit driver, and transmit output line driver.

The self-biasing transmit input buffer receives data through an isolation transformer and translates the AUI differential analog signal to digital signals suitable for driving the pulse shaping network. The pulse shaping network gives equal rise and fall times to the transmit driver, which uses a high impedance current source output to drive the transmission media. The capacitance of the transmit driver is isolated from the transmission media by an external diode with a low capacitance node. The shield of the transmission media serves as the ground return for the transmitter function.

A transmit squelch circuit, which consists of a pulse threshold detector, a pulse width detector, and a pulse duration timer, is used to suppress noise, as well as crosstalk on the AUI cable. The squelch circuitry disables the transmit driver if the signal at TX+ or TX- is smaller than the pulse threshold. Pulse noise is rejected by a pulse width detector that passes only pulses with durations greater than 20 ns. The pulse duration timer disables the transmit driver if no pulses are received for two-bit periods following valid pulses. At the end of a transmission, the pulse duration timer disables the transmitter and triggers the blanking timer, used to block "dribble" bits.

COLLISION SIGNALING

When collision signaling is enabled, a 10-MHz signal is sent to the CD± pins through an isolation transformer to the Manchester encoder/decoder. When the function is disabled, this output goes to a zero differential state. The 10-MHz output from the CD pins indicates a collision on the transmission media, a heartbeat function, or that the transmitter is in jabber mode.

COLLISION DETECTION

A collision occurs when two or more transmitters simultaneously access the transmission media. A collision is detected by comparing the DC level of the transmission media to a collision threshold. The received signal at RXI is buffered and sent through a low pass filter, then compared in the collision threshold circuit. If the DC level exceeds the collision threshold, the 10-MHz oscillator and CD outputs are enabled.

JABBER FUNCTION

When valid data is transmitted, the jabber timer is started. If there is valid data for more than 20 sec, a latch is set which disables the transmitter and enables the 10-MHz output on the CD pins. The latch is reset within 0.5 seconds after the valid data is removed from the transmitter input (TX±). This action resets the jabber timer and disables the 10-MHz oscillator and CD output. The TX± inputs must remain inactive during the 0.5-second reset period.

HEARTBEAT FUNCTION

The 10-MHz oscillator and CD outputs are enabled for about 1 µs at approximately 1.1 µs after the end of each transmissions. The heartbeat signal tells the DTE that the circuit is functioning. This is implemented by starting the heartbeat timer when the valid data signal indicates the end of a transmission.

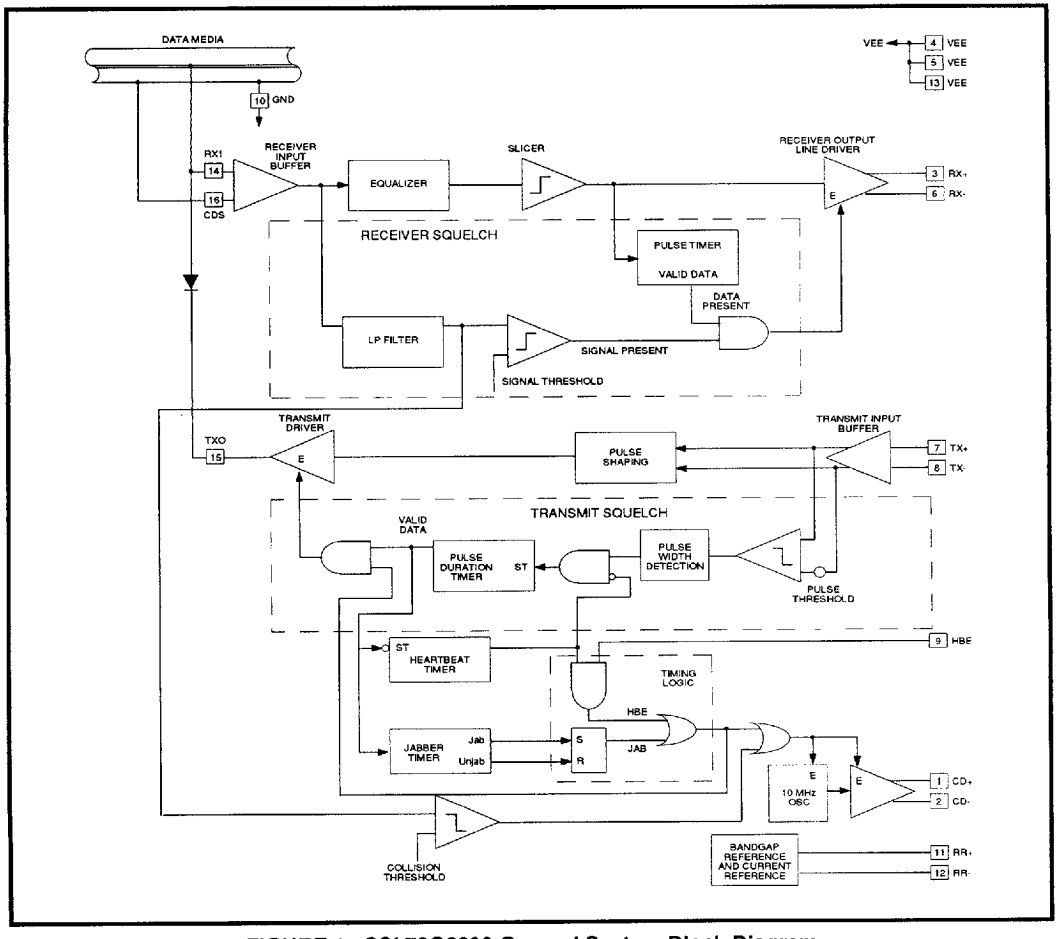

FIGURE 1: SSI 78Q8392 General System Block Diagram

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
CD+*/CD-	O	Collision Output. Balanced differential line driver outputs from the collision detect circuitry. The 10 MHz signal from the internal oscillator is transferred to these outputs in the event of collision, excessive transmission (jabber), or during CD Heartbeat condition. These outputs are open emitters; pulldown resistors to VEE are required. When operating into a 78Ω transmission line, these resistors should be 510Ω. In Cheapernet applications, where the 78Ω drop cable is not used, higher resistor values (up to 1.5k) may be used to save power.
RX+*/RX-	O	Receive Output. Balanced differential line driver outputs from the Receiver. These outputs also require 510Ω pulldown resistors.
TX+*/TX-	I	Transmit Input. Balanced differential line receiver inputs to the Transmitter. The common mode voltage for these inputs is determined internally and must not be externally established. Signals meeting Transmitter squelch requirements are waveshaped and output at TXO.
HBE	I	Heartbeat Enable. This input enables CD Heartbeat when grounded, disables it when connected to VEE.
RR+/RR-	I	External Resistor. A fixed 1k 1% resistor connected between these pins establishes internal operating currents.
RXI	I	Receive Input. Connects directly to the coaxial cable. Signals meeting Receiver squelch requirements are equalized for inter-symbol distortion, amplified, and output at RX+ and RX- pin.
TXO	O	Transmit Output. Connects either directly (Cheapernet) or via an isolation diode (Ethernet) to the coaxial cable.
CDS	I	Collision Detect Sense. Ground sense connection for the collision detect circuit. This pin should be connected separately to the shield to avoid ground drops from altering the receive mode collision threshold.
GND	–	Positive Supply Pin. A 0.1 µF ceramic de-coupling capacitor must be connected across GND and VEE as close to the device as possible.
VEE	–	Negative Supply Pins. These pins should be connected to a large metal frame area on the PC board to handle heat dissipation.

*IEEE names for CD± = CI±, RX± = DI±, TX± = DO±

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not recommended; operations should be limited to those conditions specified under recommended operating characteristics.

PARAMETER	RATING
Supply Voltage	-12V
Input Voltage	0 to -12V
Storage Temperature	-65 to 150°C
Soldering (Reflow or Dip)	300°C for 10 sec
Package power dissipation	2.5 watts @ 25°C

DC OPERATING CHARACTERISTICS

0°C < T (ambient) < +70°C, VEE = -9V + 5%

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
I_{EE1}	Supply current out of V_{EE} pin - non-transmitting			-60	-85	mA
I_{EE2}	Supply current out of V_{EE} pin - transmitting			-120	-140	mA
I_{RXI}	Receive input bias current (RXI)	See Note 3	-2		+25	µA
I_{TDC}	Transmit output dc current level (TXO)	See Note 4	37	41	45	mA
I_{TAC}	Transmit output ac current level (TXO)	See Notes 4 & 5	±28		I_{TDC}	mA
V_{CD}	Collision threshold (Receive mode)	See Note 10	-1.581	-1.52	-1.492	V
V_{OD}	Differential output voltage (RX±, CD±)	See Notes 3 & 8	±550		±1200	mV
V_{OC}	Common mode output voltage (RX±, CD±)	See Note 3, 7 & 8	-2.5	-2.0	-1.5	V
V_{OB}	Differential output voltage imbalance (RX±, CD±)	See Notes 3, 8 & 9			±40	mV
V_{TS}	Transmitter squelch threshold (TX±)		-300	-250	-175	mV
C_X	Input capacitance (RXI)			1.2		pF
R_{RXI}	Shunt resistance - non-transmitting (RXI)	See Note 3	1			MΩ
R_{TXO}	Shunt resistance - transmitting (TXO)	See Notes 4 & 6		200		kΩ

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DC OPERATING CHARACTERISTICS (continued)

NOTES

1. Currents into device pins are positive, currents out of device pins are negative. If not specified, voltages are referenced to ground.
2. All typicals are for VEE = -9V, Ta = 25°C.
3. 0 > VEE > -9.5V.
4. The voltage on TXO is -4V < V(TXO) < 0.0V.
5. The AC current measurement is referenced to the DC current level.
6. The shunt resistance does not degrade the ITAC current if five transmitters are simultaneously driving a 50Ω-terminated coax cable.
7. Operating or idle state.
8. Test load as shown in Figure 2.
9. Device measurement taken in idle state.
10. This threshold can be determined by monitoring the CD± output with a DC level in RXI.

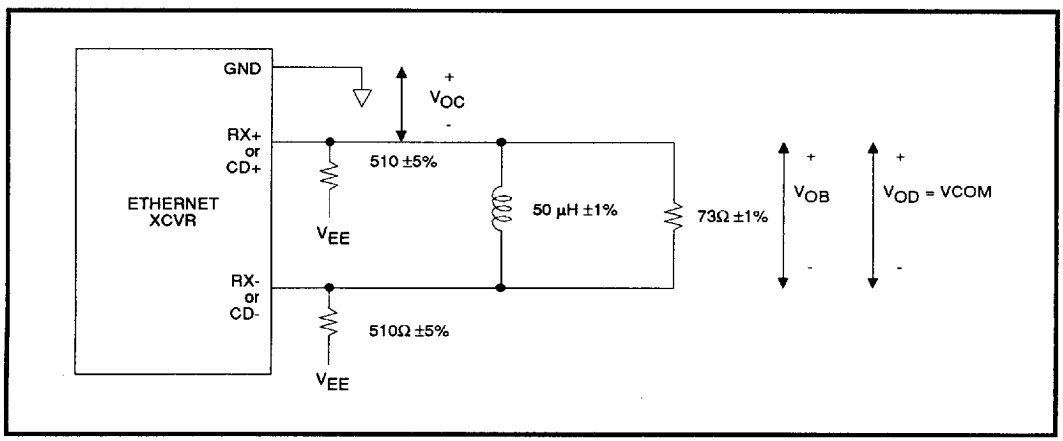


FIGURE 2: Test Load for CD± or RX±

AC OPERATING CHARACTERISTICS

0°C < T(ambient) < +70°C, VEE = 9V ± 5%

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
t_{RON} Receiver startup delay (RXI to RX±)			4	5	bits
t_{Rd} Receiver propagation delay (RXI to RX±)			15	50	ns
t_{Rr} Differential outputs rise time (RX± , CD±)			4		ns
t_{Rf} Differential outputs fall time (RX± , CD±)			4		ns
t_{RJ} Receiver & cable total jitter			2	4	ns
t_{TST} Transmitter startup delay (TX± to TXO)			1	2	bits
t_{Td} Transmitter propagation delay (TX± to TXO)			25	50	ns
t_{Tr} Transmitter rise time - 10% to 90% (TXO)		20	25	30	ns
t_{Tf} Transmitter fall time - 90% to 10% (TXO)		20	25	30	ns
t_{TM} t_{Tr} and t_{Tf} mismatch			0.5		ns
t_{TS} Transmitter skew (TXO)			±0.5		ns
t_{TON} Transmit turn-on pulse width at V_{TS} (TX±)			20		ns
t_{TOFF} Transmit turn-off pulse width at V_{TS} (TX±)			250		ns
t_{CON} Collision turn-on delay			7		bits
t_{COFF} Collision turn-off delay				20	bits
t_{CD} Collision frequency (CD±)		8.5		11.5	MHz
t_{CP} Collision pulse width (CD±)		35		70	ns
t_{HON} CD Heartbeat delay (TX± to CD±)		0.6		1.6	µs
t_{HW} CD Heartbeat duration (CD±)		0.5	1.0	1.5	µs
t_{JA} Jabber activation delay (TX± to TXO and CD±)		20		75	ms
t_{JR} Jabber reset unjab time (TX± to TXO and CD±)		250	500	750	ms

ELECTRICAL SPECIFICATIONS (continued)

TRANSMIT SPECIFICATIONS

The first bit transmitted from TXO may have data and phase violations. The second through last bit reproduce the TX± signal with less than or equal to specified jitter.

There is no logical signal inversion between Tx± and TXO output. A low level from TX+ to TX- results in more current flowing from the coaxial cable into the TXO pin.

At the end of transmission, when the transmitter changes from the enabled state to the idle state, no spurious pulses are generated, i.e., the transition on TXO proceeds monotonically to zero current.

RECEIVE SPECIFICATIONS

The first bit sent from RX± may have data and phase violations. The second through last bit reproduce the received signal with less than or equal to specified jitter.

There is no logical signal inversion between the RXI input and the RX± output. A high level at RXI produces a positive differential voltage from RX+ to RX-.

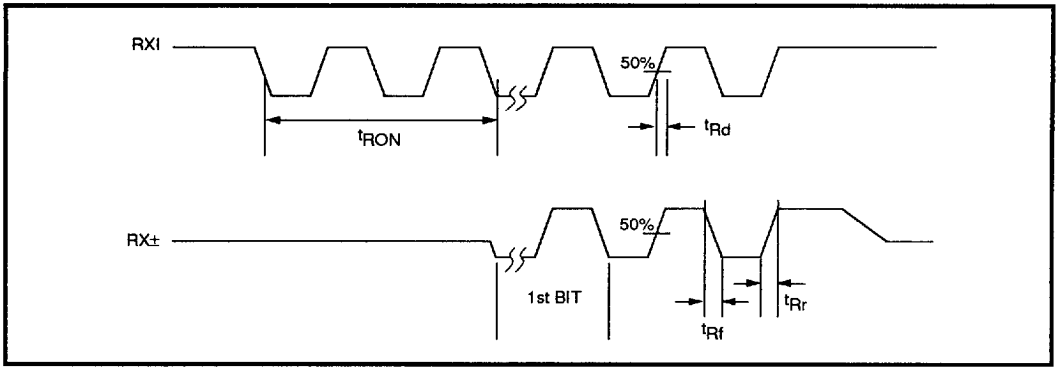


FIGURE 3: Receiver Timing

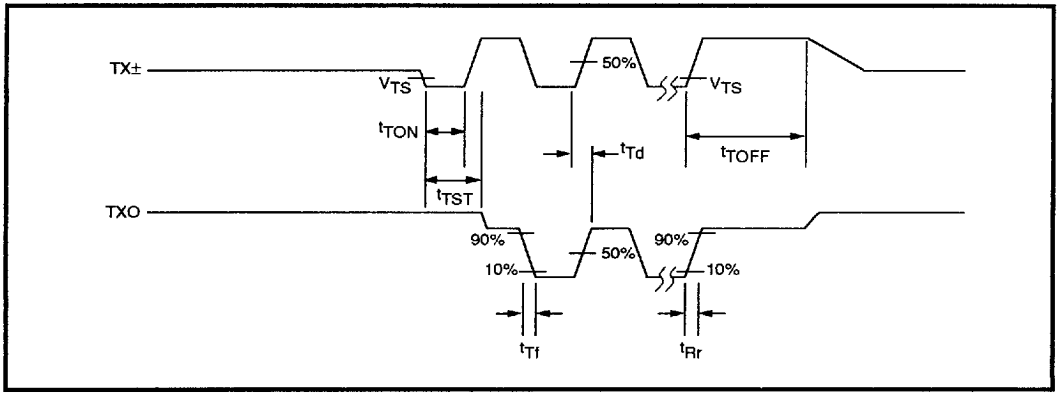


FIGURE 4: Transmitter Timing

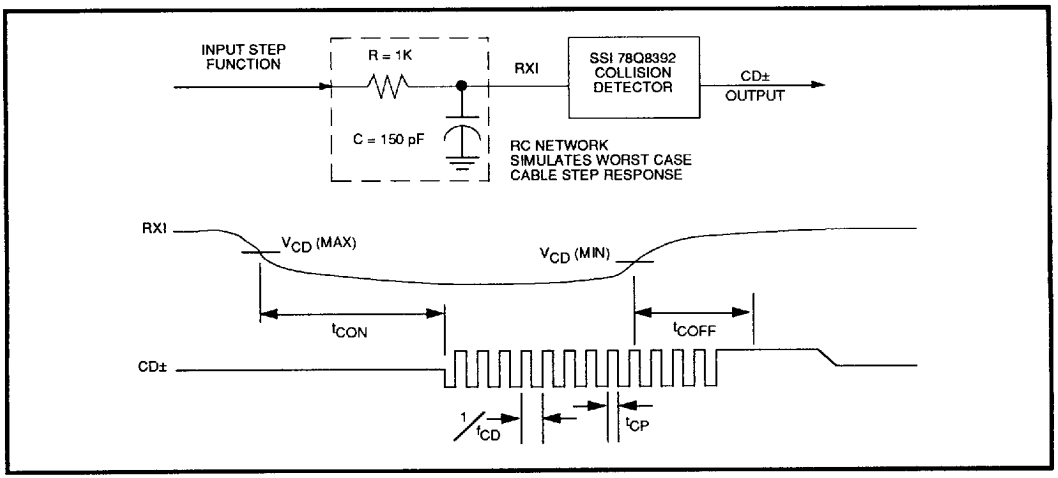


FIGURE 5: Collision Timing

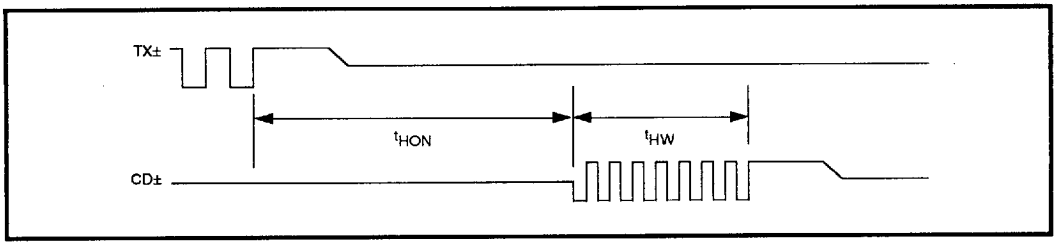


FIGURE 6: Heartbeat Timing

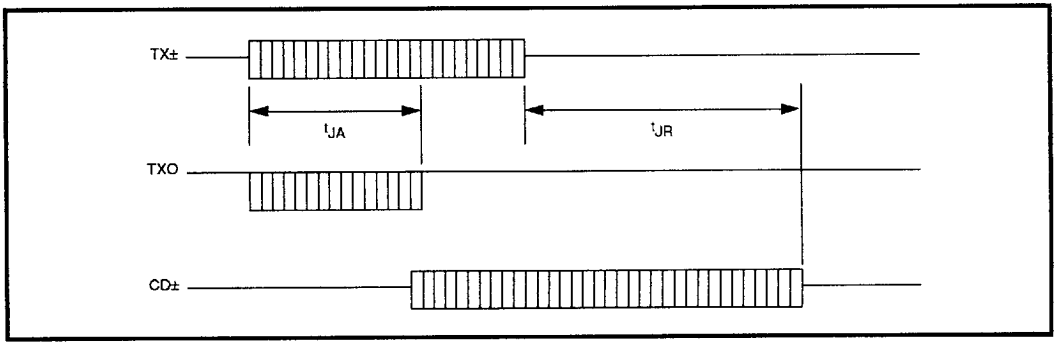


FIGURE 7: Jabber Timing

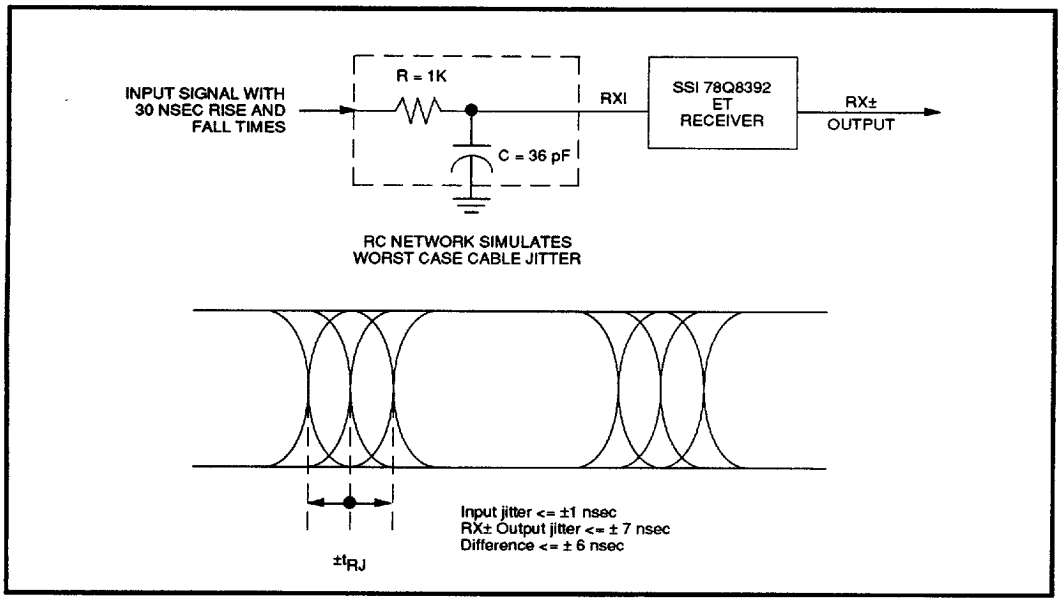


FIGURE 8: Receive Jitter Timing

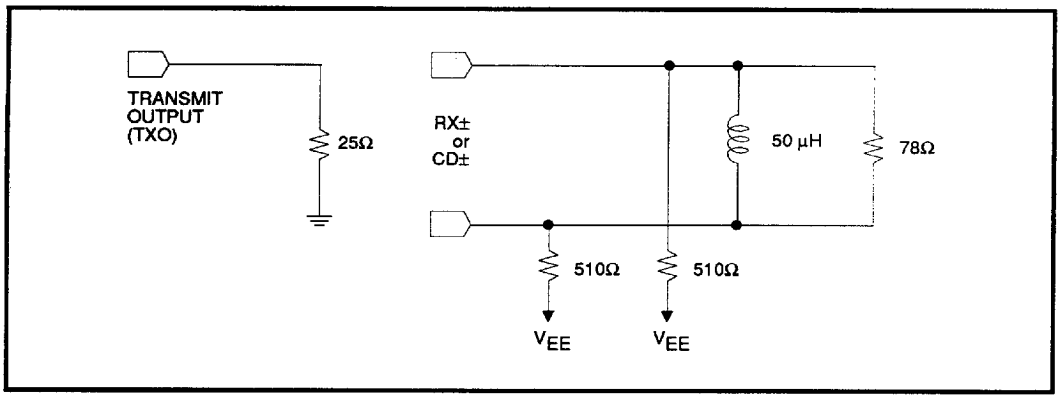
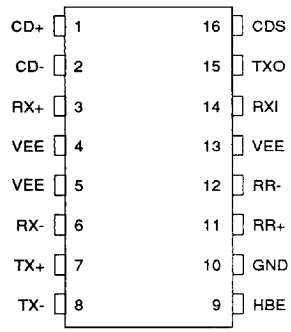


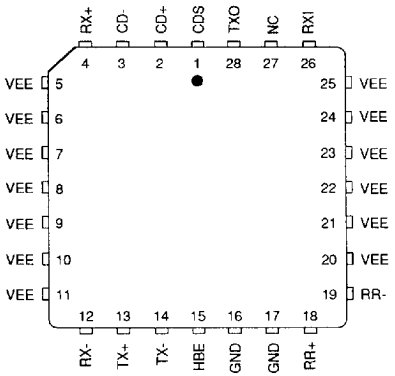
FIGURE 9: Test Loads

PACKAGE PIN DESIGNATIONS

(Top View)



16-Pin DIP



28-Pin PLCC

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGE MARK
SSI 78Q8392	16-Pin Plastic DIP	78Q8392-CP	78Q8392-CP
SSI 78Q8392	28-Pin Plastic PLCC	78Q8392-28CH	78Q8392-28CH

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