Si5351A/B/C

I²C-PROGRAMMABLE ANY-FREQUENCY CMOS CLOCK GENERATOR + VCXO

Features

- Generates up to 8 non-integer frequencies from 8 kHz to 133 MHz
- I²C user definable configuration
- Exact frequency synthesis at each output (0 ppm error)
- Highly linear VCXO
- Optional clock input (CLKIN)
- Low output period jitter: 100 ps pp
- Configurable spread spectrum selectable at each output
- Operates from a low-cost, fixed frequency crystal: 25 or 27 MHz
- Glitchless frequency changes
- Separate voltage supply pins:
  - Core VDD: 2.5 V or 3.3 V
  - Output VDDO: 2.5 V or 3.3 V
- Excellent PSRR eliminates external power supply filtering
- Very low power consumption
- Adjustable output-output delay
- Available in 3 packages types:
  - 10-MSOP: 3 outputs
  - 24-QSOP: 8 outputs
  - 20-QFN (4x4 mm): 8 outputs

10-MSOP

24-QSOP

20-QFN

Ordering Information:
See page 41

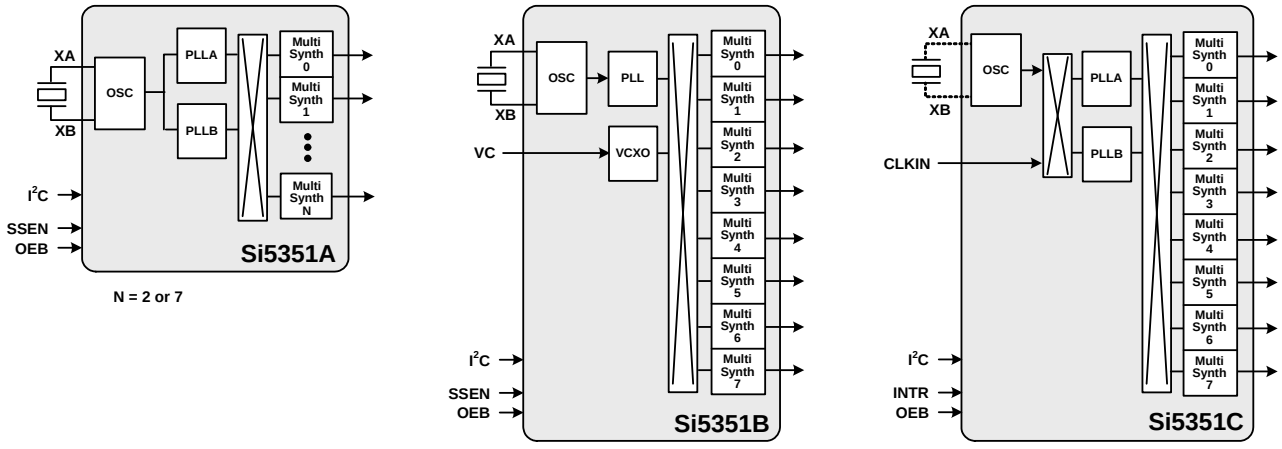
Applications

- HDTV, DVD/Blu-ray, set-top box
- Audio/video equipment, gaming
- Printers, scanners, projectors
- Residential gateways
- Networking/communication
- Servers, storage

Description

The Si5351 is an I²C configurable clock generator that is ideally suited for replacing crystals, crystal oscillators, VCXOs, phase-locked loops (PL), and fanout buffers in cost-sensitive applications. Based on a PLL/VCXO + high resolution MultiSynth fractional divider architecture, the Si5351 can generate any frequency up to 133 MHz on each of its outputs with 0 ppm error. Three versions of the Si5351 are available to meet a wide variety of applications. The Si5351A generates up to 8 free-running clocks using an internal oscillator for replacing crystals and crystal oscillators. The Si5351B adds an internal VCXO and provides the flexibility to replace both free-running clocks and synchronous clocks. The Si5351B eliminates the need for higher cost, custom pullable crystals while providing reliable operation over a wide tuning range. The Si5351C offers the same flexibility but synchronizes to an external reference clock (CLKIN).

Functional Block Diagram



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1. Electrical Specifications

Table 1. Recommended Operating Conditions

(V_{DD} = 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A		–40	25	85	°C
Core Supply Voltage	V_{DD}		2.97	3.3	3.63	V
			2.25	2.5	2.75	V
Output Buffer Voltage	V_{DDOx}		2.25	2.5	2.75	V
			2.97	3.3	3.63	V

Notes: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions.
Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.
VDD and VDDOx can be operated at independent voltages.
Power supply sequencing for VDD and VDDOx requires that both voltage rails are powered at the same time.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Value	Unit
DC Supply Voltage	V_{DD_max}		–0.5 to 3.8	V
Input Voltage	V_{IN_CLKIN}	CLKIN, SCL, SDA	–0.5 to 3.8	V
	V_{IN_VC}	VC	–0.5 to (VDD+0.3)	V
	$V_{IN\_XA/B}$	Pins XA, XB	–0.5 to 1.3 V	V
Storage Temperature Range	T_{STG}		–55 to 150	°C
Operating Junction Temperature	T_{JCT}		–55 to 150	°C

Note: Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. DC Characteristics

(V_{DD} = 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Core Supply Current	I_{DD}	Enabled 3 outputs	—	20	26	mA
		Enabled 8 outputs	—	25	38	mA
		Power Down (PDN = V_{DD})	—	50	—	µA
Output Buffer Supply Current	I_{DDOx}	C_L = 5 pF	—	2.5	4	mA
Input Current	I_{CLKIN}	CLKIN, SDA, SCL Vin < 3.6 V	—	—	10	µA
	I_{VC}	VC	—	—	30	µA

Table 4. AC Characteristics

(V_{DD} = 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power-up Time	T_{RDY}	From V_{DD} = V_{DDmin} to valid output clock, C_L = 15 pF, f_{CLKn} > 1 MHz	—	1	10	ms
Output Enable Time	T_{OE}	From OEB assertion to valid clock output, C_L = 15 pF, f_{CLKn} > 1 MHz	—	—	10	µs
Output Phase Offset	P_{STEP}		—	357	—	ps/step
Spread Spectrum Frequency Deviation	SS_{DEV}	Down spread	–0.1	—	–2.5	%
		Center spread	±0.1	—	±1.5	%
Spread Spectrum Modulation Rate	SS_{MOD}		30	31.5	33	kHz
VCXO Specifications (Si5351B only)						
VCXO Control Voltage Range	Vc		0	V_{DD}/2	V_{DD}	V
VCXO Gain (configurable)	Kv	Vc = 10–90% of V_{DD}, V_{DD} = 3.3 V	30	—	250	ppm/V
VCXO Control Voltage Linearity	KVL	Vc = 10–90% of V_{DD}	–5	—	+5	%
VCXO Pull Range (configurable)	PR	V_{DD} = 3.3 V*	±40	0	±330	ppm
VCXO Modulation Bandwidth			—	10	—	kHz
VCXO Period Jitter			—	60	110	ps
VCXO Cycle-Cycle Jitter			—	50	95	ps pk-pk
VCXO RMS Phase Jitter			—	8.5	18.5	ps rms
PLL Input Frequency Range	f_{CLKIN}		10	—	100	MHz
***Note:** Contact Silicon Labs for 2.5 V VCXO operation.						

Table 5. Thermal Characteristics

Parameter	Symbol	Test Condition	Package	Value	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	10-MSOP	131	°C/W
			24-QSOP	80	°C/W
			20-QFN	51	°C/W
Thermal Resistance Junction to Case	θ_{JC}	Still Air	10-MSOP	43	°C/W
			24-QSOP	31	°C/W
			20-QFN	16	°C/W

Table 6. Input Characteristics

(V_{DD} = 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
CLKIN Input Low Voltage	V_{IL}		–0.1	—	0.3 x V_{DD}	V
CLKIN Input High Voltage	V_{IH}		0.7 x V_{DD}	—	3.63	V

Table 7. Output Characteristics

(V_{DD} = 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Frequency Range	F_{CLK}		0.008	—	133	MHz
Load Capacitance	C_L		—	5	15	pF
Duty Cycle	DC	Measured at $V_{DD}/2$, f_{CLK} = 50 MHz	45	50	55	%
Rise/Fall Time	t_r	20%–80%, C_L = 5 pF	0.6	1	1.3	ns
	t_f		0.6	1	1.3	ns
Output High Voltage	V_{OH}	C_L = 5 pF	V_{DD} – 0.6	—	—	V
Output Low Voltage	V_{OL}		—	—	0.6	V
Period Jitter	J_{PER}	Measured over 10k cycles	—	35	100	ps pk
Period Jitter VCXO	J_{PER_VCXO}		—	60	110	ps pk
Cycle-to-Cycle Jitter	J_{CC}	Measured over 10k cycles	—	30	90	ps pk-pk
Cycle-to-Cycle Jitter VCXO	J_{CC_VCXO}		—	50	95	ps pk-pk
RMS Phase Jitter	J_{RMS}	12 kHz–20 MHz	—	3.5	11	ps rms
RMS Phase Jitter VCXO	J_{RMS_VCXO}		—	8.5	18.5	ps rms

Table 8. Crystal Requirements[1,2]

Parameter	Symbol	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}	25	—	27	MHz
Load Capacitance	C_L	6	—	12	pF
Equivalent Series Resistance	r_{ESR}	—	—	150	Ω
Crystal Max Drive Level	d_L	—	—	100	µW

Notes:
1. Crystals which require load capacitances of 6, 8, or 10 pF should use the device's internal load capacitance for optimum performance. See register 183 bits 7:6. A crystal with a 12 pF load capacitance requirement should use a combination of the internal 10 pF load capacitors in addition to external 2 pF load capacitors.
2. Refer to "AN551: Crystal Selection Guide" for more details.

Table 9. I²C Specifications (SCL,SDA)[1]

Parameter	Symbol	Test Condition	Standard Mode 100 kbps		Fast Mode 400 kbps		Unit
			Min	Max	Min	Max	
LOW Level Input Voltage	V_{ILI2C}		–0.5	0.3 x V_{DDI2C}	–0.5	0.3 x V_{DDI2C}[2]	V
HIGH Level Input Voltage	V_{IHI2C}		0.7 x V_{DDI2C}	3.63	0.7 x V_{DDI2C}[2]	3.63	V
Hysteresis of Schmitt Trigger Inputs	V_{HYS}		—	—	0.1	—	V
LOW Level Output Voltage (open drain or open collector) at 3 mA Sink Current	V_{OLI2C}[2]	V_{DDI2C}[2] = 2.5/3.3 V	0	0.4	0	0.4	V
		V_{DDI2C}[2] = 1.8 V	—	—	0	0.2 x V_{DDI2C}	V
Input Current	I_{II2C}		–10	10	–10	10	µA
Capacitance for Each I/O Pin	C_{II2C}	V_{IN} = –0.1 to V_{DDI2C}	—	4	—	4	pF
I²C Bus Timeout	T_{TO}	Timeout Enabled	25	35	25	35	ms

Notes:
1. Refer to NXP's UM10204 I²C-bus specification and user manual, revision 03, for further details: www.nxp.com/acrobat_download/usermanuals/UM10204_3.pdf.
2. Only I²C pullup voltages (VDDI2C) of 2.25 to 3.63 V are supported.

2. Functional Description

The Si5351 is a versatile I^{2}C programmable clock generator that is ideally suited for replacing crystals, crystal oscillators, VCXOs, PLLs, and buffers. A block diagram showing the general architecture of the Si5351 is shown in Figure 1. The device consists of an input stage, two synthesis stages, and an output stage.

The input stage accepts an external crystal (XTAL), a clock input (CLKIN), or a control voltage input (VC) depending on the version of the device (A/B/C). The first stage of synthesis multiplies the input frequencies to an high-frequency intermediate clock, while the second stage of synthesis uses high resolution MultiSynth fractional dividers to generate the desired output frequencies. Additional integer division is provided at the output stage for generating output frequencies as low as 8 kHz. Crosspoint switches at each of the synthesis stages allows total flexibility in routing any of the inputs to any of the outputs.

Because of this high resolution and flexible synthesis architecture, the Si5351 is capable of generating synchronous or free-running non-integer related clock frequencies at each of its outputs, enabling one device to synthesize clocks for multiple clock domains in a design.

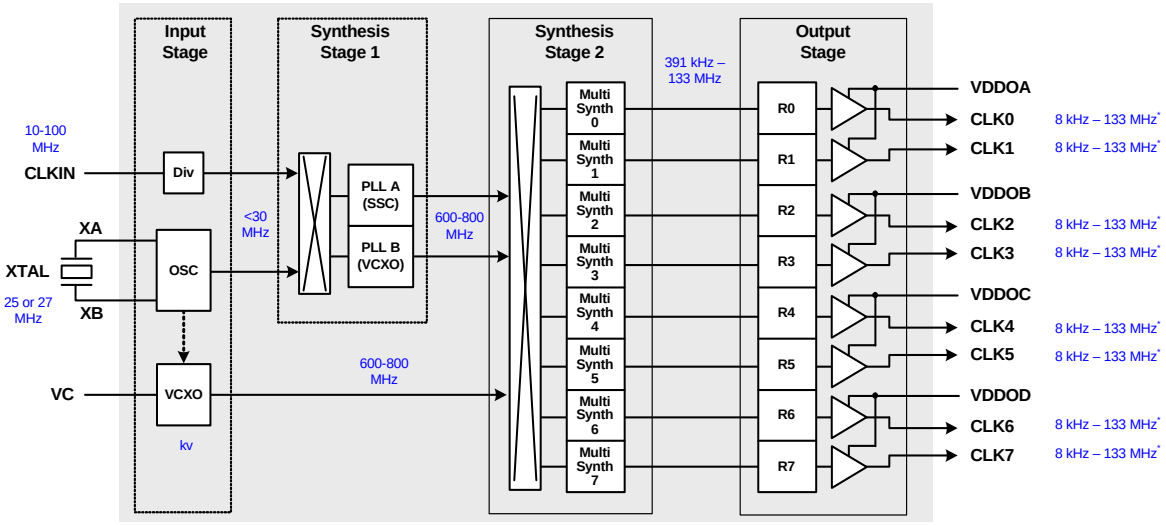


Figure 1. Si5351 Block Diagram

2.1. Input Stage

2.1.1. Crystal Inputs (XA, XB)

The Si5351 uses a fixed-frequency standard AT-cut crystal as a reference to the internal oscillator. The output of the oscillator can be used to provide a free-running reference to one or both of the PLLs for generating asynchronous clocks. The output frequency of the oscillator will operate at the crystal frequency, either 25 MHz or 27 MHz. The crystal is also used as a reference to the VCXO to help maintain its frequency accuracy.

Internal load capacitors (C_L) are provided to eliminate the need for external components when connecting a crystal to the Si5351. Options for internal load capacitors are 6, 8, or 10 pF. Crystals with alternate load capacitance requirements are supported using additional external load capacitors as shown in Figure 2. Refer to application note AN551 for crystal recommendations.

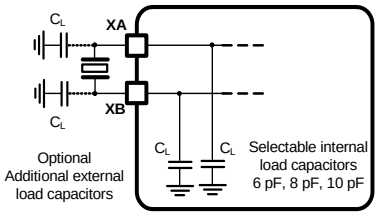


Figure 2. External XTAL with Optional Load Capacitors

2.1.2. External Clock Input (CLKIN)

The external clock input is used as a clock reference for the PLLs when generating synchronous clock outputs. CLKIN can accept any frequency from 10 to 100 MHz. A divider at the input stage limits the PLL input frequency to 30 MHz.

2.1.3. Voltage Control Input (VC)

The internal VCXO generates a center frequency in the range of 600 MHz to 800 MHz that is controlled (pulled) by the voltage applied at the VC input pin. The unique design of the VCXO eliminates the need for an external pullable crystal. Only a standard, low-cost, fixed-frequency (25 MHz or 27 MHz) AT-cut crystal is required.

The tuning range of the VCXO is configurable from 10ppm to 1000ppm to satisfy a wide variety of applications. Key advantages of the VCXO design in the Si5351 include high linearity, a wide operating range (linear from 10 to 90% of VDD), and reliable startup and operation.

2.2. Synthesis Stages

The Si5351 uses two stages of synthesis to generate its final output clocks. The first stage uses PLLs to multiply the lower frequency input references to a high-frequency intermediate clock in the range of 600 - 800 MHz. The second stage uses high-resolution MultiSynth fractional dividers to generate frequencies in the range of ~391 kHz to 100 MHz. It is also possible to generate two frequencies up to 133 MHz on two or more of the outputs.

A crosspoint switch at the input of the first stage allows each of the PLLs to lock to the CLKIN or the XTAL input. This allows each of the PLLs to lock to a different source for generating independent free-running and synchronous clocks. Alternatively, both PLLs could lock to the same source. The crosspoint switch at the input of the second stage allows any of the MultiSynth dividers to connect to PLLA or PLLB. This flexible synthesis architecture allows any of the outputs to generate synchronous or non-synchronous clocks, with spread spectrum or without spread spectrum, and with the flexibility of generating non-integer related clock frequencies at each output.

Since the VCXO already generates a high-frequency intermediate clock, it is fed directly into the second stage of synthesis. The MultiSynth high-resolution dividers synthesize the VCXO center frequency to any frequency in the range of ~391 kHz to 133 MHz. The center frequency is then controlled (or pulled) by the VC input. An interesting feature of the Si5351 is that the VCXO output can be routed to more than one MultiSynth divider. This creates a VCXO with multiple output frequencies controlled from one VC input as shown in Figure 3.

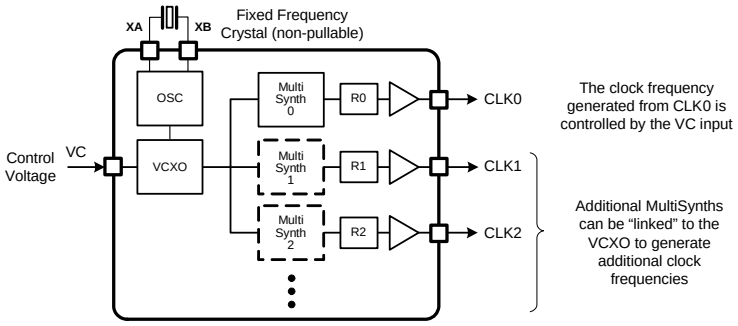


Figure 3. Using the Si5351 as a Multi-Output VCXO

2.3. Output Stage

An additional level of division (R) is available at the output stage for generating clocks as low as 8 kHz. All output drivers generate CMOS level outputs with separate output voltage supply pins (VDDOx) allowing a different voltage signal level (3.3V or 2.5V) at each of the four 2-output banks.

2.4. Spread Spectrum

Spread spectrum can be enabled on any of the clock outputs that use PLLA as its reference. Spread spectrum is useful for reducing electromagnetic interference (EMI). Enabling spread spectrum on an output clock modulates its frequency, which effectively reduces the overall amplitude of its radiated energy. Up to –15 dB reduction in EMI is possible. Note that spread spectrum is not available on clocks synchronized to PLLB or to the VCXO.

The Si5351 supports several levels of spread spectrum allowing the designer to chose an ideal compromise between system performance and EMI compliance. The amount of spread is configurable with the following:

- Down spread: –0.5 to –2.5% modulation amplitude
- Center spread: ±0.1 to ±1.5% modulation amplitude

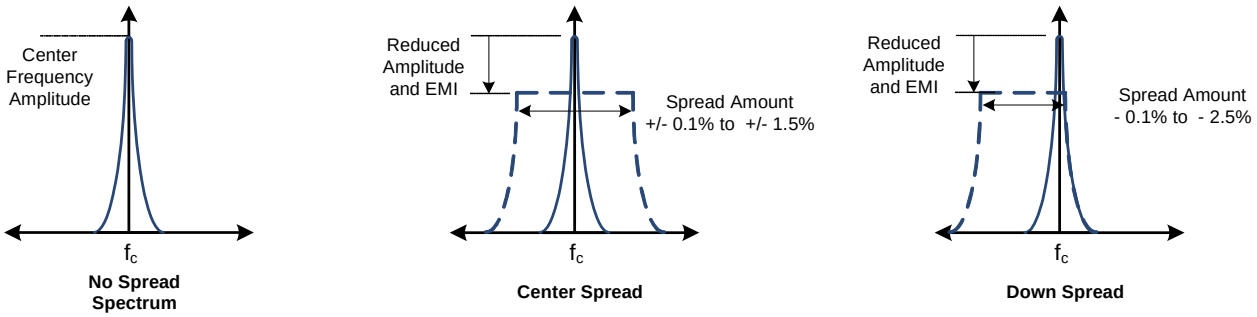


Figure 4. Available Spread Spectrum Profiles

2.5. Control Pins (OEB, SSEN)

The Si5351 offers control pins for enabling/disabling clock outputs and spread spectrum.

2.5.1. Output Enable (OEB)

The output enable pin allows enabling or disabling outputs clocks. Output clocks are enabled when the OEB pin is held low, and disabled when pulled high. When disabled, the output state is configurable as disabled high, disabled low, or disabled in high-impedance.

The output enable control circuitry ensures glitchless operation by starting the output clock cycle on the first leading edge after OEB is asserted (OEB = low). When OEB is released (OEB = high), the clock is allowed to complete its full clock cycle before going into a disabled state. The operation of the output enable pin is shown in Figure 5.

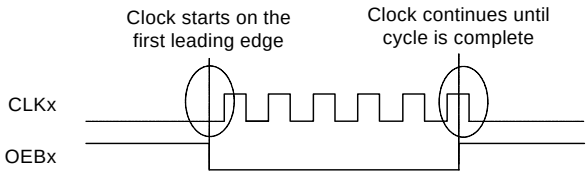


Figure 5. Glitchless Output Enable/Disable

2.5.2. Spread Spectrum Enable (SSEN)—Si5351A and Si5351B only

This control pin allows disabling the spread spectrum feature for all outputs that were configured with spread spectrum enabled. Hold SSEN low to disable spread spectrum. The SSEN pin provides a convenient method of evaluating the effect of using spread spectrum clocks during EMI compliance testing.

3. I²C Interface

Many of the functions and features of the Si5351 are controlled by reading and writing to the RAM space using the I²C interface. The following is a list of the common features that are controllable through the I²C interface. A summary of register functions is shown in Section 7.

- Read Status Indicators
  - Loss of signal (LOS) for the CLKIN input
  - Loss of lock (LOL) for PLLA and PLLB
- Configuration of multiplication and divider values for the PLLs, MultiSynth dividers
- Configuration of the Spread Spectrum profile (down or center spread, modulation percentage)
- Control of the cross point switch selection for each of the PLLs and MultiSynth dividers
- Set output clock options
  - Enable/disable for each clock output
  - Invert/non-invert for each clock output
  - Output divider values (2^n, n=1.. 7)
  - Output state when disabled (stop hi, stop low, Hi-Z)
  - Output phase offset

The I²C interface operates in slave mode with 7-bit addressing and can operate in Standard-Mode (100 kbps) or Fast-Mode (400 kbps) and supports burst data transfer with auto address increments.

The I²C bus consists of a bidirectional serial data line (SDA) and a serial clock input (SCL) as shown in Figure 6. Both the SDA and SCL pins must be connected to the VDD supply via an external pull-up as recommended by the I²C specification.

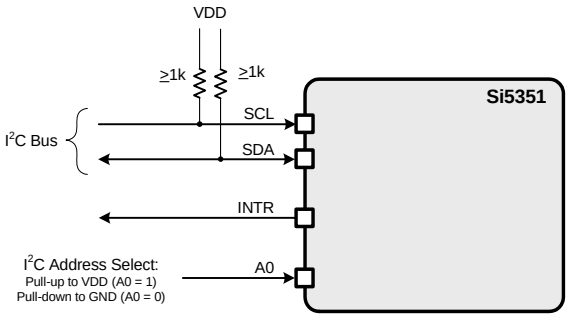


Figure 6. I²C and Control Signals

The 7-bit device (slave) address of the Si5351 consist of a 6-bit fixed address plus a user selectable LSB bit as shown in Figure 7. The LSB bit is selectable as 0 or 1 using the optional A0 pin which is useful for applications that require more than one Si5351 on a single I²C bus.

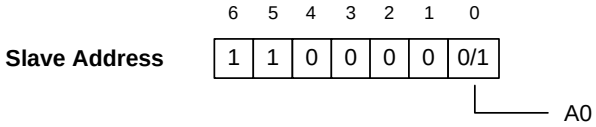


Figure 7. Si5351 I²C Slave Address

Data is transferred MSB first in 8-bit words as specified by the I²C specification. A write command consists of a 7-bit device (slave) address + a write bit, an 8-bit register address, and 8 bits of data as shown in Figure 8. A write burst operation is also shown where every additional data word is written using to an auto-incremented address.

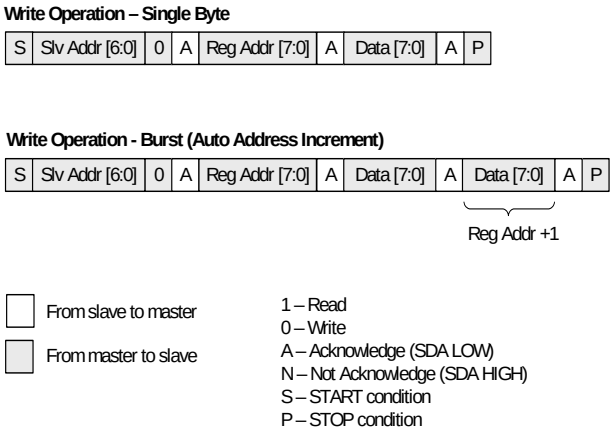


Figure 8. I²C Write Operation

A read operation is performed in two stages. A data write is used to set the register address, then a data read is performed to retrieve the data from the set address. A read burst operation is also supported. This is shown in Figure 9.

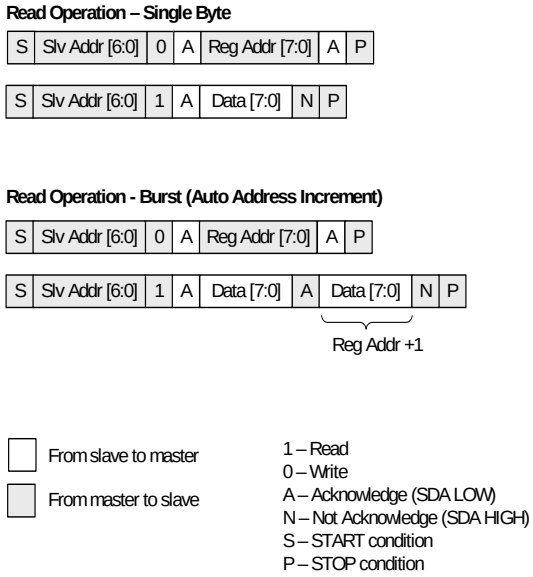


Figure 9. I²C Read Operation

AC and DC electrical specifications for the SCL and SDA pins are shown in Table 9. The timing specifications and timing diagram for the I²C bus is compatible with the I²C-Bus Standard. SDA timeout is supported for compatibility with SMBus interfaces.

4. Configuring the Si5351

The Si5351 is a highly flexible clock generator which is entirely configurable through its I^2C interface. The device's default configuration is stored in non-volatile memory (NVM) as shown in Figure 10. The NVM is a one time programmable memory (OTP) which can store a custom user configuration at power-up. This is a useful feature for applications that need a clock present at power-up (e.g., for providing a clock to a processor).

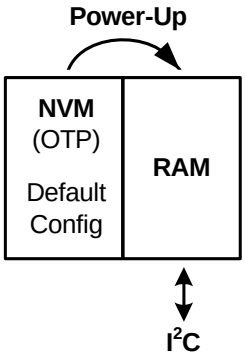


Figure 10. Si5351 Memory Configuration

During a power cycle the contents of the NVM are copied into random access memory (RAM), which sets the device configuration that will be used during normal operation. Any changes to the device configuration after power-up are made by reading and writing to registers in the RAM space through the I^2C interface. A detailed register map is shown in Section 9.

A development kit supports field programming which allows writing a custom configuration directly to the NVM. Since NVM is an OTP memory, it can only be written once. The default configuration is always re-configurable by writing to RAM through the I^2C interface after power up.

5. Si5351 Application Examples

The Si5351 is a versatile clock generator which serves a wide variety of applications. The following examples show how it can be used to replace crystals, crystal oscillators, VCXOs, and PLLs.

5.1. Replacing Crystals and Crystal Oscillators

Using an inexpensive external crystal, the Si5351A can generate up to 8 different free-running clock frequencies for replacing crystals and crystal oscillators. A 3 output version packaged in a small 10-MSOP is also available for applications that require fewer clocks. An example is shown in Figure 11.

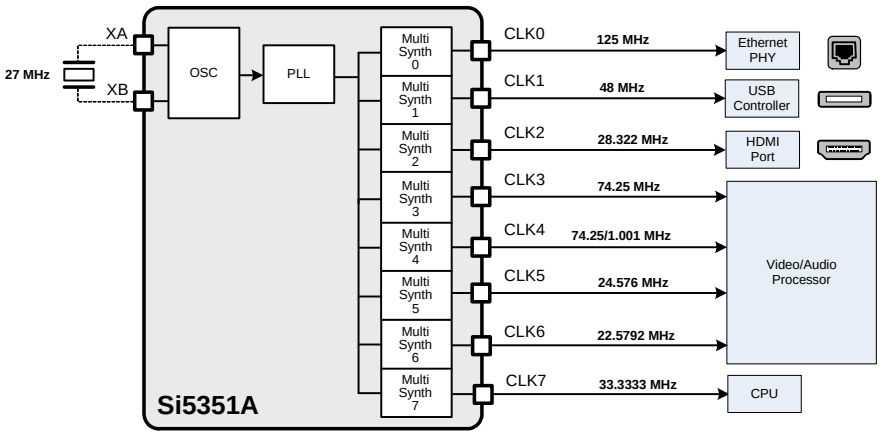
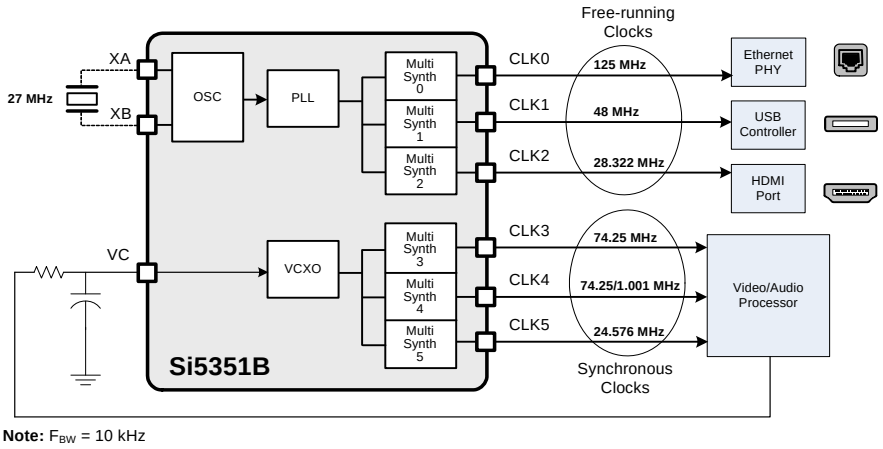


Figure 11. Using the Si5351A to Replace Multiple Crystals, Crystal Oscillators, and PLLs

5.2. Replacing Crystals, Crystal Oscillators, and VCXOs

The Si5351B combines free-running clock generation and a VCXO in a single package for cost sensitive video applications. An example is shown in Figure 12.



Note: F_{BW} = 10 kHz

Figure 12. Using the Si5351B to Replace Crystals, Crystal Oscillators, VCXOs, and PLLs

5.3. Replacing Crystals, Crystal Oscillators, and PLLs

The Si5350C generates synchronous clocks for applications that require a fully integrated PLL instead of a VCXO. Because of its dual PLL architecture, the Si5351C is capable of generating both synchronous and free-running clocks. An example is shown in Figure 13.

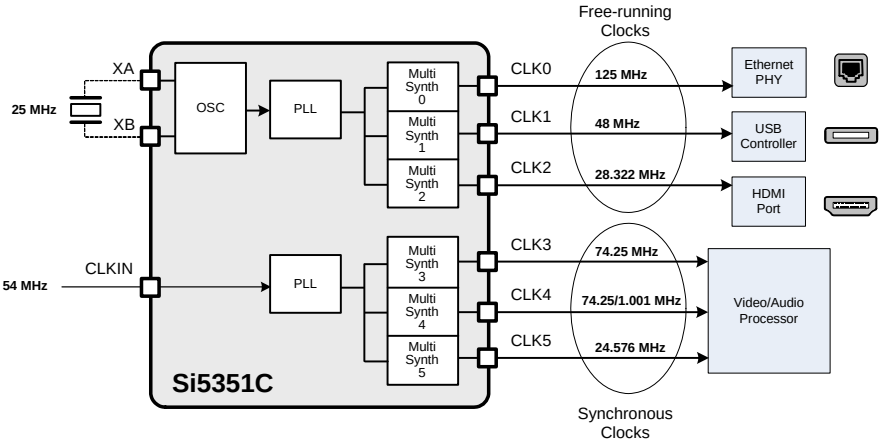


Figure 13. Using the Si5351C to Replace Crystals, Crystal Oscillators, and PLLs

6. External Component Recommendations

The Si5351 is a self-contained clock generator that requires very few external components. The following general guidelines are recommended to ensure optimum performance. Refer to application note AN554 for additional layout recommendations.

6.1. Power Supply Decoupling/Filtering

The Si5351 has built-in power supply filtering circuitry to help minimize the number of external components. All that is recommended is one 0.1 µF decoupling capacitor per power supply pin. This capacitor should be mounted as close to the VDD and VDDOx pins as possible without using vias.

6.2. Power Supply Sequencing

The VDD and VDDOx (i.e., VDDO0, VDDO1, VDDO2, VDDO3) power supply pins have been separated to allow flexibility in output signal levels. It is important that power is applied to all supply pins (VDD, VDDOx) simultaneously. Unused VDDOx pins should be tied to VDD.

6.3. External Crystal

The external crystal should be mounted as close to the pins as possible using short PCB traces. The XA and XB traces should be kept away from other high-speed signal traces. See “AN551: Crystal Selection Guide” for more details.

6.4. External Crystal Load Capacitors

The Si5351 provides the option of using internal and external crystal load capacitors. If external load capacitors are used, they should be placed as close to the XA/XB pads as possible. See “AN554: Layout Recommendations” for more details.

6.5. Unused Pins

Unused voltage control pin should be tied to GND.

Unused CLKIN pin should be tied to GND.

Unused XA/XB pins should be tied to GND.

Unused output pins (CLK0–CLK7) should be left floating.

Unused VDDOx pins should be tied to VDD.

7. Register Map Summary

The following is a summary of the register map used to read status, control, and configure the Si5351.

Register	7	6	5	4	3	2	1	0
0	SYS_INIT	LOL_B	LOL_A	LOS			REVID[1:0]	
1	SYSCAL_ STKY	LOS_B_ STKY	LOL_A_ STKY	LOS_ STKY				
2	SYSCAL_ MASK	LOS_B_ MASK	LOL_A _ MASK	LOS_ MASK				
3	CLK7_EN	CLK6_EN	CLK5_EN	CLK4_EN	CLK3_EN	CLK2_EN	CLK1_EN	CLK0_EN
4–8	Reservedt							
9	OEB_CLK7	OEB_CLK6	OEB_CLK5	OEB_CLK4	OEB_CLK3	OEB_CLK2	OEB_CLK1	OEB_CLK0
10–14	Reserved							
15	0	0	0	0	PLLB_SRC	PLLA_SRC	0	0
16	CLK0_PDN	MS0_INT	MS0_SRC	CLK0_INV				
17	CLK1_PDN	MS1_INT	MS1_SRC	CLK1_INV				
18	CLK2_PDN	MS2_INT	MS2_SRC	CLK2_INV				
19	CLK3_PDN	MS3_INT	MS3_SRC	CLK3_INV				
20	CLK4_PDN	MS4_INT	MS4_SRC	CLK4_INV				
21	CLK5_PDN	MS5_INT	MS5_SRC	CLK5_INV				
22	CLK6_PDN	MS6_INT	MS6_SRC	CLK6_INV				
23	CLK7_PDN	MS7_INT	MS6_SRC	CLK7_INV				
24	CLK3_DIS_STATE		CLK2_DIS_STATE		CLK1_DIS_STATE		CLK0_DIS_STATE	
25	CLK7_DIS_STATE		CLK6_DIS_STATE		CLK5_DIS_STATE		CLK4_DIS_STATE	
26–172	PLL, MultiSynth, and output clock delay offset Configuration Registers. Use ClockBuilder Desktop Software to Determine These Register Values.							
173–176	Reserved							
177	PLLB_RST		PLLA_RST					
178–182	Reserved							
183	XTAL_CL							
184–255	Reserved							

8. Register Descriptions

Register 0. Interrupt Status Sticky

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SYS_INIT	LOL_B	LOL_A	LOS			REVID[1:0]	
Type	R	R	R	R	R	R	R	R

Reset value = 0000 0000

Bit	Name	Function
7	SYS_INIT	**System Initialization Status.** During power up the device copies the content of the NVM into RAM and performs a system initialization. The device is not operational until initialization is complete. It is not recommended to read or write registers in RAM through the I^2C interface until initialization is complete. An interrupt will be triggered (INTR pin = 1, Si5351C only) during the system initialization period. 0: System initialization is complete. Device is ready. 1: Device is in system initialization mode.
6	LOL_B	**PLLB Loss Of Lock Status.** Si5351A/C only. PLLB will operate in a locked state when it has a valid reference from CLKIN or XTAL. A loss of lock will occur if the frequency of the reference clock forces the PLL to operate outside of its lock range as specified in Table 4, or if the reference clock fails to meet the minimum requirements of a valid input signal as specified in Table 6. An interrupt will be triggered (INTR pin = 1, Si5351C) during a LOL condition. 0: PLL B is locked. 1: PLL B is unlocked. When the device is in this state it will trigger an interrupt causing the INTR pin to go high (Si5351C only).
5	LOL_A	**PLL A Loss Of Lock Status.** PLL A will operate in a locked state when it has a valid reference from CLKIN or XTAL. A loss of lock will occur if the frequency of the reference clock forces the PLL to operate outside of its lock range as specified in Table 4, or if the reference clock fails to meet the minimum requirements of a valid input signal as specified in Table 6. An interrupt will be triggered (INTR pin = 1, Si5351C only) during a LOL condition. 0: PLL A is operating normally. 1: PLL A is unlocked. When the device is in this state it will trigger an interrupt causing the INTR pin to go high (Si5351C only).
4	LOS	**CLKIN Loss Of Signal (Si5351C Only).** A loss of signal status indicates if the reference clock fails to meet the minimum requirements of a valid input signal as specified in Table 6. An interrupt will be triggered (INTR pin = 1, Si5351C only) during a LOS condition. 0: Valid clock signal at the CLKIN pin. 1: Loss of signal detected at the CLKIN pin.
3:2	Reserved	**Reserved.** Leave as default.
1:0	REVID[1:0]	Revision ID. Device revision number. Set at the factory.

Register 1. Device Status

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SYS_INIT_STKY	LOL_B_STKY	LOL_A_STKY	LOS_STKY				
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 0000 0000

Bit	Name	Function
7	SYS_INIT_STKY	**System Calibration Status Sticky Bit.** The SYS_INIT_STKY bit is triggered when the SYS_INIT bit (register 0, bit 7) is triggered high. It remains high until cleared. Writing a 0 to this register bit will cause it to clear. 0: No SYS_INIT interrupt has occurred since it was last cleared. 1: A SYS_INIT interrupt has occurred since it was last cleared.
6	LOL_B_STKY	**PLLB Loss Of Lock Status Sticky Bit.** The LOL_B_STKY bit is triggered when the LOL_B bit (register 0, bit 6) is triggered high. It remains high until cleared. Writing a 0 to this register bit will cause it to clear. 0: No PLL B interrupt has occurred since it was last cleared. 1: A PLL B interrupt has occurred since it was last cleared.
5	LOL_A_STKY	**PLLA Loss Of Lock Status Sticky Bit.** The LOL_A_STKY bit is triggered when the LOL_A bit (register 0, bit 5) is triggered high. It remains high until cleared. Writing a 0 to this register bit will cause it to clear. 0: No PLLA interrupt has occurred since it was last cleared. 1: A PLLA interrupt has occurred since it was last cleared.
4	LOS_STKY	**CLKIN Loss Of Signal Sticky Bit (Si5351C Only).** The LOS_STKY bit is triggered when the LOS bit (register 0, bit 4) is triggered high. It remains high until cleared. Writing a 0 to this register bit will cause it to clear. 0: No LOS interrupt has occurred since it was last cleared. 1: A LOS interrupt has occurred since it was last cleared.
3:0	Reserved	**Reserved.** Leave as default.

Register 2. Interrupt Status Mask

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SYS_INIT_MASK	LOL_B_MASK	LOL_A_MASK	LOS_MASK				
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 0000 0000

Bit	Name	Function
7	SYS_INIT_MASK	**System Initialization Status Mask.** Use this mask bit to prevent the INTR pin (Si5351C only) from going high when SYS_INIT goes high. 0: Do not mask the SYS_INIT interrupt. 1: Mask the SYS_INIT interrupt.
6	LOL_B_MASK	**PLLB Loss Of Lock Status Mask.** Use this mask bit to prevent the INTR pin (Si5351C only) from going high when LOL_B goes high. 0: Do not mask the LOL_B interrupt. 1: Mask the LOL_B interrupt.
5	LOL_A_MASK	**PLL A Loss Of Lock Status Mask.** Use this mask bit to prevent the INTR pin (Si5351C only) from going high when LOL_A goes high. 0: Do not mask the LOL_A interrupt. 1: Mask the LOL_A interrupt.
4	LOS_MASK	**CLKIN Loss Of Signal Mask (Si5351C Only).** Use this mask bit to prevent the INTR pin (Si5351C only) from going high when LOS goes high. 0: Do not mask the LOS interrupt. 1: Mask the LOS interrupt.
3:0	Reserved	**Reserved.** Leave as default.

Register 3. Output Enable Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CLK7_EN	CLK6_EN	CLK5_EN	CLK4_EN	CLK3_EN	CLK2_EN	CLK1_EN	CLK0_EN
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 0000 0000

Bit	Name	Function
7:0	CLKx_EN	**Output Enable for CLKx.** Where x = 0, 1, 2, 3, 4, 5, 6, 7 0: Enable CLKx output. 1: Disable CLKx output.

Register 9. OEB Pin Enable Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	OEB_CLK7	OEB_CLK6	OEB_CLK5	OEB_CLK4	OEB_CLK3	OEB_CLK2	OEB_CLK1	OEB_CLK0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 0000 0000

Bit	Name	Function
7:0	OEB_CLKx	**OEB pin enable control of CLKx.** Where x = 0, 1, 2, 3, 4, 5, 6, 7 0: OEB pin controls enable/disable state of CLKx output. 1: OEB pin does not control enable/disable state of CLKx output.

Register 15. PLL Input Source

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					PLLB_SRC	PLLA_SRC		
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 0000 0000

Bit	Name	Function
7:4	Reserved	**Reserved**. Leave as default.
3	PLLB_SRC	Input Source Select for PLLB. 0: Select the XTAL input as the reference clock for PLLB (Si5351A/C only). 1: Select the CLKIN input as the reference clock for PLLB (Si5351C only).
2	PLLA_SRC	Input Source Select for PLLA. 0: Select the XTAL input as the reference clock for PLLA. 1: Select the CLKIN input as the reference clock for PLLA (Si5351C only).
1:0	Reserved	**Reserved**. Leave as default.

Register 16. CLK0 Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CLK0_PDN	MS0_INT	MS0_SRC	CLK0_INV	CLK0_SRC[1:0]			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 0000 0000

Bit	Name	Function
7	CLK0_PDN	**Clock 0 Power Down.** This bit allows powering down the CLK0 output driver to conserve power when the output is unused. 0: CLK0 is powered up. 1: CLK0 is powered down.
6	MS0_INT	**MultiSynth 0 Integer Mode.** This bit can be used to force MS0 into Integer mode to improve jitter performance. Note that the fractional mode is necessary when a delay offset is specified for CLK0. 0: MS0 operates in fractional division mode. 1: MS0 operates in integer mode.
5	MS0_SRC	**MultiSynth Source Select for CLK0.** 0: Select PLLA as the source for MultiSynth0. 1: Select PLLB (Si5351A/C only) or VCXO (Si5351B only) MultiSynth0.
4	CLK0_INV	**Output Clock 0 Invert.** 0: Output Clock 0 is not inverted. 1: Output Clock 0 is inverted.
3:2	CLK0_SRC[1:0]	**Output Clock 0 Input Source.** These bits determine the input source for CLK0. 00: Select the XTAL as the clock source for CLK0. This option by-passes both synthesis stages (PLL/VCXO & MultiSynth) and connects CLK0 directly to the oscillator which generates an output frequency determined by the XTAL frequency. 01: Select CLKIN as the clock source for CLK0. This by-passes both synthesis stages (PLL/VCXO & MultiSynth) and connects CLK0 directly to the CLKIN input. This essentially creates a buffered output of the CLKIN input. 10: Reserved. Do not select this option. 11: Select MultiSynth 0 as the source for CLK0. Select this option when using the Si5351 to generate free-running or synchronous clocks.
1:0	Reserved	**Reserved.** Leave as default.

Register 17. CLK1 Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CLK1_PDN	MS1_INT	MS1_SRC	CLK1_INV	CLK1_SRC[1:0]			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 0000 0000

Bit	Name	Function
7	CLK1_PDN	**Clock 0 Power Down.** This bit allows powering down the CLK1 output driver to conserve power when the output is unused. 0: CLK1 is powered up. 1: CLK1 is powered down.
6	MS0_INT	**MultiSynth 0 Integer Mode.** This bit can be used to force MS0 into Integer mode to improve jitter performance. Note that the fractional mode is necessary when a delay offset is specified for CLK1. 0: MS0 operates in fractional division mode. 1: MS0 operates in integer mode.
5	MS0_SRC	**MultiSynth Source Select for CLK1.** 0: Select PLLA as the source for MultiSynth0. 1: Select PLLB (Si5351A/C only) or VCXO (Si5351B only) MultiSynth0.
4	CLK1_INV	**Output Clock 0 Invert.** 0: Output Clock 0 is not inverted. 1: Output Clock 0 is inverted.
3:2	CLK1_SRC[1:0]	**Output Clock 0 Input Source.** These bits determine the input source for CLK1. 00: Select the XTAL as the clock source for CLK1. This option by-passes both synthesis stages (PLL/VCXO & MultiSynth) and connects CLK1 directly to the oscillator which generates an output frequency determined by the XTAL frequency. 01: Select CLKIN as the clock source for CLK1. This by-passes both synthesis stages (PLL/VCXO & MultiSynth) and connects CLK1 directly to the CLKIN input. This essentially creates a buffered output of the CLKIN input. 10: Reserved. Do not select this option. 11: Select MultiSynth 0 as the source for CLK1. Select this option when using the Si5351 to generate free-running or synchronous clocks.
1:0	Reserved	**Reserved.** Leave as default.

Register 18. CLK2 Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CLK2_PDN	MS2_INT	MS2_SRC	CLK2_INV	CLK2_SRC[1:0]			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 0000 0000

Bit	Name	Function
7	CLK2_PDN	**Clock 0 Power Down.** This bit allows powering down the CLK2 output driver to conserve power when the output is unused. 0: CLK2 is powered up. 1: CLK2 is powered down.
6	MS0_INT	**MultiSynth 0 Integer Mode.** This bit can be used to force MS0 into Integer mode to improve jitter performance. Note that the fractional mode is necessary when a delay offset is specified for CLK2. 0: MS0 operates in fractional division mode. 1: MS0 operates in integer mode.
5	MS0_SRC	**MultiSynth Source Select for CLK2.** 0: Select PLLA as the source for MultiSynth0. 1: Select PLLB (Si5351A/C only) or VCXO (Si5351B only) MultiSynth0.
4	CLK2_INV	**Output Clock 0 Invert.** 0: Output Clock 0 is not inverted. 1: Output Clock 0 is inverted.
3:2	CLK2_SRC[1:0]	**Output Clock 0 Input Source.** These bits determine the input source for CLK2. 00: Select the XTAL as the clock source for CLK2. This option by-passes both synthesis stages (PLL/VCXO & MultiSynth) and connects CLK2 directly to the oscillator which generates an output frequency determined by the XTAL frequency. 01: Select CLKIN as the clock source for CLK2. This by-passes both synthesis stages (PLL/VCXO & MultiSynth) and connects CLK2 directly to the CLKIN input. This essentially creates a buffered output of the CLKIN input. 10: Reserved. Do not select this option. 11: Select MultiSynth 0 as the source for CLK2. Select this option when using the Si5351 to generate free-running or synchronous clocks.
1:0	Reserved	**Reserved.** Leave as default.

Register 19. CLK3 Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CLK3_PDN	MS3_INT	MS3_SRC	CLK3_INV	CLK3_SRC[1:0]			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 0000 0000

Bit	Name	Function
7	CLK3_PDN	**Clock 0 Power Down.** This bit allows powering down the CLK3 output driver to conserve power when the output is unused. 0: CLK3 is powered up. 1: CLK3 is powered down.
6	MS0_INT	**MultiSynth 0 Integer Mode.** This bit can be used to force MS0 into Integer mode to improve jitter performance. Note that the fractional mode is necessary when a delay offset is specified for CLK3. 0: MS0 operates in fractional division mode. 1: MS0 operates in integer mode.
5	MS0_SRC	**MultiSynth Source Select for CLK3.** 0: Select PLLA as the source for MultiSynth0. 1: Select PLLB (Si5351A/C only) or VCXO (Si5351B only) MultiSynth0.
4	CLK3_INV	**Output Clock 0 Invert.** 0: Output Clock 0 is not inverted. 1: Output Clock 0 is inverted.
3:2	CLK3_SRC[1:0]	**Output Clock 0 Input Source.** These bits determine the input source for CLK3.
1:0	Reserved	**Reserved.** Leave as default.

Register 20. CLK4 Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CLK4_PDN	MS4_INT	MS4_SRC	CLK4_INV	CLK4_SRC[1:0]			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 0000 0000

Bit	Name	Function
7	CLK4_PDN	**Clock 0 Power Down.** This bit allows powering down the CLK4 output driver to conserve power when the output is unused. 0: CLK4 is powered up. 1: CLK4 is powered down.
6	MS0_INT	**MultiSynth 0 Integer Mode.** This bit can be used to force MS0 into Integer mode to improve jitter performance. Note that the fractional mode is necessary when a delay offset is specified for CLK4. 0: MS0 operates in fractional division mode. 1: MS0 operates in integer mode.
5	MS0_SRC	**MultiSynth Source Select for CLK4.** 0: Select PLLA as the source for MultiSynth0. 1: Select PLLB (Si5351A/C only) or VCXO (Si5351B only) MultiSynth0.
4	CLK4_INV	**Output Clock 0 Invert.** 0: Output Clock 0 is not inverted. 1: Output Clock 0 is inverted.
3:2	CLK4_SRC[1:0]	**Output Clock 0 Input Source.** These bits determine the input source for CLK4. 00: Select the XTAL as the clock source for CLK4. This option by-passes both synthesis stages (PLL/VCXO & MultiSynth) and connects CLK4 directly to the oscillator which generates an output frequency determined by the XTAL frequency. 01: Select CLKIN as the clock source for CLK4. This by-passes both synthesis stages (PLL/VCXO & MultiSynth) and connects CLK4 directly to the CLKIN input. This essentially creates a buffered output of the CLKIN input. 10: Reserved. Do not select this option. 11: Select MultiSynth 0 as the source for CLK4. Select this option when using the Si5351 to generate free-running or synchronous clocks.
1:0	Reserved	**Reserved.** Leave as default.

Register 21. CLK5 Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CLK5_PDN	MS5_INT	MS5_SRC	CLK5_INV	CLK5_SRC[1:0]			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 0000 0000

Bit	Name	Function
7	CLK5_PDN	**Clock 0 Power Down.** This bit allows powering down the CLK5 output driver to conserve power when the output is unused. 0: CLK4 is powered up. 1: CLK4 is powered down.
6	MS0_INT	**MultiSynth 0 Integer Mode.** This bit can be used to force MS0 into Integer mode to improve jitter performance. Note that the fractional mode is necessary when a delay offset is specified for CLK4. 0: MS0 operates in fractional division mode. 1: MS0 operates in integer mode.
5	MS0_SRC	**MultiSynth Source Select for CLK5.** 0: Select PLLA as the source for MultiSynth0. 1: Select PLLB (Si5351A/C only) or VCXO (Si5351B only) MultiSynth0.
4	CLK5_INV	**Output Clock 0 Invert.** 0: Output Clock 0 is not inverted. 1: Output Clock 0 is inverted.
3:2	CLK5_SRC[1:0]	**Output Clock 0 Input Source.** These bits determine the input source for CLK5. 00: Select the XTAL as the clock source for CLK5. This option by-passes both synthesis stages (PLL/VCXO & MultiSynth) and connects CLK5 directly to the oscillator which generates an output frequency determined by the XTAL frequency. 01: Select CLKIN as the clock source for CLK5. This by-passes both synthesis stages (PLL/VCXO & MultiSynth) and connects CLK5 directly to the CLKIN input. This essentially creates a buffered output of the CLKIN input. 10: Reserved. Do not select this option. 11: Select MultiSynth 0 as the source for CLK5. Select this option when using the Si5351 to generate free-running or synchronous clocks.
1:0	Reserved	**Reserved.** Leave as default.

Register 22. CLK6 Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CLK6_PDN	MS6_INT	MS6_SRC	CLK6_INV	CLK6_SRC[1:0]			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 0000 0000

Bit	Name	Function
7	CLK6_PDN	**Clock 0 Power Down.** This bit allows powering down the CLK6 output driver to conserve power when the output is unused. 0: CLK6 is powered up. 1: CLK6 is powered down.
6	MS0_INT	**MultiSynth 0 Integer Mode.** This bit can be used to force MS0 into Integer mode to improve jitter performance. Note that the fractional mode is necessary when a delay offset is specified for CLK6. 0: MS0 operates in fractional division mode. 1: MS0 operates in integer mode.
5	MS0_SRC	**MultiSynth Source Select for CLK6.** 0: Select PLLA as the source for MultiSynth0. 1: Select PLLB (Si5351A/C only) or VCXO (Si5351B only) MultiSynth0.
4	CLK6_INV	**Output Clock 0 Invert.** 0: Output Clock 0 is not inverted. 1: Output Clock 0 is inverted.
3:2	CLK6_SRC[1:0]	**Output Clock 0 Input Source.** These bits determine the input source for CLK6. 00: Select the XTAL as the clock source for CLK6. This option by-passes both synthesis stages (PLL/VCXO & MultiSynth) and connects CLK6 directly to the oscillator which generates an output frequency determined by the XTAL frequency. 01: Select CLKIN as the clock source for CLK6. This by-passes both synthesis stages (PLL/VCXO & MultiSynth) and connects CLK6 directly to the CLKIN input. This essentially creates a buffered output of the CLKIN input. 10: Reserved. Do not select this option. 11: Select MultiSynth 0 as the source for CLK6. Select this option when using the Si5351 to generate free-running or synchronous clocks.
1:0	Reserved	**Reserved.** Leave as default.

Register 23. CLK7 Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CLK7_PDN	MS7_INT	MS7_SRC	CLK7_INV	CLK7_SRC[1:0]			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 0000 0000

Bit	Name	Function
7	CLK7_PDN	**Clock 0 Power Down.** This bit allows powering down the CLK7 output driver to conserve power when the output is unused. 0: CLK7 is powered up. 1: CLK7 is powered down.
6	MS0_INT	**MultiSynth 0 Integer Mode.** This bit can be used to force MS0 into Integer mode to improve jitter performance. Note that the fractional mode is necessary when a delay offset is specified for CLK7. 0: MS0 operates in fractional division mode. 1: MS0 operates in integer mode.
5	MS0_SRC	**MultiSynth Source Select for CLK7.** 0: Select PLLA as the source for MultiSynth0. 1: Select PLLB (Si5351A/C only) or VCXO (Si5351B only) MultiSynth0.
4	CLK7_INV	**Output Clock 0 Invert.** 0: Output Clock 0 is not inverted. 1: Output Clock 0 is inverted.
3:2	CLK7_SRC[1:0]	**Output Clock 0 Input Source.** These bits determine the input source for CLK7. 00: Select the XTAL as the clock source for CLK7. This option by-passes both synthesis stages (PLL/VCXO & MultiSynth) and connects CLK7 directly to the oscillator which generates an output frequency determined by the XTAL frequency. 01: Select CLKIN as the clock source for CLK7. This by-passes both synthesis stages (PLL/VCXO & MultiSynth) and connects CLK7 directly to the CLKIN input. This essentially creates a buffered output of the CLKIN input. 10: Reserved. Do not select this option. 11: Select MultiSynth 0 as the source for CLK7. Select this option when using the Si5351 to generate free-running or synchronous clocks.
1:0	Reserved	**Reserved.** Leave as default.

Register 24. CLK3–0 Disable State

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CLK3_DIS_STATE		CLK2_DIS_STATE		CLK1_DIS_STATE		CLK0_DIS_STATE	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 0000 0000

Bit	Name	Function
7:0	CLKx_DIS_STATE	**Clock x Disable State.** Where x = 0, 1, 2, 3. These 2 bits determine the state of the CLKx output when disabled. Individual output clocks can be disabled using register *Output Enable Control* located at address 3. Outputs are also disabled using the OEB pin. 00: CLKx is set to a LOW state when disabled. 01: CLKx is set to a HIGH state when disabled. 10: CLKx is set to a HIGH IMPEDANCE state when disabled. 11: CLKx is NEVER DISABLED.

Register 25. CLK7–4 Disable State

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CLK7_DIS_STATE		CLK6_DIS_STATE		CLK5_DIS_STATE		CLK4_DIS_STATE	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 0000 0000

Bit	Name	Function
7:0	CLKx_DIS_STATE	**Clock x Disable State.** Where x = 4, 5, 6, 7. These 2 bits determine the state of the CLKx output when disabled. Individual output clocks can be disabled using register *Output Enable Control* located at address 3. Outputs are also disabled using the OEB pin. 00: CLKx is set to a LOW state when disabled. 01: CLKx is set to a HIGH state when disabled. 10: CLKx is set to a HIGH IMPEDANCE state when disabled. 11: CLKx is NEVER DISABLED.

Register 177. PLL Reset

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PLLB_RST		PLLA_RST					
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 0000 0000

Bit	Name	Function
7	PLLB_RST	**PLLB_Reset.** Writing a 1 to this bit will reset PLLB. This is a self clearing bit (Si5351A/C only).
6	Reserved	**Reserved.** Leave as default.
5	PLLA_RST	**PLLA_Reset.** Writing a 1 to this bit will reset PLLA. This is a self clearing bit.
4:0	Reserved	**Reserved.** Leave as default.

Register 183. Crystal Internal Load Capacitance

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	XTAL_CL[1:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 11xx xxxx

Bit	Name	Function
7:6	XTAL_CL[1:0]	**Crystal Load Capacitance Selection.** These 2 bits determine the internal load capacitance value for the crystal. See "2.1.1. Crystal Inputs (XA, XB)" on page 8. 00: Reserved. Do not select this option. 01: Internal CL = 6 pF. 10: Internal CL = 8 pF. 11: Internal CL = 10 pF (default).
5:0	Reserved	**Reserved.** Leave as default.

9. Detailed Block Diagrams

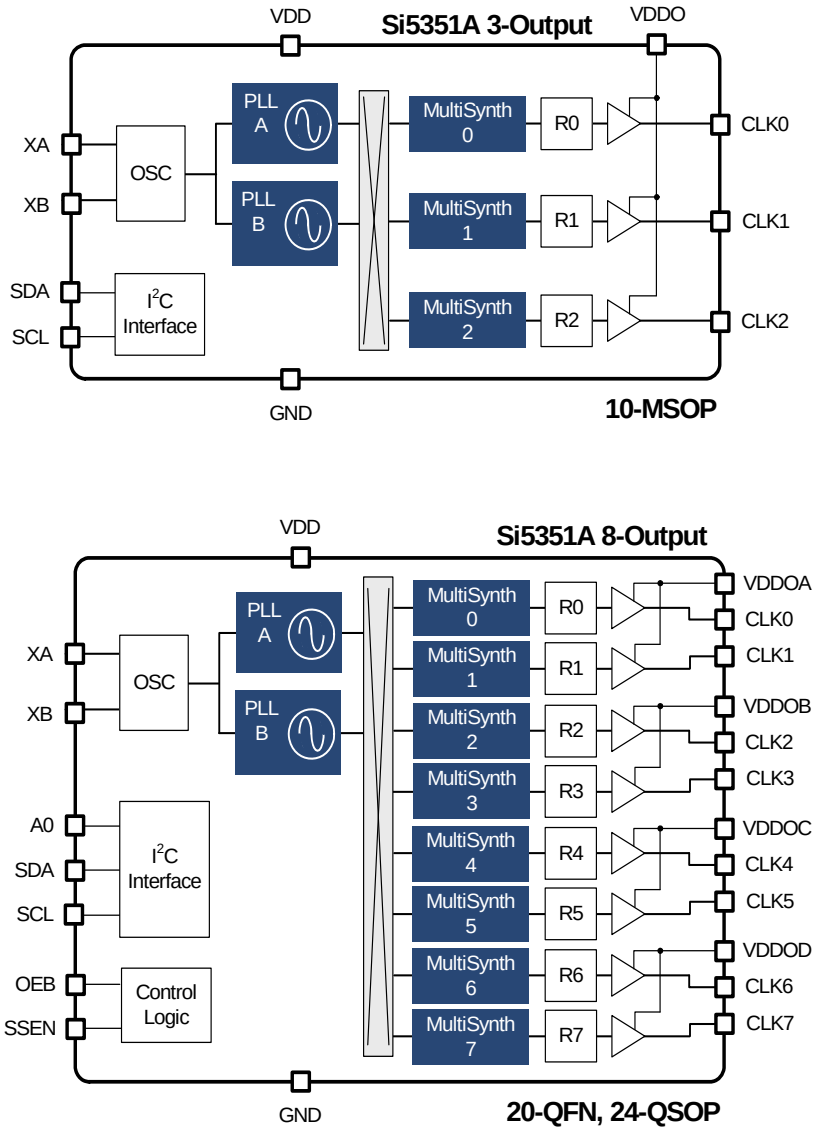


Figure 14. Block Diagrams of 3-Output and 8-Output Si5351A Devices

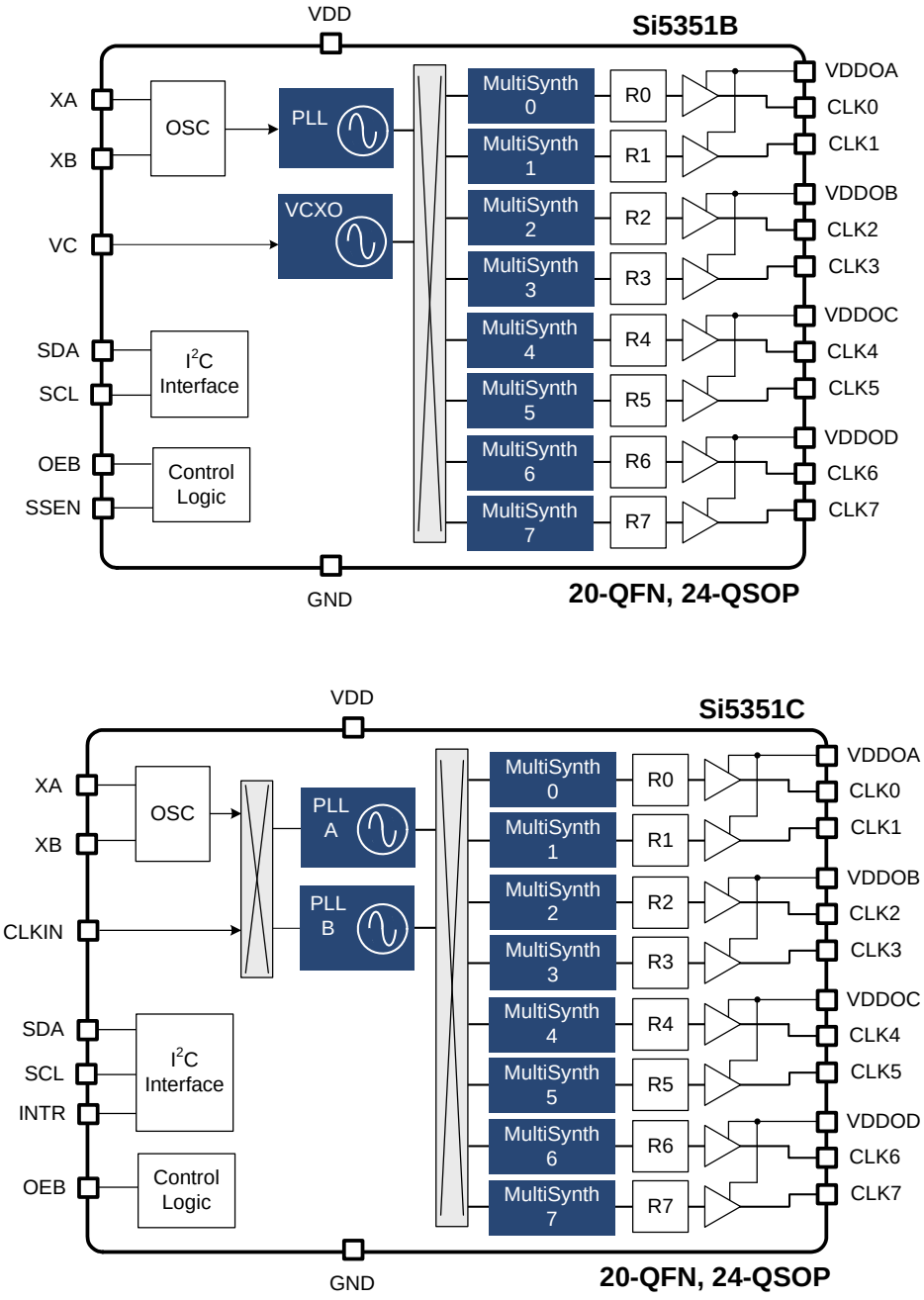
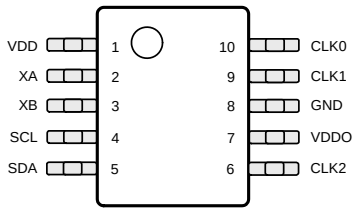


Figure 15. Block Diagrams of Si5351B and Si5351C 8-Output Devices

10. Pin Descriptions (10-Pin MSOP)

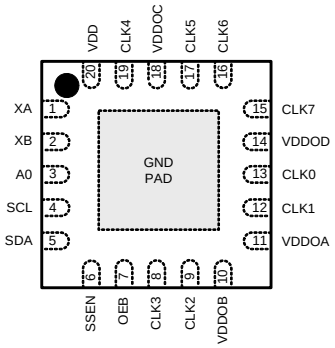
Si5351A 10-MSOP
Top View



Pin Name	Pin Number	Pin Type*	Function
	10-MSOP		
XA	2	I	Input pin for external crystal.
XB	3	I	Input pin for external crystal.
CLK0	10	O	Output clock 0.
CLK1	9	O	Output clock 1.
CLK2	6	O	Output clock 2.
SCL	4	I	Serial clock input for the I^2C bus. This pin must be pulled-up using a pull-up resistor of at least 1 kΩ.
SDA	5	I/O	Serial data input for the I^2C bus. This pin must be pulled-up using a pull-up resistor of at least 1 kΩ.
VDD	1	P	Core voltage supply pin.
VDDO	7	P	Output voltage supply pin for CLK0, CLK1, and CLK2. See "6.2. Power Supply Sequencing" on page 15.
GND	8	P	Ground.
***Note:** I = Input, O = Output, P = Power			

11. Si5351A Pin Descriptions (20-Pin QFN, 24-Pin QSOP)

Si5351A 20-QFN
Top View



Si5351A 24-QSOP
Top View

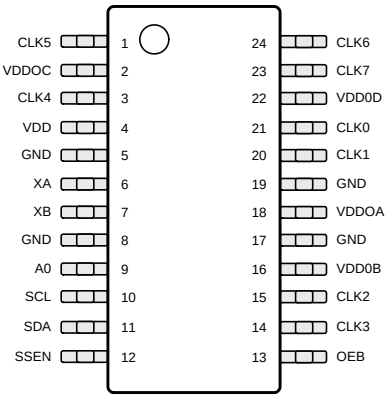


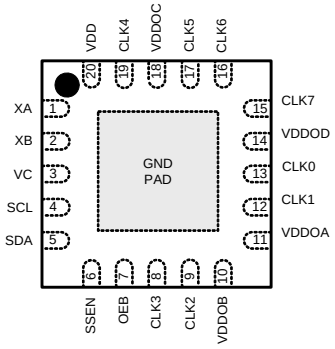
Table 10:

Pin Name	Pin Number		Pin Type*	Function
	20-QFN	24-QSOP		
XA	1	6	I	Input pin for external crystal.
XB	2	7	I	Input pin for external crystal.
CLK0	13	21	O	Output clock 0.
CLK1	12	20	O	Output clock 1.
CLK2	9	15	O	Output clock 2.
CLK3	8	14	O	Output clock 3.
CLK4	19	3	O	Output clock 4.
CLK5	17	1	O	Output clock 5.
CLK6	16	24	O	Output clock 6.
CLK7	15	23	O	Output clock 7.
A0	3	9	I	I^2C address bit.
SCL	4	10	I	I^2C bus serial clock input. Pull-up to VDD core with 1 kΩ.
SDA	5	11	I/O	I^2C bus serial data input. Pull-up to VDD core with 1 kΩ.
SSEN	6	12	I	Spread spectrum enable. High = enabled, Low = disabled.
OEB	7	13	I	Output driver enable. Low = enabled, High = disabled.
VDD	20	4	P	Core voltage supply pin. See 6.2.
VDDOA	11	18	P	Output voltage supply pin for CLK0 and CLK1. See 6.2.
VDDOB	10	16	P	Output voltage supply pin for CLK2 and CLK3. See 6.2.
VDDOC	18	2	P	Output voltage supply pin for CLK4 and CLK5. See 6.2.
VDDOD	14	22	P	Output voltage supply pin for CLK6 and CLK7. See 6.2.
GND	Center Pad	5, 8, 17, 19	P	Ground. Use multiple vias to ensure a solid path to GND.

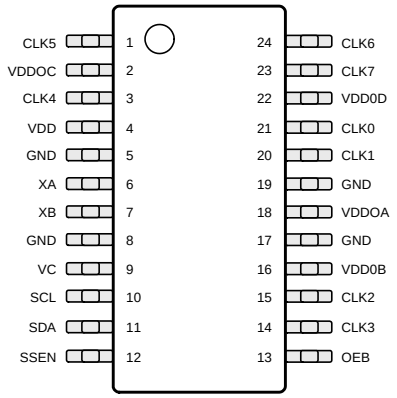
1. I = Input, O = Output, P = Power.
2. Input pins are not internally pulled up.

12. Si5351B Pin Descriptions (20-Pin QFN, 24-Pin QSOP)

Si5351B 20-QFN
Top View



Si5351B 24-QSOP
Top View

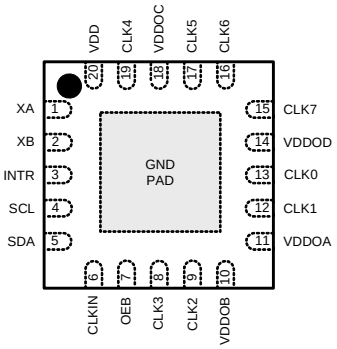


Pin Name	Pin Number		Pin Type*	Function
	20-QFN	24-QSOP		
XA	1	6	I	Input pin for external crystal
XB	2	7	I	Input pin for external crystal
CLK0	13	21	O	Output clock 0
CLK1	12	20	O	Output clock 1
CLK2	9	15	O	Output clock 2
CLK3	8	14	O	Output clock 3
CLK4	19	3	O	Output clock 4
CLK5	17	1	O	Output clock 5
CLK6	16	24	O	Output clock 6
CLK7	15	23	O	Output clock 7
VC	3	9	I	VCXO control voltage input
SCL	4	10	I	I^2C bus serial clock input. Pull-up to VDD core with 1 kΩ.
SDA	5	11	I/O	I^2C bus serial data input. Pull-up to VDD core with 1 kΩ.
SSEN	6	12	I	Spread spectrum enable. High = enabled, Low = disabled.
OEB	7	13	I	Output driver enable. Low = enabled, High = disabled.
VDD	20	4	P	Core voltage supply pin
VDDOA	11	18	P	Output voltage supply pin for CLK0 and CLK1. See 6.2
VDDOB	10	16	P	Output voltage supply pin for CLK2 and CLK3. See 6.2
VDDOC	18	2	P	Output voltage supply pin for CLK4 and CLK5. See 6.2
VDDOD	14	22	P	Output voltage supply pin for CLK6 and CLK7. See 6.2
GND	Center Pad	5, 8, 17, 19	P	Ground

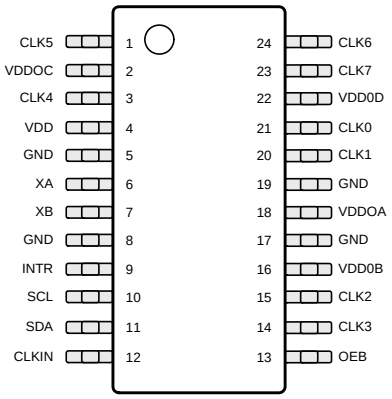
***Note:** I = Input, O = Output, P = Power
***Note:** Input pins are not internally pulled up.

13. Si5351C Pin Descriptions (20-Pin QFN, 24-Pin QSOP)

Si5351C 20-QFN
Top View



Si5351C 20-QSOP
Top View



Pin Name	Pin Number		Pin Type*	Function
	20-QFN	24-QSOP		
XA	1	6	I	Input pin for external crystal.
XB	2	7	I	Input pin for external crystal.
CLK0	13	21	O	Output clock 0.
CLK1	12	20	O	Output clock 1.
CLK2	9	15	O	Output clock 2.
CLK3	8	14	O	Output clock 3.
CLK4	19	3	O	Output clock 4.
CLK5	17	1	O	Output clock 5.
CLK6	16	24	O	Output clock 6.
CLK7	15	23	O	Output clock 7.
INTR	3	9	O	Interrupt pin. High = interrupt active.
SCL	4	10	I	I^2C bus serial clock input. Pull-up to VDD core with 1 kΩ.
SDA	5	11	I/O	I^2C bus serial data input. Pull-up to VDD core with 1 kΩ.
CLKIN	6	12	I	PLL clock input.
OEB	7	13	I	Output driver enable. Low = enabled, High = disabled.
VDD	20	4	P	Core voltage supply pin
VDDOA	11	18	P	Output voltage supply pin for CLK0 and CLK1. See 6.2
VDDOB	10	16	P	Output voltage supply pin for CLK2 and CLK3. See 6.2
VDDOC	18	2	P	Output voltage supply pin for CLK4 and CLK5. See 6.2
VDDOD	14	22	P	Output voltage supply pin for CLK6 and CLK7. See 6.2
GND	Center Pad	5, 8, 17, 19	P	Ground.

***Note:** I = Input, O = Output, P = Power
***Note:** Input pins are not internally pulled up

14. Package Outline (24-Pin QSOP)

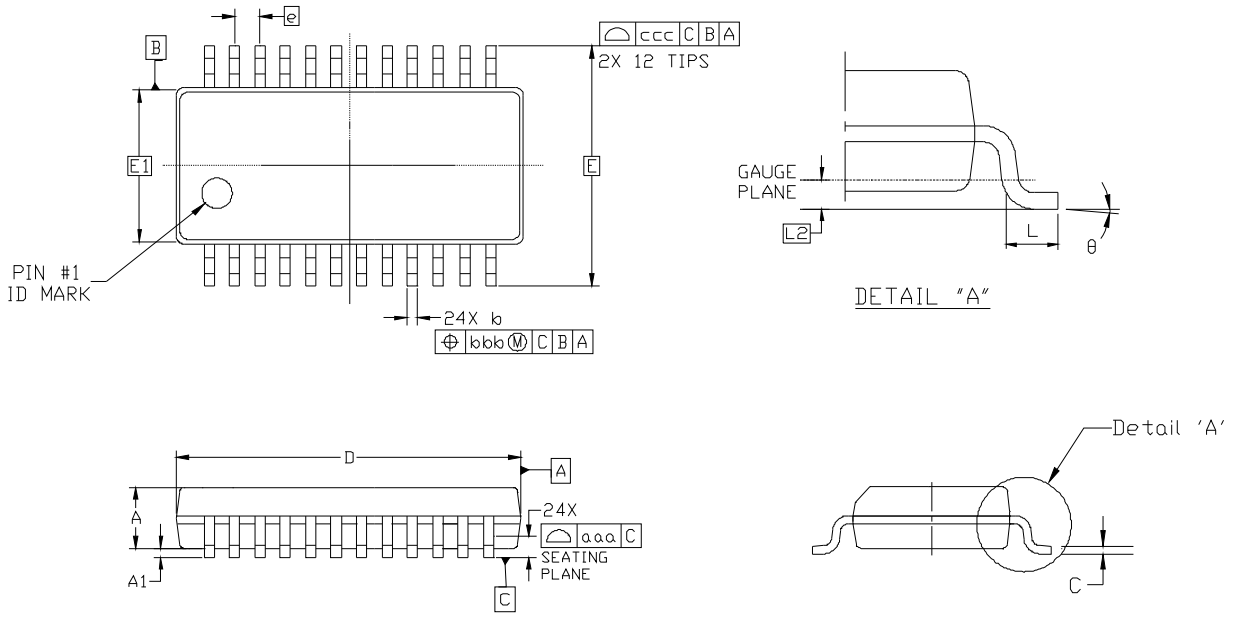


Table 11. 24-QSOP Package Dimensions

Dimension	Min	Nom	Max
A	—	—	1.75
A1	0.10	—	0.25
b	0.19	—	0.30
c	0.15	—	0.25
D	8.55	8.65	8.75
E		6.00 BSC	
E1	3.81	3.90	3.99
e		0.635 BSC	
L	0.40	—	1.27
L2		0.25 BSC	
q	0	—	8
aaa		0.10	
bbb		0.17	
ccc		0.10	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-137, Variation C
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

15. Package Outline (20-Pin QFN)

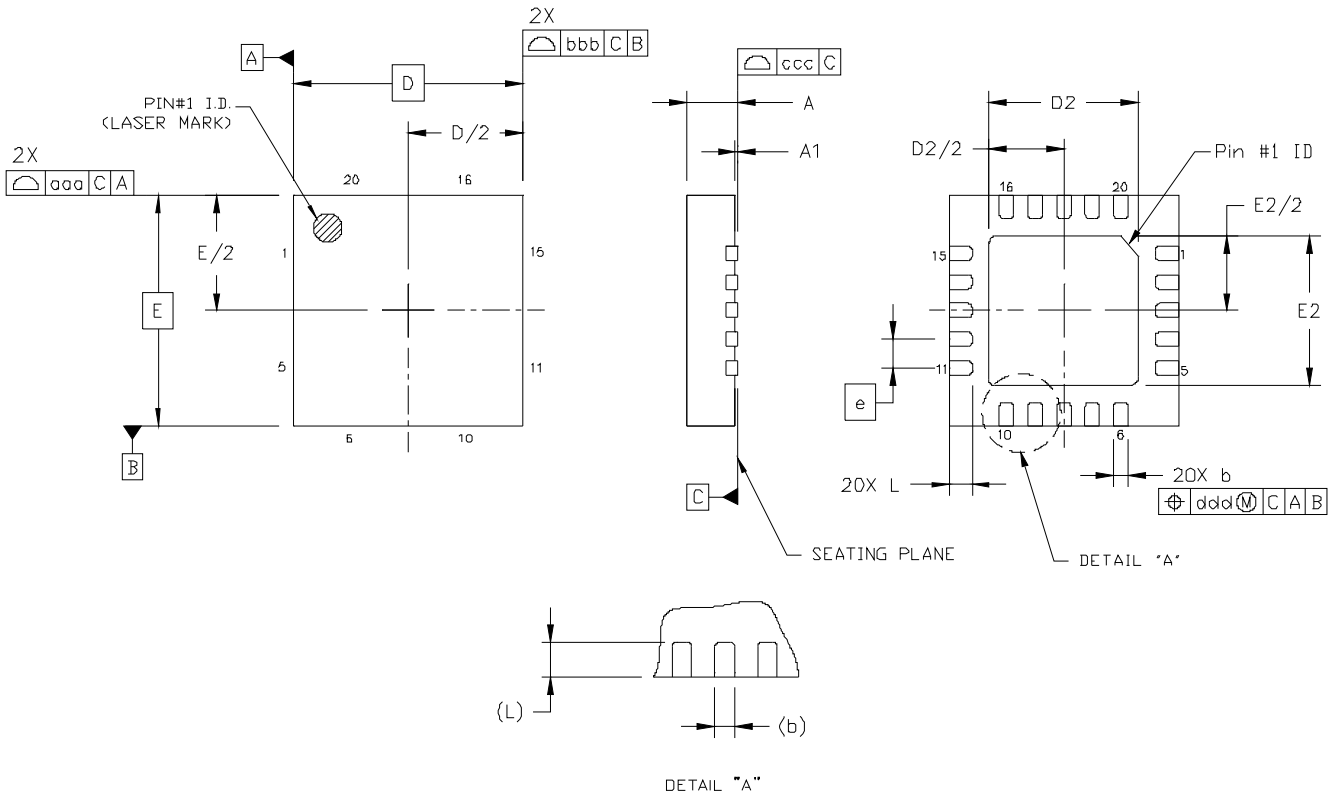


Table 12. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		4.00 BSC	
D2	2.65	2.70	2.75
e		0.50 BSC	
E		4.00 BSC	
E2	2.65	2.70	2.75
L	0.30	0.40	0.50
aaa			0.10
bbb			0.10
ccc			0.08
ddd			0.10
eee			0.10

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Outline MO-220, variation VGGD-8.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

16. Package Outline (10-Pin MSOP)

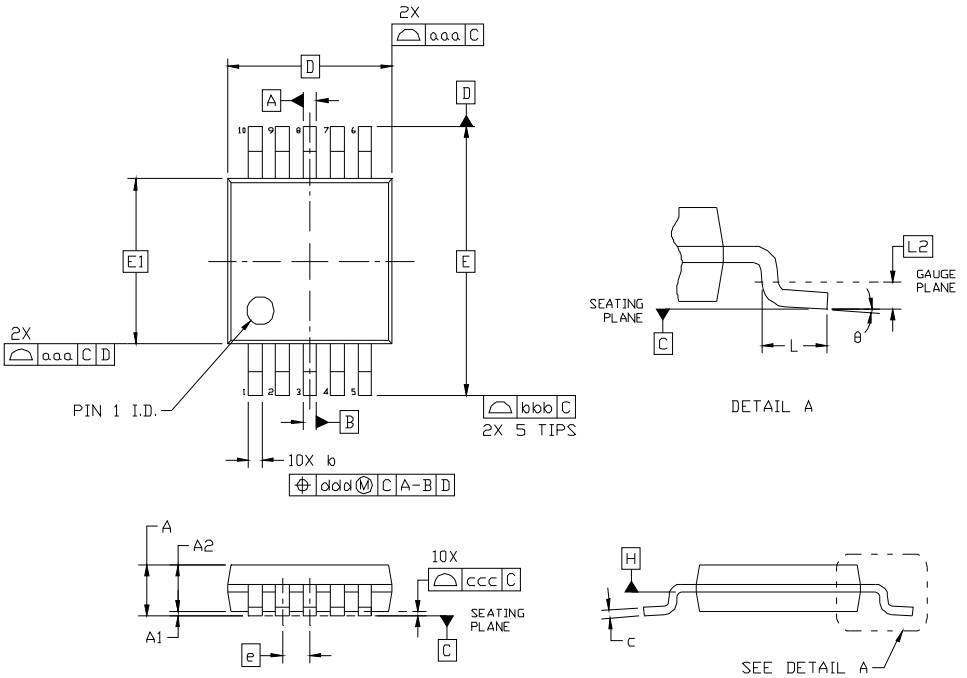


Table 13. 24-QSOP Package Dimensions

Dimension	Min	Nom	Max
A	—	—	1.10
A1	0.00	—	0.15
A2	0.75	0.85	0.95
b	0.17	—	0.33
c	0.08	—	0.23
D	3.00 BSC		
E	4.90 BSC		
E1	3.00 BSC		
e	0.50 BSC		
L	0.40	0.60	0.80
L2	0.25 BSC		
q	0	—	8
aaa	—	—	0.20
bbb	—	—	0.25
ccc	—	—	0.10
ddd	—	—	0.08

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-137, Variation C
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

17. Ordering Information

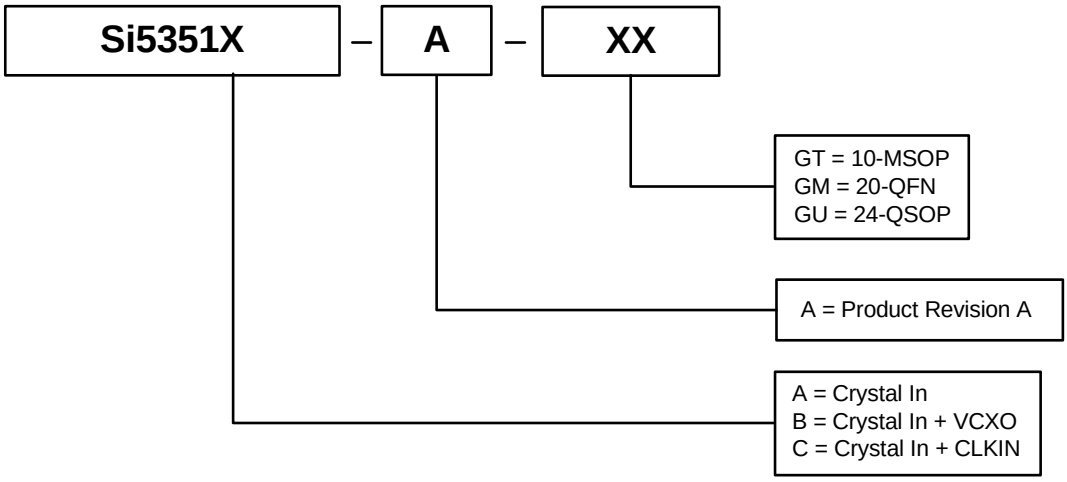


Figure 16. Device Part Numbers

A development kit containing ClockBuilder Desktop software and hardware enable easy field programming of blank Si5351 devices for instances when rapid prototyping is required. Note that the Si5351 must be field-programmed using the development kit. In addition to field programming, this development kit supports simplified device evaluation of any Si5351 device. The orderable part numbers for the development kits are provided in Figure 17.

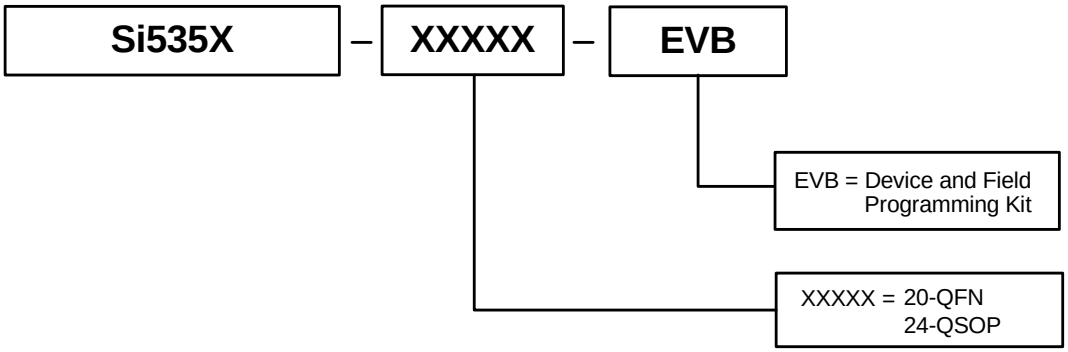


Figure 17. Development Kit Part Numbers

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