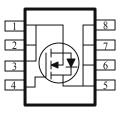
N-Channel 30-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low r_{DS(on)} provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SOIC-8 saves board space
- Fast switching speed
- High performance trench technology

PRODUCT SUMMARY			
V _{DS} (V)	$r_{\mathrm{DS(on)}} m(\Omega)$	I _D (A)	
30	$13.5 @ V_{GS} = 10V$	13	
	$20 @ V_{GS} = 4.5V$	11	





ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	Limit	Units	
Drain-Source Voltage		V _{DS}	30	V	
Gate-Source Voltage		V _{GS}	±20	v	
	$T_A=25^{\circ}C$	т	±13		
Continuous Drain Current ^a	$T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$	ID	±11	А	
Pulsed Drain Current ^b		I _{DM}	±50		
Continuous Source Current (Diode Conduction) ^a		Is	2.3	А	
	T _A =25°C	D	3.1	W	
Power Dissipation ^a	$T_{A} = 25^{\circ}C$ $T_{A} = 70^{\circ}C$	PD	2.2	vv	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150	°C	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Maximum	Units	
Maximum Junction-to-Case ^a	t <= 5 sec	$R_{\theta JC}$	25	°C/W	
Maximum Junction-to-Ambient ^a	t <= 5 sec	$R_{\theta JA}$	50	°C/W	

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature

SPECIFICATIONS (T _A = 25°C UNLESS OTHERWISE NOTED)							
Davianistan		Limits			TT4		
Parameter	Symbol	Symbol Test Conditions		Тур	Max	Unit	
Static							
Gate-Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \text{ uA}$	1			V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = 20 V$			±100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 24 V, V_{GS} = 0 V$ $V_{DS} = 24 V, V_{GS} = 0 V, T_J = 55^{\circ}C$			1 25	uA	
On-State Drain Current ^A	I _{D(on)}	$V_{DS} = 5 V, V_{GS} = 10 V$	20			А	
Drain-Source On-Resistance ^A	r _{DS(on)}	$V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$ $V_{GS} = 4.5 \text{ V}, I_D = 8 \text{ A}$			13.5 20	mΩ	
Forward Tranconductance ^A	g _{fs}	$V_{DS} = 15 \text{ V}, I_D = 10 \text{ A}$		40		S	
Diode Forward Voltage	V _{SD}	$I_{\rm S} = 2.3$ A, $V_{\rm GS} = 0$ V		0.7		V	
Dynamic ^b							
Total Gate Charge	Qg	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V},$ $I_D = 10 \text{ A}$		12.5		nC	
Gate-Source Charge	Q _{gs}			2.6			
Gate-Drain Charge	Q _{gd}			4.6			
Input Capacitance	C _{iss}	$V_{DS} = 15 V, V_{GS} = 0 V,$ f = 1MHz		1191		pF	
Output Capacitance	C _{oss}			412			
Reverse Transfer Capacitance	C _{rss}			160			
Turn-On Delay Time	t _{d(on)}	$V_{DD} = 25 \text{ V}, \text{ R}_{L} = 25 \Omega$, $\text{Id} = 1 \text{ A},$ $V_{GEN} = 10 \text{ V}$		20		nS	
Rise Time	t _r			9			
Turn-Off Delay Time	t _{d(off)}			70			
Fall-Time	t _f			20			

Notes

a. Pulse test: $PW \le 300$ us duty cycle $\le 2\%$.

b. Guaranteed by design, not subject to production testing.

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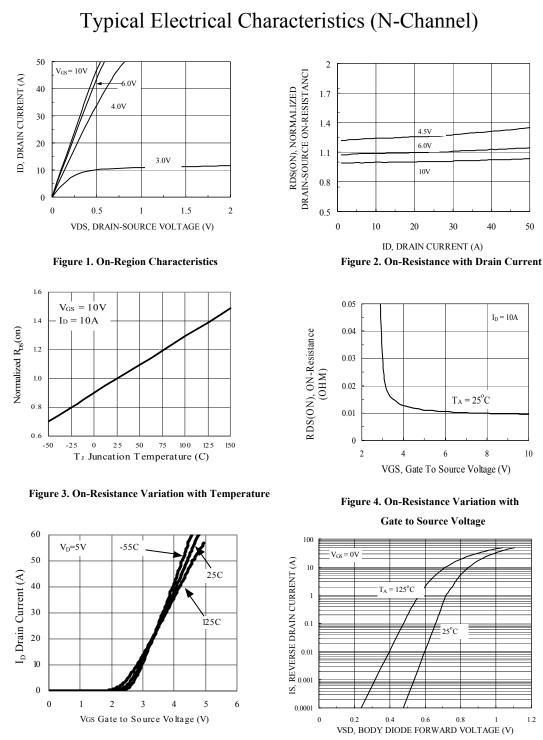
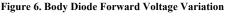


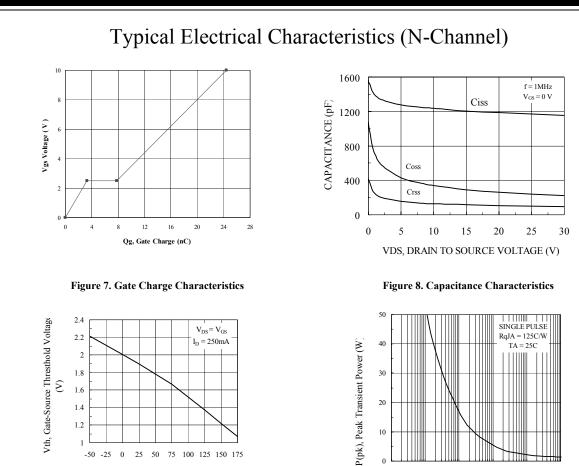
Figure 5. Transfer Characteristics

Figure 4. On-Resistance Variation with



with Source Current and Temperature

1.2



TA, AMBIENT TEMPERATURE (°C)

Figure 9. Threshold Vs Ambient Temperature



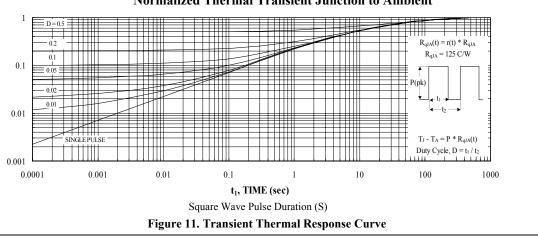
0.1

1

t1, TIME (sec)

10

100



Normalized Thermal Transient Junction to Ambient

0.001

0.01

