

**SANYO**

No. ※ 5090A

**LC378100PP, PM-10/LC378100PP, PM-20LV****8 MEG (1048576 words × 8 bits) Mask ROM  
Internal Clocked Silicon Gate****Preliminary****Overview**

The LC378100PP, PM-10 and LC378100PP, PM-20LV are 8388608-bit Mask Programmable Read Only Memories organized as 1048576 words by 8 bits.

The LC378100PP, PM-10 has a fast access time of 100 ns ( $t_{AA}$ ) and 40 ns ( $t_{OA}$ ) and a low standby power dissipation of 30  $\mu$ A under 5 V supply voltage. So, it is suitable for the fast 5 V operating systems.

The LC378100PP, PM-20LV has an access time of 200 ns ( $t_{AA}$ ) and 80 ns ( $t_{OA}$ ) and low standby power dissipation of 5  $\mu$ A under 3 V supply voltage. So, it is suitable for the low power systems such as battery used ones. Moreover, the LC378100PP, PM-20LV offers a fast access time of 150 ns ( $t_{AA}$ ) and 60 ns ( $t_{OA}$ ) under 3.3 V (3.0 to 3.6 V) supply voltage.

Pin configurations are the JEDEC standard type so as to achieve the easy exchange for EPROMs.

Pin 24 is mask programmable and it is possible to select either active HIGH or LOW in order to eliminate bus contention in multiple-bus microprocessor systems.

**Features**

- 1048576 words × 8 bits organization
- Power supply
 

LC378100PP, PM-10:	5.0 V $\pm$ 10%
LC378100PP, PM-20LV:	2.7 to 3.6 V
- Fast access time ( $t_{AA}$ ,  $t_{CA}$ )
 

LC378100PP, PM-10:	100 ns (max.)
LC378100PP, PM-20LV:	200 ns (max.)
	150 ns
	( $V_{CC}$ = 3.0 to 3.6 V)
- Operating current
 

LC378100PP, PM-10:	70 mA (max.)
LC378100PP, PM-20LV:	20 mA (max.)
- Standby current
 

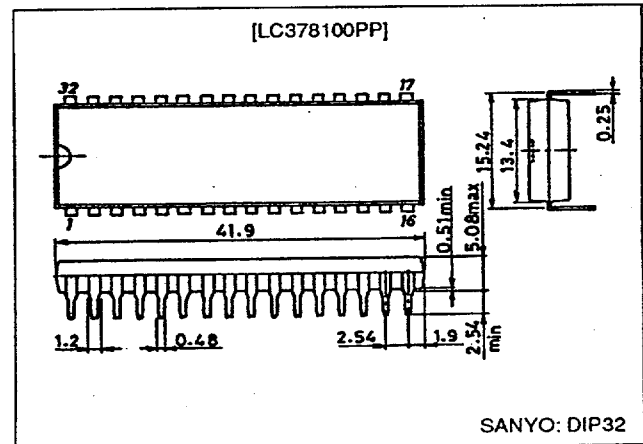
LC378100PP, PM-10:	30 $\mu$ A (max.)
LC378100PP, PM-20LV:	5 $\mu$ A (max.)
- Full static operation (internal clocked type)
- 3 state outputs
- JEDEC standard pin configuration
- Package type
 

LC378100PP-10/20LV:	DIP32 (600 mil)
LC378100PM-10/20LV:	SOP32 (525 mil)

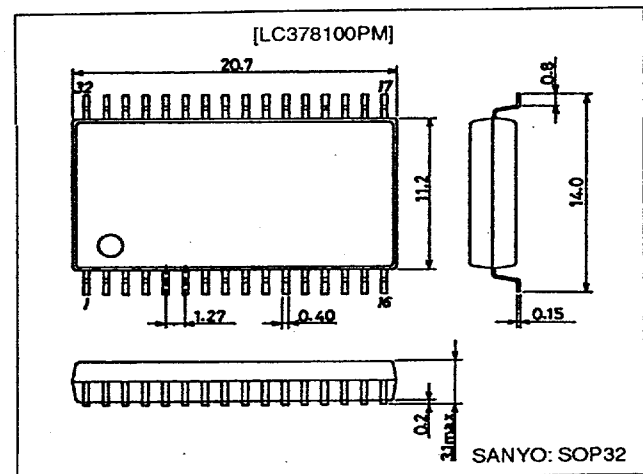
**Package Dimensions**

unit: mm

3192-DIP32



3205-SOP32

**SANYO Electric Co., Ltd. Semiconductor Business Headquarters**

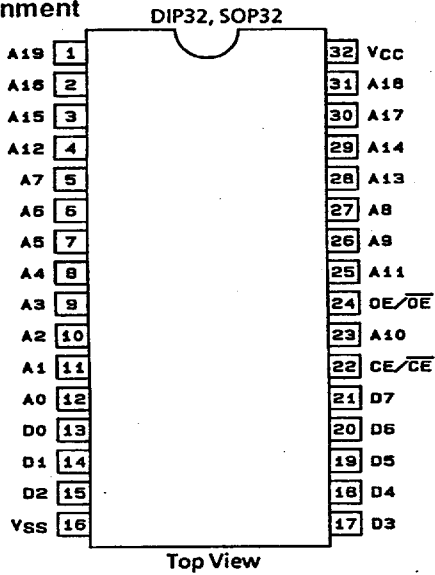
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51195TH (OT)/41095TH (OT) No. 5090-1/5

LC378100PP, PM-10/LC378100PP, PM-20LV

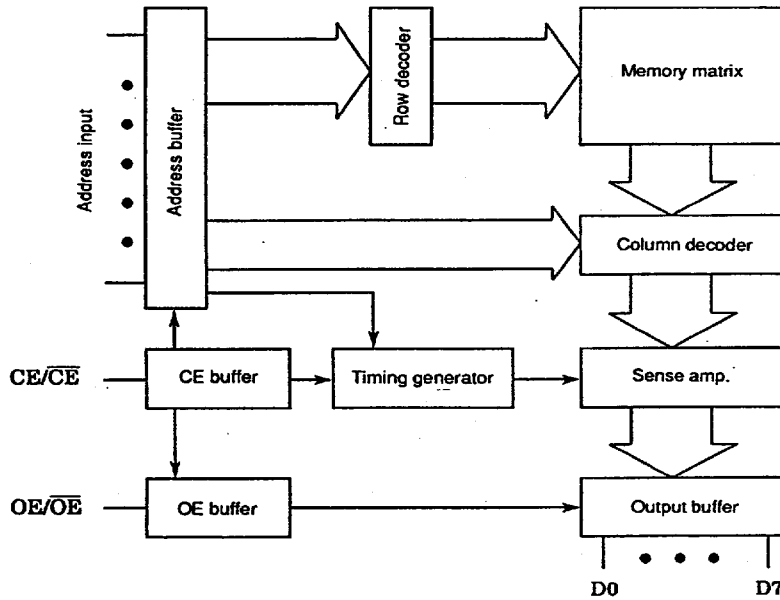
Pin Assignment



Pin Functions

A0 to A19	Address input
D0 to D7	Data output
CE/CE	Chip enable input
OE/OE	Output enable input
V <sub>CC</sub>	Power supply
V <sub>SS</sub>	Ground

Block Diagram



Truth Table

CE/CE	OE/OE	Output	V <sub>CC</sub> current
L/H	X	High-Z	Standby mode
H/L	L/H	High-Z	Operating mode
H/L	H/L	DOUT	Operating mode

X: H or L level should be offered.

## Specifications

### Absolute Maximum Ratings\*1

Parameter	Symbol	Conditions	Ratings	Unit
Maximum power supply voltage	$V_{CC}$ max		-0.3 to +7.0	V
Supply input voltage	$V_{IN}$		-0.3*2 to $V_{CC} + 0.3$	V
Supply output voltage	$V_{OUT}$		-0.3 to $V_{CC} + 0.3$	V
Allowable power dissipation	$P_d$ max	$T_a = 25^\circ\text{C}$ ; Referenced values for the SANYO DIP package	1.0	W
Operating temperature	$T_{opr}$		0 to +70	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-55 to +125	$^\circ\text{C}$

Note: 1. Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to Recommended Operating Conditions.

2.  $V_{IN}$  (min) = -3.0 V (pulse width  $\leq 30$  ns)

### Input/Output Capacitance\* at $T_a = 25^\circ\text{C}$ , $f = 1.0$ MHz

Parameter	Symbol	Conditions	min	typ	max	Unit
Input capacitance	$C_{IN}$	$V_{IN} = 0$ V; Referenced values for the SANYO DIP package			8	pF
Output capacitance	$C_{OUT}$	$V_{OUT} = 0$ V; Referenced values for the SANYO DIP package			10	pF

Note: \* This parameter is periodically sampled and not 100% tested.

### 3 V Operation

#### DC Recommended Operating Ranges at $T_a = 0$ to $+70^\circ\text{C}$

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	$V_{CC}$ max		2.7	3.0	3.6	V
Input high level voltage	$V_{IH}$		$0.8 V_{CC}$		$V_{CC} + 0.3$	V
Input low level voltage	$V_{IL}$		-0.3		+0.4	V

#### DC Electrical Characteristics at $T_a = 0$ to $+70^\circ\text{C}$ , $V_{CC} = 2.7$ to $3.6$ V

Parameter	Symbol	Conditions	min	typ	max	Unit
Operating supply current	$I_{CCA1}$	$\overline{CE} = 0.2$ V ( $CE = V_{CC} - 0.2$ V), $V_I = V_{CC} - 0.2$ V/0.2 V			15	mA
	$I_{CCA2}$	$\overline{CE} = V_{IL}$ ( $CE = V_{IH}$ ), $I_O = 0$ mA, $V_I = V_{IH}/V_{IL}$ , $f = 5$ MHz			20	mA
Standby supply current	$I_{CCS1}$	$\overline{CE} = V_{CC} - 0.2$ V ( $CE = 0.2$ V)			5 (0.5*)	$\mu\text{A}$
	$I_{CCS2}$	$\overline{CE} = V_{IH}$ ( $CE = V_{IL}$ )			50 (10*)	$\mu\text{A}$
Input leakage current	$I_{LI}$	$V_{IN} = 0$ to $V_{CC}$	-1.0		+1.0	$\mu\text{A}$
Output leakage current	$I_{LO}$	$\overline{CE}$ or $\overline{OE} = V_{IH}$ ( $CE$ or $OE = V_{IL}$ ), $V_{OUT} = 0$ to $V_{CC}$	-1.0		+1.0	$\mu\text{A}$
Output high level voltage	$V_{OH}$	$I_{OH} = -0.5$ mA	$V_{CC} - 0.2$			V
Output low level voltage	$V_{OL}$	$I_{OL} = 0.5$ mA			0.2	V

Note: \* Guaranteed at  $T_a = 25^\circ\text{C}$

#### AC Characteristics at $T_a = 0$ to $+70^\circ\text{C}$ , $V_{CC} = 2.7$ to $3.6$ V

Parameter	Symbol	Conditions	min	typ	max	Unit
Cycle time	$t_{CYC}$		200 (150*2)			ns
Address access time	$t_{AA}$				200 (150*2)	ns
Chip enable access time	$t_{CA}$				200 (150*2)	ns
Output enable access time	$t_{OA}$				80 (60*2)	ns
Output hold time	$t_{OH}$		25			ns
Output disable time*1	$t_{OD}$				50	ns

Note: 1.  $t_{OD}$  is measured from the earlier edge of the  $\overline{CE}$  (CE) or  $\overline{OE}$  (OE)'s going high (low).

This parameter is periodically sampled and not 100% tested.

2. Guaranteed at  $V_{CC} = 3.0$  to  $3.6$  V

5 V Operation

DC Recommended Operating Ranges at Ta = 0 to +70°C

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V <sub>CC</sub> max		4.5	5.0	5.5	V
Input high level voltage	V <sub>IH</sub>		2.4		V <sub>CC</sub> + 0.3	V
Input low level voltage	V <sub>IL</sub>		-0.3		+0.8	V

DC Electrical Characteristics at Ta = 0 to +70°C, V<sub>CC</sub> = 5.0 V ± 10%

Parameter	Symbol	Conditions	min	typ	max	Unit
Operating supply current	I <sub>CCA1</sub>	$\overline{CE} = 0.2\text{ V}$ (CE = V <sub>CC</sub> - 0.2 V), V <sub>I</sub> = V <sub>CC</sub> - 0.2 V/0.2 V			30	mA
	I <sub>CCA2</sub>	$\overline{CE} = V_{IL}$ (CE = V <sub>IH</sub> ), I <sub>O</sub> = 0 mA, V <sub>I</sub> = V <sub>IH</sub> /V <sub>IL</sub> , f = 10 MHz			70	mA
Standby supply current	I <sub>CCS1</sub>	$\overline{CE} = V_{CC} - 0.2\text{ V}$ (CE = 0.2 V)			30 (1.0*)	μA
	I <sub>CCS2</sub>	$\overline{CE} = V_{IH}$ (CE = V <sub>IL</sub> )			1.0 (300*)	mA (μA)
Input leakage current	I <sub>I</sub>	V <sub>IN</sub> = 0 to V <sub>CC</sub>	-1.0		+1.0	μA
Output leakage current	I <sub>LO</sub>	$\overline{CE}$ or $\overline{OE} = V_{IH}$ (CE or OE = V <sub>IL</sub> ), V <sub>OUT</sub> = 0 to V <sub>CC</sub>	-1.0		+1.0	μA
Output high level voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1.0 mA	2.4			V
Output low level voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.0 mA			0.4	V

Note: \* Guaranteed at Ta = 25°C

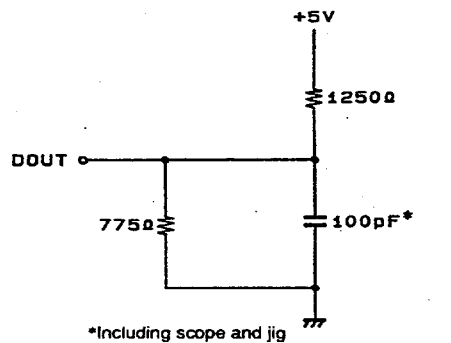
AC Characteristics at Ta = 0 to +70°C, V<sub>CC</sub> = 5.0 V ± 10%

Parameter	Symbol	Conditions	min	typ	max	Unit
Cycle time	t <sub>CYC</sub>		100			ns
Address access time	t <sub>AA</sub>				100	ns
Chip enable access time	t <sub>CA</sub>				100	ns
Output enable access time	t <sub>OA</sub>				40	ns
Output hold time	t <sub>OH</sub>		20			ns
Output disable time*	t <sub>OD</sub>				30	ns

Note: \* t<sub>OD</sub> is measured from the earlier edge of the  $\overline{CE}$  (CE) or  $\overline{OE}$  (OE)'s going high (low). This parameter is periodically sampled and not 100% tested.

AC Test Conditions

Input pulse levels	0.4 V to 0.8 V <sub>CC</sub> (3 V measurement), 0.6 V to 2.6 V (5 V measurement)
Input rise/fall time	5 ns
Input timing level	1.5 V
Output timing level	1.5 V
Output load	70 pF (3 V measurement) See figure (5 V measurement)

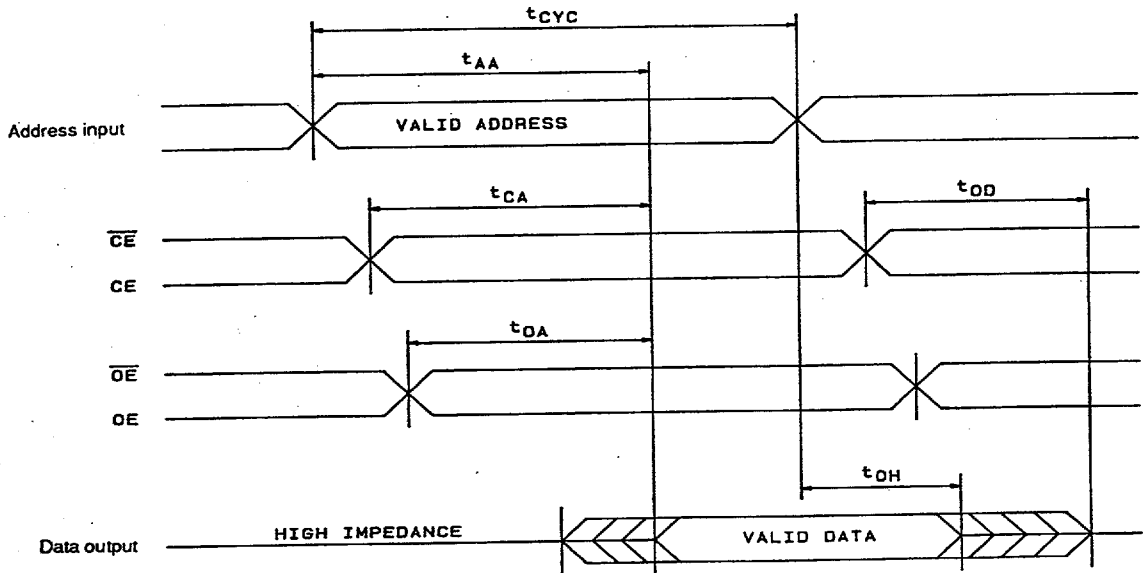


\*Including scope and jig

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Output Load (5 V measurement)

Timing Chart



A03780

Usage Notes

For the reasons of using ATD (Address Transition Detector) circuit, the output data of this LSI directly after supplying voltage are invalid. The valid data would be offered after the transition of at least one of CE or address signals under the stable supply voltage.

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