DG201
Quad SPST CMOS Analog Switch

INTERSIL

T-51-11

GENERAL DESCRIPTION

The DG201 solid-state analog switches are designed using an improved, high-voltage CMOS monolithic technology. They provide performance advantages not previously available from solid-state switches. Destructive latch-up of solid-state analog gates has been eliminated by INTERSIL's CMOS technology.

The DG201 is completely specification and pin-out compatible with the industry standard device.

FEATURES

- **Switches Greater Than 28V_{p-p} Signals With ±15V Supplies**
- **Break-Before-Make Switching t_{off} = 250ns, t_{on} = Typically 500ns**
- **TTL, DTL, CMOS, PMOS Compatible**
- **Non-Latching With Supply Turn-Off**
- **Complete Monolithic Construction**
- **Industry Standard (DG201)**

ORDERING INFORMATION

Industry Standard Part Number	Temperature Range	Package
DG201AK	−55°C to +125°C	16-Pin CERDIP
DG201BK	−25°C to +85°C	16-Pin CERDIP
DG201CJ	0°C to +70°C	16-Pin Plastic DIP

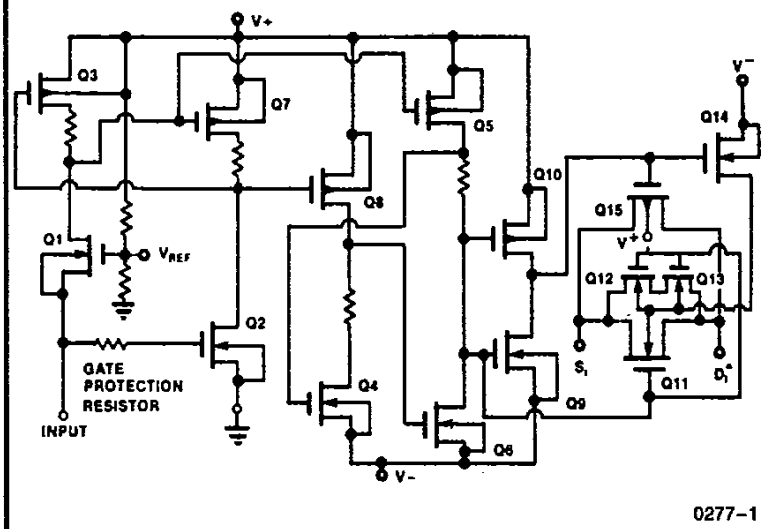

Figure 1: Functional Diagram (¼ DG201) Switch Open For Logic "1" Input

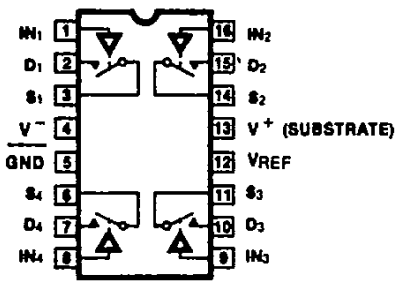

Figure 2: Pin Configuration (Outline dwgs JE, PE) DUAL-IN-LINE PACKAGE

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ABSOLUTE MAXIMUM RATINGS

V^+ to V^- ..... <36V
V^+ to V_D ..... <30V
V_D to V^- ..... <30V
V_D to V_S ..... <28V
V_{REF} to V^- ..... <33V
V_{REF} to V_{IN} ..... <30V
V_{REF} to GND ..... <20V

V_{IN} to GND ..... <20V
Current (Any Terminal) ..... <30mA
Storage Temperature ..... −65°C to +150°C
Operating Temperature ..... −55°C to +125°C
Lead Temperature (Soldering, 10sec) ..... 300°C
Power Dissipation 450mW
Derate 6mW/°C Above 70°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DG201 ELECTRICAL CHARACTERISTICS (T_A=25°C, V^+ = +15V, V^- = −15V)

Per Channel		Test Conditions	Min/Max Limits						Units
			Military			Commercial			
Symbol	Characteristic		−55°C	+25°C	+125°C	0°C	+25°C	+70°C/+85°C	
$I_{IN(ON)}$	Input Logic Current	V_{IN}=0.8V See Note 1	10	±1	10	±1	±1	10	µA
$I_{IN(OFF)}$	Input Logic Current	V_{IN}=2.4V See Note 1	10	±1	10	±1	±1	10	µA
$R_{DS(ON)}$	Drain-Source On Resistance	I_S=10mA V_{ANALOG}=±10V	80	80	125	100	100	125	Ω
$R_{DS(ON)}$	Channel to Channel $R_{DS(ON)}$ Match			25 (typ)			30 (typ)		Ω
V_{ANALOG}	Analog Signal Handling Capability			±15 (typ)			±15 (typ)		V
$I_{D(OFF)}$	Switch OFF Leakage Current	V_{ANALOG}=−14V to +14V		±1	100		±5	100	nA
$I_{S(OFF)}$	Switch OFF Leakage Current	V_{ANALOG}=−14V to +14V		±1	100		±5	100	nA
$I_{D(ON)}$ + $I_{S(ON)}$	Switch ON Leakage Current	V_D=V_S=±14V		±2	200		±5	200	nA
t_{on}	Switch "ON" Time See Note 2	R_L=1kΩ, V_{ANALOG} =−10V to +10V See Figure 3		1.0			1.0		µs
t_{off}	Switch "OFF" Time See Note 2	R_L=1kΩ, V_{ANALOG} =−10V to +10V See Figure 3		0.5			0.5		µs
$Q_{(INJ.)}$	Charge Injection	See Figure 4		15 (typ)			20 (typ)		mV
OIRR	Min. Off Isolation Rejection Ratio	f=1MHz, R_L=100Ω, C_L≤5pF See Figure 5		54 (typ)			50 (typ)		dB
I^+_Q	+ Power Supply Quiescent Current	V_{IN}=0V to 5V	2000	1000	2000	2000	1000	2000	µA
I^-_Q	−Power Supply Quiescent Current		2000	1000	2000	2000	1000	2000	µA
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio	One Channel Off		54 (typ)			50 (typ)		dB

NOTE 1: Typical values are for design aid only, not guaranteed and not subject to production testing.

NOTE: All typical values have been characterized but are not tested.

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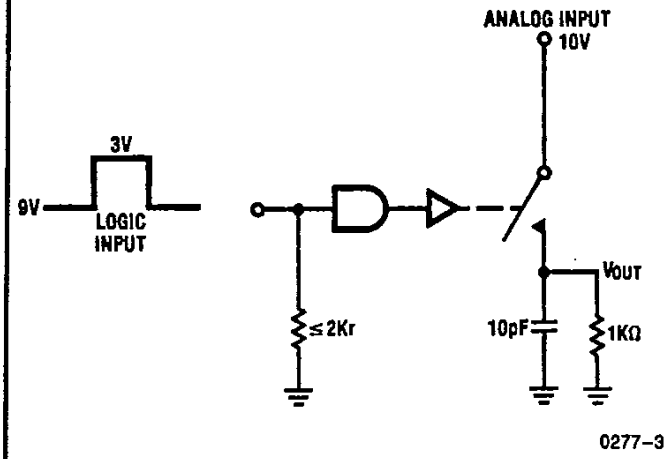
TEST CIRCUITS



(Note 2)

Figure 3

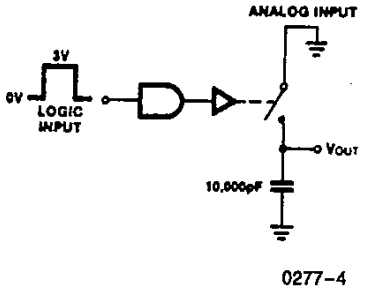


Figure 4

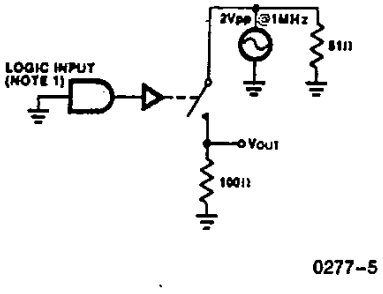
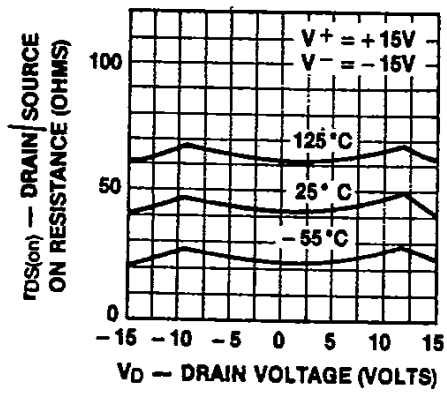
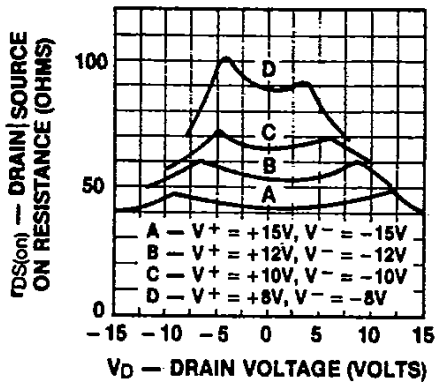


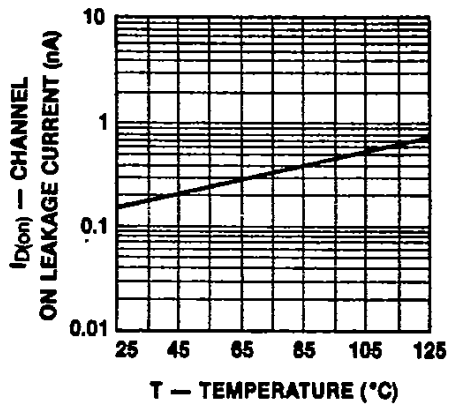
Figure 5

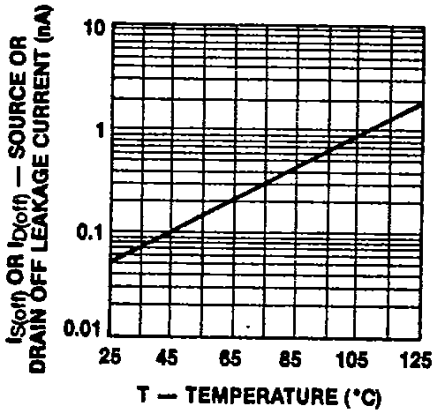
NOTE 2: All channels are turned off by high "1" logic inputs and all channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the min. range for switching properly. Peak input current required for transition is typically −120μA. Pull down resistor, if used, ≤ 2KΩ.

TYPICAL PERFORMANCE CHARACTERISTICS









NOTE: All typical values have been characterized but are not tested.

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APPLICATIONS

Using the V_{REF} Terminal

The DG201 has an internal voltage divider that sets the TTL threshold on the input control lines for $V^+ = 15V$. The schematic is shown here, with nominal resistor values, giving approximately 2.4V on the V_{REF} pin. As the TTL input signal goes from +0.8V to +2.4V, Q1 and Q2 switch states to turn the switch ON and OFF.

If the power supply voltage is less than +15V, then a resistor needs to be added between V^+ and V_{REF} pin, to restore +2.4V at V_{REF}. The table shows the value of this resistor for various supply voltages, to maintain TTL compatibility. If CMOS logic levels with a +5V supply are being used, the threshold shifts are less critical, but a separate column of suitable values is given in the table. For logic swings of −5V to +5V, no resistor is needed.

In general, the "low" logic level should be <0.8V to prevent Q1 and Q2 from both being ON together (this will cause incorrect switch function). With open collector logic, and a low value of pull-up resistor, the logic 'low' level can be above 0.8V. In this case, INTERSIL can supply parts with thresholds >1.5V(consult factory). The V_{REF} point should be set at least 2.6V above this "low" state, or to >4.1V. An external resistor of 27kΩ and V_{REF} is required, for a +15V supply.

V+ Supply (V)	TTL Resistor (kΩ)	CMOS Resistor (kΩ)
+15	–	–
+12	100	–
+10	51	–
+9	(34)	34
+8	(27)	27
+7	18	18

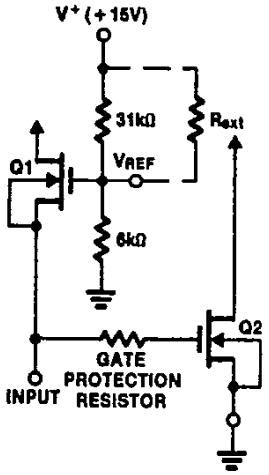

Figure 6