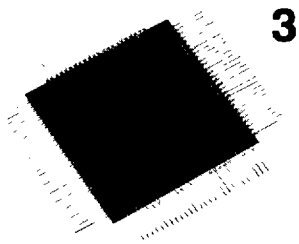
ILC DATA DEVICE CORPORATION®

DD-03232

32-CHANNEL DISCRETE-TO-DIGITAL INTERFACE "R3D3"



DESCRIPTION

The DD-03232 devices are 32-channel discrete-to-digital interfaces with universal HIRF-isolated inputs to handle 28V/Open, Open/GND and 28V/Gnd signals.

Using comparators in a triple-redundant configuration, the devices will take consensus on input states and raise a flag when consensus fails. Its output is an addressable 8-bit or 16-bit tri-state port, selectable for channel data, status, bounce, built-in self-test (BIST) and major fault, compatible with TTL logic.

APPLICATIONS

The design specifically addresses chip-level redundancy, built-in self-test autonomy, fault isolation and tolerance.

With high reliability and low cost, these features enable the devices to serve a variety of interface requirements in avionic applications, including flight critical, essential, and non essential functions. The optional ARINC 429 output port is particularly well-suited to data-concentrator requirements.

FEATURES

- ***Triple Redundancy***
- ***HIRF Layer***
- ***Universal Inputs***
  - ***28V/Gnd***
  - ***Open/Gnd***
  - ***28V/Open***
- ***Built-in Self-Test***
- ***Soft Failure Reporting***
  - ***Deferred Maintenance***
  - ***Higher MTBUR***
- ***Optional ARINC 429 Output Port***

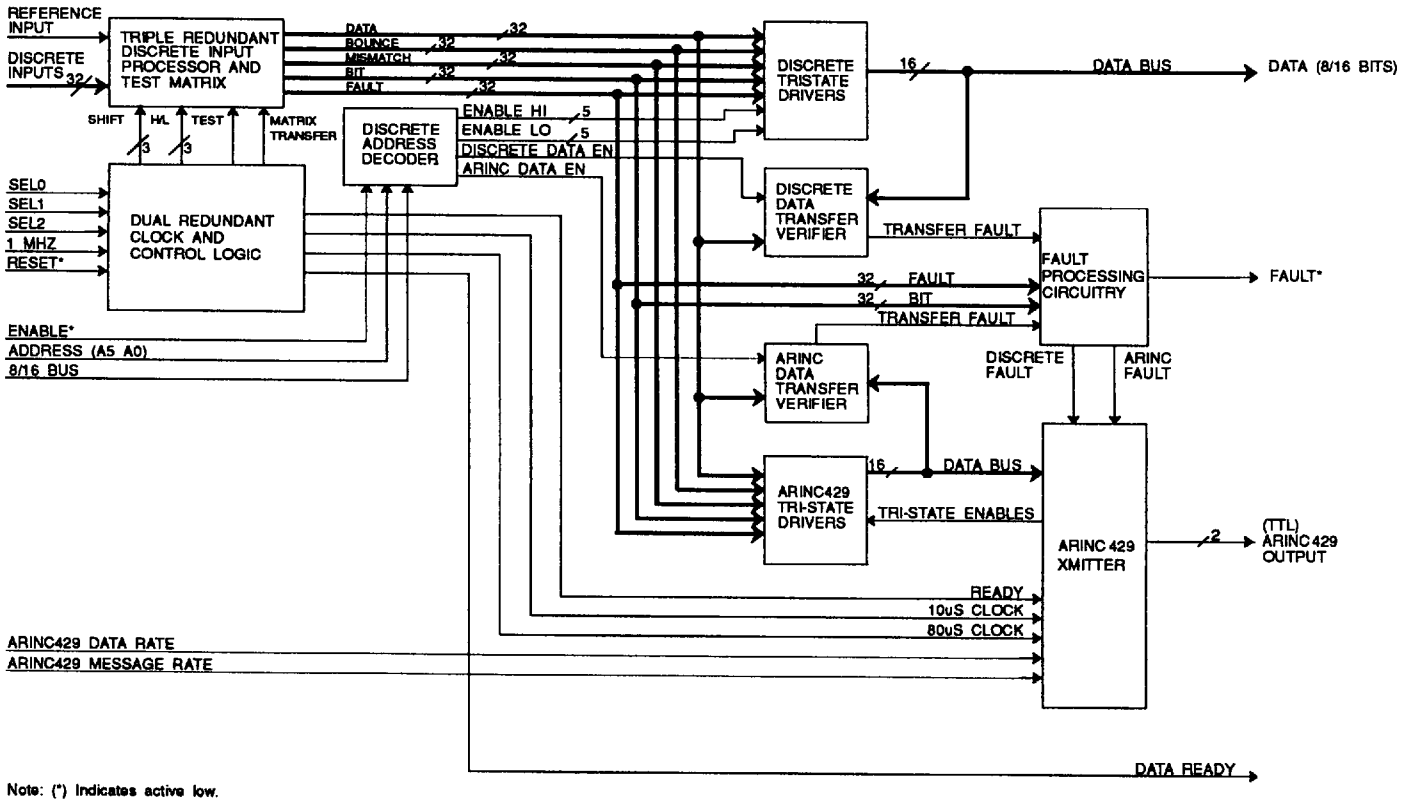


FIGURE 1. DD-03232 BLOCK DIAGRAM

TABLE 1. DD-03232 SPECIFICATION				
PARAMETER	**UNITS**	**MIN**	**TYP**	**MAX**
ABSOLUTE MAXIMUM RATINGS				
Supply Voltages (V_{CC}, V_{DD})	V	-0.3	5.0	7.0
Reference Inputs	V	-80		+80
Discrete Inputs	V	-80		+80
Digital Inputs	V	-0.3		V_{DD}+0.3
DIGITAL INPUTS/OUTPUTS				
Logic Compatibility (See Note 1)	TTL/ CMOS			
Digital Inputs				
■ V_{IH} (V_{DD} = +5.5V)	V	+3.85		
■ V_{IL} (V_{DD} = +4.5V)	V	1.35		
■ I_{IL1} (V_{IN} = 0) (See Note 2)	µA	-40		-400
■ I_{IH1} (3< V_{IN} < V_{DD}) (See Note 2)	µA	0		-400
■ I_{IL2} (V_{IN} = 0) (See Note 3)	µA	-400		-1000
■ I_{IH2} (3< V_{IN} < V_{DD}) (See Note 3)	µA	0		-700
Clock Input (See Note 4)	MHz	0.99	1.00	1.01
Digital Outputs				
■ V_{OH} (I_{OH} = -4ma)	V	V_{DD}-0.5		
■ V_{OL} (I_{OH} = 4ma)	V	0.5		
Analog Inputs	See FIGURE 3			
POWER SUPPLY REQUIREMENTS (Total V_{DD}, Analog & Digital) I_{DD} (V_{DD} = +5V [Digital Outputs Unloaded])	ma		25	45
POWER DISSIPATION P_D	mw		125.0	250.0

TABLE 1. DD-03232 SPECIFICATION				
PARAMETER	**UNITS**	**MIN**	**TYP**	**MAX**
THERMAL				
Operating Temperature				
■ Type 1	°C	-40		85
■ Type 2	°C	-55		125
■ Type 3	°C	0		70
Storage Temp	°C	-65		150
Lead Temperature				
(localized, 1 sec. duration)	°C			280
(body, 2 sec. duration)	°C			210
Junction Temperature				
θ_{jc}	°C/W		5.0	
θ_{ca}	°C/W		20.0	
MTBF per Mil-Hbk-217 for Airborne Inhabited Cargo at 64°C	1,400,000 hrs. plastic 1,540,000 hrs. ceramic			
PHYSICAL CHARACTERISTICS				
Size	in.	2.3 x 2.3		
	(cm)	(5.84 x 5.84)		
Weight	oz.	1.0		
	(g)	(26.0)		

Note 1: ASIC inputs are CMOS. TTL compatability is achieved with on-board 10KΩ pull-up resistors for ADDRESS and $\overline{\text{ENABLE}}$ inputs only.
Note 2: For all inputs except $\overline{\text{ENABLE}}$ and A0 - A5.
Note 3: For $\overline{\text{ENABLE}}$ and A0 - A5.
Note 4: For ARINC 429 option the bit rate is derived from the clock. Refer to ARINC 429 Bit Rate to avoid interference. ARINC 429-14 (January 4, 1993), paragraph 2.4 "Timing Related Elements" contains a "COMMENTARY" section following subparagraph 2.1.4.2 ("Low Speed Operation") that cautions against using "precisely" 100 kilobits per second.

WHAT IS A DISCRETE?

Advisory Circular (FAA), Airworthiness Approval of Traffic Alert and Collision Avoidance Systems (TCAS II) and Mode S Transponders, AC20-131, defines a discrete as "a separate, complete and distinct signal." In many instances these signals are binary, on or off, 28V-based signals; they are typically Open/Ground, 28V/Open, or 28V/Ground with very low bandwidth (DC to 200Hz).

While on the surface the translation of these signals to TTL-levels compatible with digital avionics may seem simple, RTCA DO-160C power, lightning and high-intensity-radiated-fields (HIRF) are complicating factors. Add to that the desire to have a standardized, addressable, reliable interface and the challenge is apparent.

Today's systems address the interface with tailored circuits for each interface comprised of R-C input filters, divider networks, diode isolation and comparators. Multichannel interface to a processor requires additional logic and latches. The resulting circuit generally lacks any built-in test capability, consumes considerable pc-board real estate (up to 1 sq. in. per channel), and offers no chip-level redundancy.

FUNCTIONAL INTEGRATION

Using the aggregated signal definition and functional requirements of industry, ILC Data Device Corporation has developed a 32-channel discrete interface with universal HIRF-isolated inputs to handle 28V/Open, Open/Gnd and 28V/Gnd signals. Using comparators in a triple-redundant configuration, each channel will take consensus on input state, raising a flag when consensus fails. Each channel is routed through 3 separate HIRF circuits and 3 different comparators located on 3 different chip edges. Its output is a selectable 8-bit or 16-bit tri-state port, addressable for channel data, status, bounce, mismatch, built-in self-test and major fault information.

Its design specifically addresses chip-level redundancy, built-in self-test autonomy, fault isolation and tolerance. Moreover, its functional integration results in significant added reliability. A comparative look at MTBF calculated in accordance with MIL-HBK-217 for airborne inhabited cargo environments at 64°C indicates an order of magnitude improvement (1,540,000 hours vs. 173,000 hours) for a ceramic packaged integrated approach vs. a similarly packaged discrete-component implementation. Moreover, the real estate is reduced from 32 square inches to 5.3 square inches.

Additional Key Features include:

FAULT ISOLATION: Triple-redundant comparators are located on three different edges of the custom chip such that an edge-failure is not catastrophic.

FAULT TOLERANCE: A single comparator failure is reported as a mismatch or BIT fault, but does not result in a hard- failure.

BOUNCE: Relays and switches, as mechanical devices, have a characteristic "bounce" to their signal transition. It is desirable to mask this bounce by delaying the output digital transition accordingly. The sampling rate of the device can be varied to allow for debounce of relay/switch inputs. In addition, the triple sampling of a given comparator enables a consistent reading of otherwise asynchronous signals. Bounce is an addressable status that allows the user to detect bouncing or intermittent relays/switches.

GROUND DIFFERENTIALS: When the reference inputs are connected to the 28V supply, the thresholds are designed to tolerate ±3.5V ground differences.

REGISTERS: 8-bit or 16-bit selectable data or status is available via tri-state buffers for interface to any system processor.

OPTIONAL ARINC429 PORT: A serial ARINC 429 output is available for data-concentrator applications. This enables the transfer of data to other systems with a minimum of wiring and processor loading.

HIRF: The device incorporates passive circuitry to isolate the intelligence from both lightning effects and radiated fields as defined in DO-160C. This protection is applicable to the discrete inputs, reference inputs, and their relationship to each other and to ground.

TEST PATTERNS: Internal Test Patterns can be selected to produce alternating "1"s and "0"s to verify that all address and data bits are operational. While these outputs are always available, regardless of READY state, they must be addressed by the user (A5...A0) in accordance with TABLES 3 and 4.

DISSIMILAR PATHS: Errors are reported through the registers and through the optional ARINC 429 port as cross checks.

DEFERRED MAINTENANCE: The error reporting scheme differentiates soft and hard failures to allow continued operation despite failures.

INTELLIGENCE: The device built-in-test, status reporting scheme, and fault-tolerance/isolation significantly reduce application software requirements. FIGURE 1 illustrates the model DD-03232 functional block diagram.

MICROPROCESSOR INTERFACE

READ CYCLE TIMING

The DD-03232 is configured to interface between an 8/16-bit microprocessor. FIGURE 2 illustrates this interface.

The read cycle(s) should be preceeded by polling the device's READY bit located within the Status Register. The Status Register can be read at any time regardless of the state of the READY signal (pin) from the device.

If the READY bit is at logic 1 (this can be easily tested by a branch if negative statement) the address of the desired register, along with the negative true $\overline{\text{ENABLE}}$ signal, should be presented to the device. The addressed data will be available within 100 ns.

After the data is read the $\overline{\text{ENABLE}}$ line should be returned to the logic 1 level.

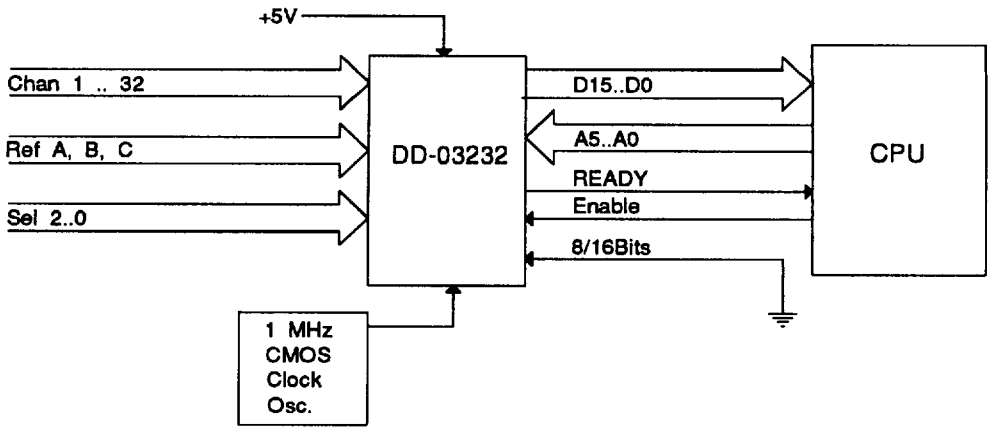
All of the data within the device is guaranteed to remain stable for at least 20 µs after the high-to-low transition of the READY signal (see FIGURE 3).

ANALOG INPUTS

ANALOG INPUT CHANNELS: (Pins 25, 26, 29-56, 59 and 61) 200KΩ input resistance, 500µs time constant, responsive to Open/Gnd (when configured with appropriate external pull-up), 28V/Open and 28V/Gnd input with HIRF/lightning immunity. Refer to FIGURE 4 for a detail of the input structure. As illustrated, the inputs are triple redundant, including HIRF, and use comparators on 3 different edges of the chip to minimize the impact of common-mode failures.

REFERENCE: Triple redundant, configured for 28V tracking discretes. User adjustable for other reference levels by connecting external resistors between corresponding TRIM and REF inputs.

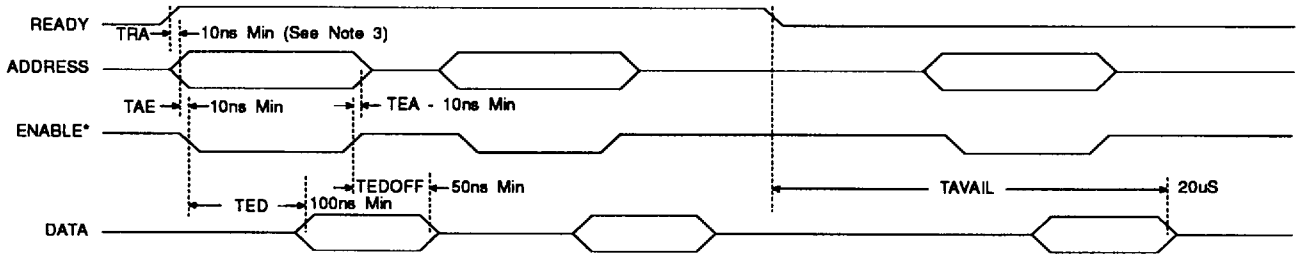
FIGURE 4 also shows the reference structure. Each set of Ref/Trim inputs must be configured identically. For 28V supply tracking, Ref A, Ref B and Ref C are all connected to the 28V supply while Trim A, Trim B and Trim C are left open.



NOTE: 1) If 8/16 Bits pin is tied to +5 Volts, then the DD-03232 is in 8-Bit Mode.
The following must also be modified:
D0 tied to D8
D1 tied to D9
D2 tied to D10
D3 tied to D11
D4 tied to D12
D5 tied to D13
D6 tied to D14
D7 tied to D15

2) If the ARINC 429 option is not used, then pin 104 (429STRBI) MUST be grounded for the "bounce" circuit to operate properly.

FIGURE 2. R3D3 TO CPU INTERFACE



Note:
1) TRA = Time Ready Address
TAE = Time Address Enable
TED = Time Enable Data
TEA = Time Enable to Address
TEDOFF = Time Enable Off - Data Off
TAVAIL = Time Ready* - Data Available
2) (*) Indicates active low.
3) When driven from a TTL device, this time will increase to 200ns.

FIGURE 3. READ CYCLE TIMING

REF A, B, C: (Pins 17, 19 and 21) Input to the divider supplying the reference voltage to the "A", "B" & "C" group of 32 input channels.

TRIM A, B, C: (Pins 16, 18 and 20) Junction of the first resistor and the rest of the reference "A", "B", and "C" divider.

DIGITAL INPUTS

All digital input pins function as current sources.

DEBOUNCE (SEL2..SEL0): (Pins 4-6) The input Discrete Sampling Rate (Debounce Time) is user programmable via the three Select lines (SEL2..SEL0) in accordance with the TABLE 2. The intent of this function is to mask the bounce of the input discrete appropriate to its characteristic performance. See "bounce" on page 3.

TABLE 2. DISCRETE SAMPLING RATE

SELECT (SEL2..SEL0)	SAMPLE RATE
000	5 ms
001	10 ms
010	20 ms
011	50 ms
100	100 ms
101	200 ms
110	500 ms
111	1000 ms

$\overline{\text{ENABLE}}$: (Pin 97) The $\overline{\text{ENABLE}}$ line controls the tri-state drivers of the 8 or 16 bit Data Bus outputs. The tri-state Data Bus drivers are enabled when this signal is at logic 0 and are tri-stated when this signal is at logic 1. $\overline{\text{ENABLE}}$ is a read signal and should only be low during reads.

8/16 BITS: (Pin 73) "0" Selects 16-Bit databus output, "1" selects 8-Bit databus output.

ADDRESS LINES (A5..A0): (Pins 91-96) The six address lines (A5..A0 where A0 is the LSB) provide for the selection of the desired 8- or 16-bit Data Bus information in accordance with TABLES 3 and 4 (Word/Byte Modes).

CLOCK (1 MHz CLK): (Pin 106) The user must supply a 1 MHz clock whose stability is of no importance except to the serial bit rate of the optional ARINC 429 port (see Note 4 of TABLE 1). The clock is brought into the internal ASIC at 2 widely separated points designated as CLOCK_A (primary) and CLOCK_B (secondary).

The primary clock will be selected and drive the device unless a clock fault is detected, in which case the operation of the device will be switched over to the secondary clock.

Both clocks are continually monitored for status and this information is available as separate bits in the Status Register.

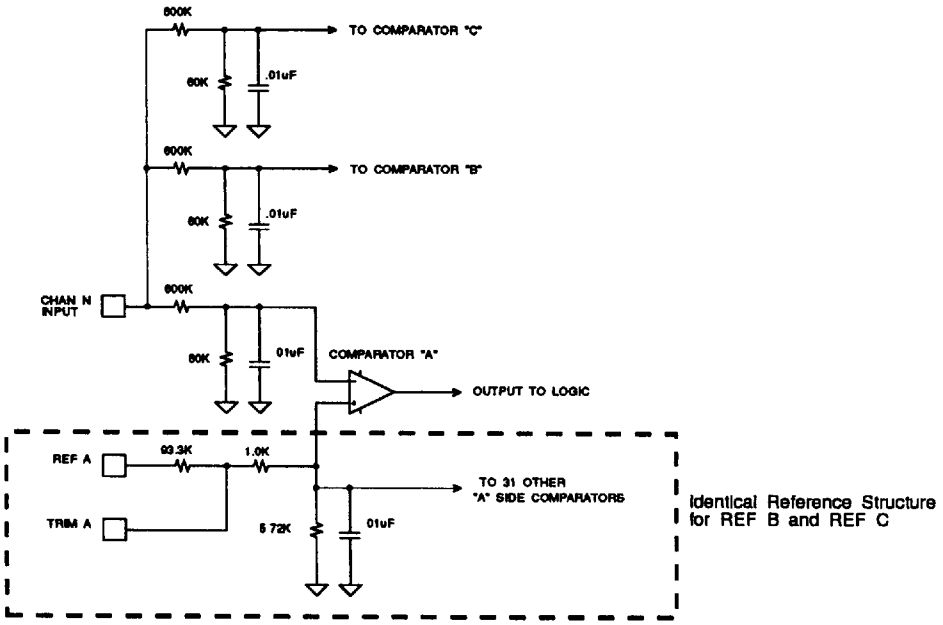


FIGURE 4. DD-03232 INPUT STRUCTURE

TABLE 3. WORD MODE (16-BIT BUS)	
ADDRESS (A5..A0)	DATA (D7..D0)
00 000X	BOUNCE CH_16..CH_01
00 001X	BOUNCECH_32..CH_17
00 010X	MISMATCH CH_16..CH_01
00 011X	MISMATCH CH_32..CH_17
00 100X	BIT CH_16..CH_01
00 101X	BIT CH_32..CH_17
00 110X	FAULT CH_16..CH_01
00 111X	FAULT CH_32..CH_17
01 000X	DATA CH_16..CH_01
01 001X	DATA CH_32..CH_17
01 010X	TEST PATTERN 0's and 1's
01 011X	STATUS REGISTER
01 100X	FACTORY TEST WORD 1
01 101X	FACTORY TEST WORD 2
01 110X	FACTORY TEST WORD 3
01 111X	FACTORY TEST WORD 4
10 000X	NOT USED
10 001X	NOT USED
10 010X	NOT USED
10 011X	NOT USED
10 100X	NOT USED
10 101X	TEST PATTERN 1's and 0's
10 110X	NOT USED
10 111X	:
11 111X	NOT USED

TABLE 4. BYTE MODE (8-BIT BUS)	
ADDRESS (A5..A0)	DATA (D7..D0)
00 0000	BOUNCE CH_08..CH_01
00 0001	BOUNCE CH_16..CH_09
00 0010	BOUNCE CH_24..CH_17
00 0011	BOUNCE CH_32..CH_25
00 0100	MISMATCH CH_08..CH_01
00 0101	MISMATCH CH_16..CH_09
00 0110	MISMATCH CH_24..CH_17
00 0111	MISMATCH CH_32..CH_25
00 1000	BIT CH_08..CH_01
00 1001	BIT CH_16..CH_09
00 1010	BIT CH_24..CH_17
00 1011	BIT CH_32..CH_25
00 1100	FAULT CH_08..CH_01
00 1101	FAULT CH_16..CH_09
00 1110	FAULT CH_24..CH_17
00 1111	FAULT CH_32..CH_25

TABLE 4. BYTE MODE (8-BIT BUS) continued	
ADDRESS (A5..A0)	DATA (D7..D0)
01 0000	DATA CH_08..CH_01
01 0001	DATA CH_16..CH_09
01 0010	DATA CH_24..CH_17
01 0011	DATA CH_32..CH_25
01 0100	TEST PATTERN 0's and 1's
01 0101	TEST PATTERN 0's and 1's
01 0110	STATUS REGISTER LO
01 0111	STATUS REGISTER HI
01 1000	FACTORY TEST WORD 1 LO
01 1001	FACTORY TEST WORD 1 HI
01 1010	FACTORY TEST WORD 2 LO
01 1011	FACTORY TEST WORD 2 HI
01 1100	FACTORY TEST WORD 3 LO
01 1101	FACTORY TEST WORD 3 HI
01 1110	FACTORY TEST WORD 4 LO
01 1111	FACTORY TEST WORD 4 HI
10 0000	NOT USED
10 0001	NOT USED
10 0010	NOT USED
10 0011	NOT USED
10 0100	NOT USED
10 0101	NOT USED
10 0110	NOT USED
10 0111	NOT USED
10 1000	NOT USED
10 1001	NOT USED
10 1010	TEST PATTERN 1's and 0's
10 1011	TEST PATTERN 1's and 0's
10 1100	NOT USED
10 1101	:
11 1111	NOT USED

Note 1: A true BOUNCE bit indicates that the input signal of the associated channel changed in an alternating fashion i.e. OFF-ON-OFF or ON-OFF-ON in three successive samples at the selected sample rate.

Note 2: A MISMATCH bit that is true indicates that one of the triple redundant inputs of the associated channel did not agree with the other two for three consecutive samples of the input i.e. there was a lack of consensus for the three inputs.

Note 3: A BIT indication for any channel signifies that the associated channel has failed the Built-In-Test sequence which is performed prior to every input sample taken. These signals are reset at the start of each Built-In-Test sequence, and will be set if any of the tests in the sequence fail. A BIT indication is a SOFT FAULT condition indicating that there is a problem with the channel but the associated output data can be believed because of the internal voting taking place.

Note 4: A FAULT bit that is true indicates that the associated channel has a major problem and the associated data should not be believed. A FAULT indication is a HARD FAULT condition indicating that the Built-In-Test has failed one or more of the voting tests.

Note 5: A DATA bit indicates the triple redundant vote or unanimous consensus of the input discrete state for the associated channel over the last two data samples taken.

Note 6: The two available TEST PATTERNS contain an alternating string of 1's and 0's, and 0's and 1's, which can be used to verify that all of the data bits are operational (i.e. there are no stuck bits). The two test patterns have been located at addresses of alternating address bits so that the address decoder bits are tested at the same time.

FACTORY TEST INPUTS: (Pins 23, 22 ,100 AND 101) The TMUX, TMODE, FMUX and FMODE input signals are used for factory testing and should be tied to logic 1 for the device to operate properly.

RESET: (Pin 24) The RESET signal is used to reset the device during factory testing. It is connected to an internal RC network to provide a Power-on-Reset for the device. Under normal operating conditions this pin should be a no-connect. If there is some reason to reset the device from external circuitry this pin can be momentarily pulled to logic 0 through an open collector device. **Do not hard wire this pin to +5V or ground.**

OUTPUTS

DATA (D15..D0): (Pins 74, 76-90) 8-bit byte or 16-bit word information is available on the Data Bus depending on the logic state of the BUS Select line described above.

In the Byte mode the upper and lower Bytes are enabled separately so that bit 0 can be hard wired to bit 8, bit 1 to bit 9 etc. thereby providing an 8-bit data bus.

It is obviously important that the 8-bit mode be selected if these data bits are wired together or corrupted data will result. The available data can be found under the Address Lines section above.

FAULT: (Pin 99) The FAULT flag was designed to serve as an interrupt to the microprocessor when a HARD or SOFT error has been detected within the device (see BIT and FAULT notes in TABLE 4). If this signal is asserted (logic 0) the Status Register should be read to determine the nature of the fault. Thereafter more detailed information can be found in the associated addressable registers. The Fault Flag will remain at a logic 0 for as long as the fault condition persists. FIGURE 5 illustrates the fault logic tree.

Note: Depending on the exact nature of the fault, the Fault Flag may return to logic 0 during the Built-In-Test interval (when the READY signal is at logic 0) if there is a persistent fault condition.

Fault Conditions:

FAULT is 0 for any of the following fault conditions. The reason for the fault can be obtained from the status register which is accessible regardless of READY state. FIGURE 6 shows the contents of the status register.

A definition of each bit is as follows:

BIT FAULT: A logic 1 for this bit indicates that one of the channels has failed the Built-In-Test sequence. The actual offending channel(s) can be determined by reading the associated BIT data words.

DISCRETE FAULT: A logic 1 for this bit indicates that one of the channels detected a HARD failure during the Built-In-Test sequence or that the discrete input data word did not transfer to the data bus output properly when it was read. If a HARD fault was detected the offending channel can be determined by reading the associated FAULT data registers. If it was generated by a transfer error the DISCRETE TRANSFER FAULT bit in this status register will be set to logic 1.

ARINC FAULT: A logic 1 for this bit indicates that one of the channels detected a HARD failure during the Built-In-Test sequence or that the discrete input data word did not transfer to the ARINC transmitter section properly.

If a HARD fault was detected the offending channel can be determined by reading the associated FAULT data registers. If it was generated by a transfer error then no FAULT bits will be set to logic 1. (Note 1)

ARINC READY: A logic 0 for this bit indicates that an ARINC transmission is currently in process. A logic 1indicates that no ARINC transmission is currently in process. (Note 1)

CLOCK_A FAULT: A logic 1 for this bit indicates that the primary 1 MHz clock circuitry is defective and that the device is running off the secondary 1 MHz clock.

CLOCK_B FAULT: A logic 1 for this bit indicates that the secondary 1 MHz clock circuitry is defective and cannot be used as a backup.

BIT	SIGNAL
00	BIT FAULT
01	DISCRETE FAULT
02	ARINC FAULT
03	ARINC READY
04	CLOCK_A FAULT
05	CLOCK_B FAULT
06	NO CLOCK
07	DISCRETE TRANSFER FAULT
08	LOGIC LOW (HIGH BYTE)
09	LOGIC LOW
10	LOGIC LOW
11	LOGIC LOW
12	LOGIC LOW
13	LOGIC LOW
14	LOGIC LOW
15	READY

FIGURE 6. STATUS WORD BIT MAP

Note: All bits available regardless of ready-state.

Note 1: This signal is only meaningful for the ARINC 429 device option.

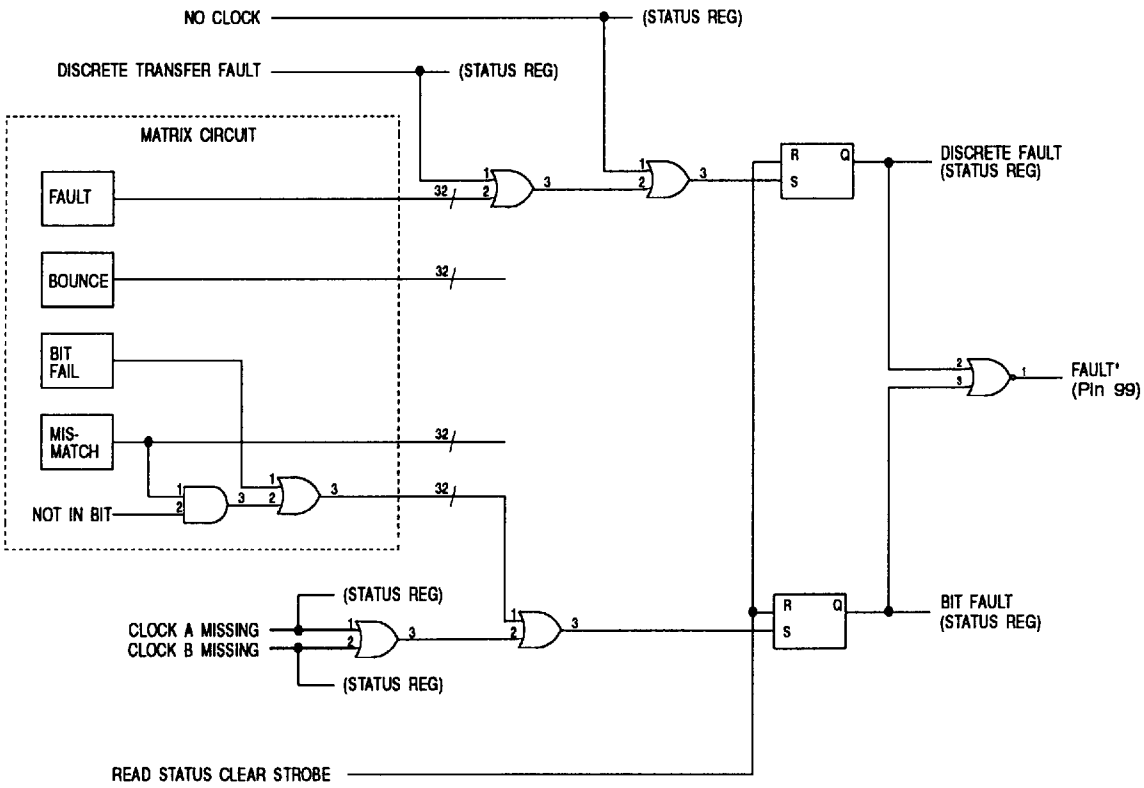


FIGURE 5. FAULT LOGIC TREE

NO CLOCK: A logic 1 for this bit indicates that there is no 1MHz clock being supplied to the device (or that both have failed).

DISCRETE TRANSFER FAULT: A logic 1 for this bit indicates that the discrete data word(s) did not transfer properly during the associated microprocessor read cycle (i.e. the word present on the data bus did not agree with the internal data). The most likely cause of this type of fault is a collision on the data bus during the read cycle.

Note: This condition is only monitored for the discrete data words, not for all of the available data.

CLKTST: (Pin 106) This signal is used for factory testing and should not be connected to any external circuitry or normal operation of the device could be affected. Specifically this signal is a low drive internal test point connected to the primary clock signal. Grounding this signal forces the device to switch to the secondary internal clock.

READY: (Pin 98) A logic 1 for this bit indicates that all of the available data is stable and can be read. A logic 0 indicates that the device is in the Built-In-Test mode, or taking a sample of the discrete input data lines.

This signal should be polled directly or by reading the status word prior to performing any read cycles. The internal data is guaranteed to be stable for 20 µs after the logic 1 to logic 0 transition (READY to NOT READY) of this signal. Therefore, it should not be necessary to repoll this signal after the read.

Note 1: This signal is only meaningful for the ARINC 429 device option.

ARINC 429 PORT (OPTIONAL)

DD-03232XX-XX4 indicates the inclusion of the ARINC 429 data output. The option enables transmission of discrete data via a serial ARINC 429 (CMOS levels) output simultaneous with the 8/16-bit BUS output. The following features and pins apply:

ARINC 429 DATA RATE (429DRATE): (Pin 1) A logic 1 (or a no-connect) for this input selects the ARINC 429 Low Speed data rate of 12.5 KHz. A logic 0 selects the High Speed data rate of 100 KHz . (Note 1)

ARINC 429 MESSAGE RATE (429MRATE): (Pin 3) The message rate of the ARINC 429 output is selectable at either a fixed 100ms rate or at the selected sampling rate of the input discretes. A logic 1 selects the input sampling rate as the message rate, and a logic 0 selects the fixed 100 ms message rate.(Note 1)

Note: If the Low Speed ARINC 429 bit rate is selected (12.5 KHz) an entire ARINC message will take about 35 ms to complete, therefore, input discrete sampling rates of 5ms, 10ms, and 20ms cannot be utilized or the ARINC message will be truncated unless the fixed 100 ms message rate is selected.

429 STROBE IN (429STRBI): (Pin 104) This pin is utilized in the special case when the device is being used as a remote ARINC 429 serial port and not connected to a local microprocessor. When the device is being used in this specific configuration the associated 429 Strobe Out should be connected to this pin. In other cases this pin must be grounded.

Related Information: Because the BOUNCE data is momentarily latched within the device, this information is normally reset by a READ to the associated BOUNCE data words. In the instances when there is no microprocessor, and therefore no READS to the BOUNCE data, this connection provides a mechanism to reset the source of the BOUNCE information (just after it is transferred to the ARINC transmitter section) at the start of each ARINC message. (Note 1)

429 STROBE OUT (429STRB0): (Pin 2) This signal is used in conjunction with the "429 Strobe In" described above. It is basically a 500 ns positive pulse which occurs at the start of each 429 message. See the section "429 Strobe In" for further information concerning the use of this signal. (Note 1)

ARINC_LO AND ARINC_HI: (Pin 102 and 103) These two signals comprise the ARINC 429 serial output transmission. Both are TTL compatible signals where the ARINC_LO signal contains the logic 0 serial transmission and the ARINC_HI signal contains the logic 1 serial transmission. These two signals must be connected to a DD-03182, 429 Line Driver, in order to obtain a single ended ARINC 429 transmission signal. FIGURE 9 illustrates this interface.

The content and word order of the ARINC 429 transmission is shown in FIGURE 7. (Note 1)

As noted, these features are only guaranteed and tested if the ARINC 429 option is selected. In addition, the clock frequency (1 MHz) must be selected carefully so as not to interfere with other avionic communications as detailed in ARINC 429. The ARINC 429 option bit rate is derived from the (1 MHz) clock. Refer to ARINC 429 Bit Rate to avoid interference. ARINC 429-14 (January 4, 1993), paragraph 2.4 "Timing Related Elements" contains a "COMMENTARY" section following subparagraph 2.1.4.2 ("Low Speed Operation") that cautions against using "precisely" 100 kilobits per second.

Note 1: This signal is only meaningful for the ARINC 429 device option.

	PAR	SSM		MSB									16 BIT DATA						LSB		F	C	SDI		LABEL REVERSED OCTAL								
																									LSB							MSB	
ARINC 429 BITS:	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
TRIPLE BOUNCE 16..1	P	A	B	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	0	F	C	0	0	1	0	0	0	0	0	0	0	001
TRIPLE BOUNCE 32..17	P	A	B	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	0	F	C	0	0	0	1	0	0	0	0	0	0	002
MISMATCH 16..1	P	A	B	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	0	F	C	0	0	1	1	0	0	0	0	0	0	003
MISMATCH 32..17	P	A	B	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	0	F	C	0	0	0	0	1	0	0	0	0	0	004
BIT 16..1	P	A	B	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	0	F	C	0	0	1	0	1	0	0	0	0	0	005
BIT 32..17	P	A	B	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	0	F	C	0	0	0	1	1	0	0	0	0	0	006
TRIPLE FAULT 16..1	P	A	B	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	0	F	C	0	0	1	1	1	0	0	0	0	0	007
TRIPLE FAULT 32..17	P	A	B	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	0	F	C	0	0	0	0	0	1	0	0	0	0	010
TRIPLE DATA 16..1	P	A	B	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	0	F	C	0	0	1	0	0	1	0	0	0	0	011
TRIPLE DATA 32..17	P	A	B	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	0	F	C	0	0	0	1	0	1	0	0	0	0	012
TEST 5's	P	1	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	F	C	0	0	1	1	0	1	0	0	0	0	013
TEST A's	P	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	F	C	0	0	0	0	1	1	0	0	0	0	014

Notes:
A B = 0 0 IF NO MAJOR FAULTS.
A B = 1 1 IF MAJOR FAULTS EXIST (DATA IS BAD).
C = 0 WHEN 429 DATA RATE IS 100KPBS; C=1 WHEN DATA RATE IS 12.5 KBPS.
D = DATA BIT.
F = 1 IF THE DISCRETE INTERFACE OUTPUT HAS ANY MAJOR FAULT (429 DATA MAY STILL BE GOOD).
P = ARINC 429 PARITY BIT.
THE 12 WORDS ARE TRANSMITTED IN ORDER SHOWN FROM TOP TO BOTTOM.

FIGURE 7. ARINC BIT DESCRIPTION

OPTIONAL 429 LINE DRIVER

If you choose the 429 option for the DD-03232, you can use a line driver chip to transmit the data on the serial data bus. DDC has a device called the DD-03182 which will support ARINC 429, 571 and 575 bus standards.

The serial data is presented on DATA(A) & Data(B) inputs in a dual rail format. The driver is enabled by the SYNC & CLOCK inputs. The output voltage level is programmed by the V_{REF} input & is normally tied to +5VDC along with V_1 to produce output levels of +5V, 0V, and -5V on each output for 10V differential outputs. (See FIGURE 8)

The output resistance is 75 Ohms ±20%; 37.5 Ohms on each output. The outputs are fused for fail safe protection against shorts to aircraft power. The output slew rate is controlled by external timing capacitors on C_A & C_B. Typical Values are 75 pF for 100 KHz data & 500 pF for 12.5 KHz data.

DD-03182 PIN DESCRIPTION

Pin 1: V_{REF} (Input) - The voltage on V_{REF} sets the output voltage levels on A_{OUT} & B_{OUT}. The output logic levels swing between +V_{REF} volts, 0 volts and -V_{REF} volts.

Pins 2, 10: N/C - No Connect

Pin 3: SYNC (Input) - Logic 0 outputs will be forced to NULL or MARK state. Logic 1 enables data transmission.

Pin 14: CLOCK (Input) - Logic 0 outputs will be forced to NULL or MARK state. Logic 1 enables data transmission.

Pins 4, 13: DATA(A)/DATA(B) (Inputs) - These signals contain the serial data to be transmitted on the ARINC 429 data bus.

Pins 5, 12: C_A/C_B (Analog) - External timing capacitors are tied from these points to ground to establish the output signal slew rate. Typically, C_A=C_B=75 pF for 100 KHz data and C_A=C_B=500 pF for 12.5 KHz data.

Pins 6, 11: A_{OUT}/B_{OUT} (Output) - These are the line driver outputs which are connected to the aircraft serial data bus.

Pin 7: -V (Input) - This is the negative supply input (-15VDC nominal).

Pin 8: Gnd - Ground

Pin 9: +V (Input) This is the positive supply input (+15VDC nominal).

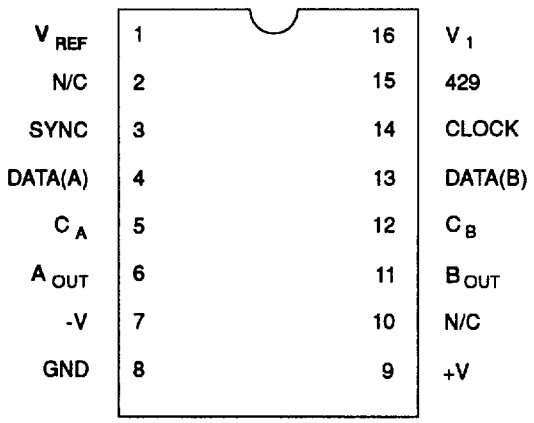
Pin 15: 429 (Input) - Tie to +5V.

Pin 16: V_1(Input) This is the logic supply input (+5VDC nominal).

DD-03182 SPECIFICATIONS

PARAMETER	UNITS	MIN	TYP	MAX
ABSOLUTE MAXIMUM RATINGS				
VOLTAGE BETWEEN PINS				
■ +V & -V	V			40
■ V_1 & GND	V			7
■ V_{REF} & GND	V			6
POWER SUPPLY REQUIREMENTS				
■ +V	VDC	10.5	15	16.5
■ -V	VDC	-10.5	-15	-16.5
■ V_1	VDC	4.75	5	5.25
■ V_{REF}	VDC	4.75	5	5.25
THERMAL				
Operating Temperature	°C	-55		+125
Storage Temperature	°C	-65		+150
Lead Temperature (localized, 10 sec duration)	°C			+300

TOP VIEW



DD-03182 PIN OUT

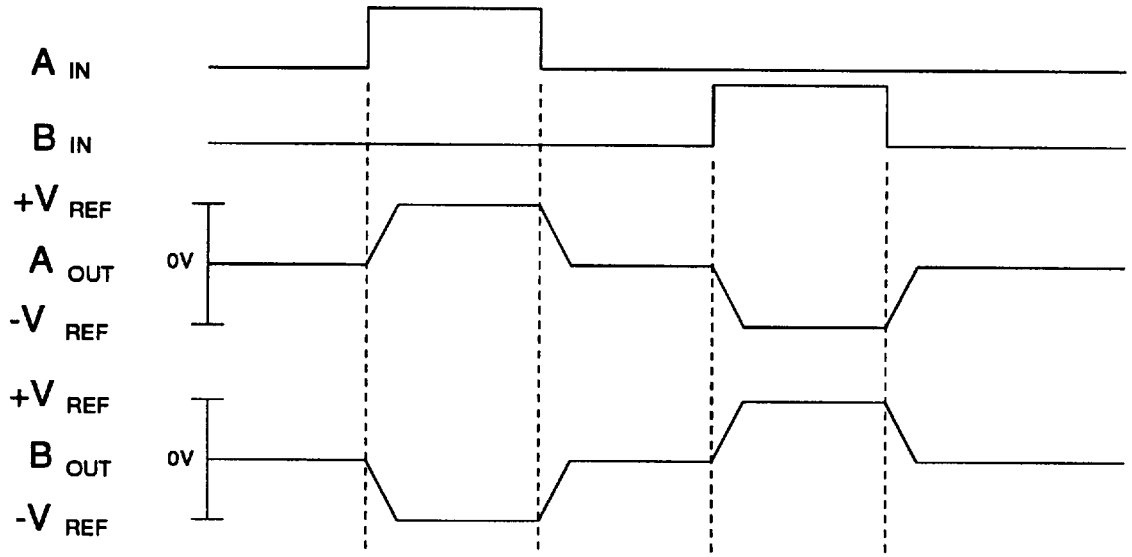
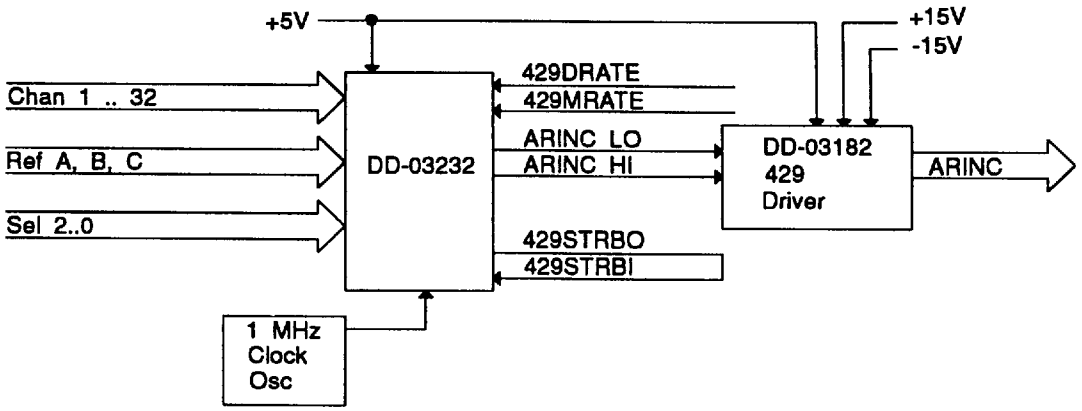


FIGURE 8. ARINC 429 WAVEFORM



NOTE: 1) 429 MRATE and DRATE can either be tied to GND or +5V (Refer to Page 8).

2) If the ARINC 429 option is not used, then pin 104 (429STRBI) MUST be grounded for the "bounce" circuit to operate properly.

FIGURE 9. DD-03232 TO ARINC 429 INTERFACE

TABLE 5. DD-03232 PIN FUNCTION					
PIN NUMBER	**FUNCTION**	**PIN NUMBER**	**FUNCTION**	**PIN NUMBER**	**FUNCTION**
1(Note 1)	429DRATE	37	CHAN 11 INPUT	73	8/16 BITS
2(Note 1)	429STRBO	38	CHAN 12 INPUT	74	D15
3(Note 1)	429MRATE	39	CHAN 13 INPUT	75 (Note 5)	GND (DIGITAL)
4	SEL0	40	CHAN 14 INPUT	76	D14
5	SEL1	41	CHAN 15 INPUT	77	D13
6	SEL2	42	CHAN 16 INPUT	78	D12
7 (Note 5)	V_{DD} (DIGITAL)	43	CHAN 17 INPUT	79	D11
8 (Note 5)	V_{DD} (DIGITAL)	44	CHAN 18 INPUT	80	D10
9 (Note 5)	V_{DD} (DIGITAL)	45	CHAN 19 INPUT	81	D9
10 (Note 5)	V_{DD} (DIGITAL)	46	CHAN 20 INPUT	82	D8
11 (Note 5)	V_{DD} (DIGITAL)	47	CHAN 21 INPUT	83	D7
12 (Note 5)	V_{DD} (DIGITAL)	48	CHAN 22 INPUT	84	D6
13 (Note 5)	V_{DD} (DIGITAL)	49	CHAN 23 INPUT	85	D5
14	N/C	50	CHAN 24 INPUT	86	D4
15 (Note 5)	V_{DD} (ANALOG)	51	CHAN 25 INPUT	87	D3
16	TRIM A	52	CHAN 26 INPUT	88	D2
17	REF A	53	CHAN 27 INPUT	89	D1
18	TRIM C	54	CHAN 28 INPUT	90	D0
19	REF C	55	CHAN 29 INPUT	91	A5
20	TRIM B	56	CHAN 30 INPUT	92	A4
21	REF B	57	N/C	93	A3
22 (Note 3)	$\overline{\text{TMODE}}$	58	N/C	94	A2
23 (Note 3)	$\overline{\text{TMUX}}$	59	CHAN 31 INPUT	95	A1
24 (Note 2)	$\overline{\text{RESET}}$	60	N/C	96	A0
25	CHAN 1 INPUT	61	CHAN 32 INPUT	97	$\overline{\text{ENABLE}}$
26	CHAN 2 INPUT	62	N/C	98	READY
27	N/C	63	N/C	99	$\overline{\text{FAULT}}$
28	N/C	64	N/C	100 (Note 3)	$\overline{\text{FMUX}}$
29	CHAN 3 INPUT	65	N/C	101 (Note 3)	$\overline{\text{FMODE}}$
30	CHAN 4 INPUT	66 (Note 5)	GND (DIGITAL)	102 (Note 1)	ARINC_LO
31	CHAN 5 INPUT	67 (Note 5)	GND (DIGITAL)	103 (Note 1)	ARINC_HI
32	CHAN 6 INPUT	68 (Note 5)	GND (DIGITAL)	104 (Note 4)	429STRBI
33	CHAN 7 INPUT	69 (Note 5)	GND (DIGITAL)	105	1 MHz CLK
34	CHAN 8 INPUT	70 (Note 5)	GND (ANALOG)	106 (Note 2)	CLKTEST
35	CHAN 9 INPUT	71 (Note 5)	GND (DIGITAL)		
36	CHAN 10 INPUT	72 (Note 5)	GND (DIGITAL)		

Note 1: If ARINC 429 Port option is NO, these pins are RESERVED (DO NOT CONNECT TO THESE PINS).
Note 2: DO NOT CONNECT.
Note 3: These signals should be tied to +5V.
Note 4: **This pin must be grounded if 429 option is not implemented.**
Note 5: V_{DD} (Digital) and V_{DD} (Analog) MUST be connected to th same power source;
GND (Digital) and GND (Analog) MUST be connected to the same GND potential.

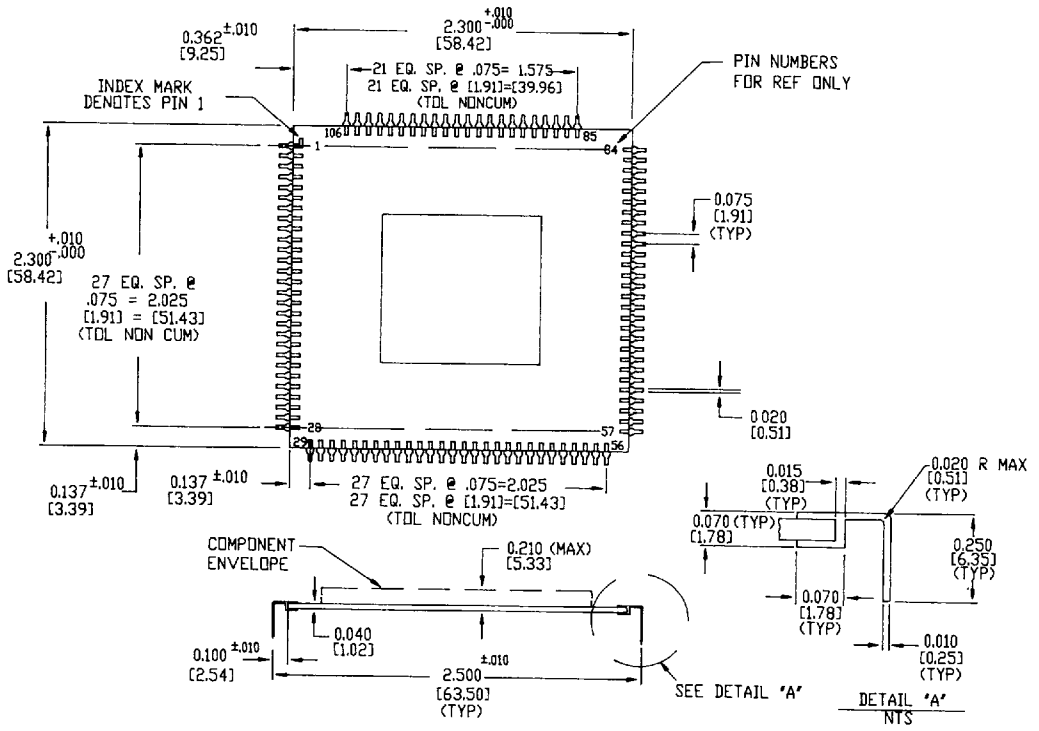


FIGURE 10. DD-03232 PLUG-IN PACKAGE MECHANICAL OUTLINE

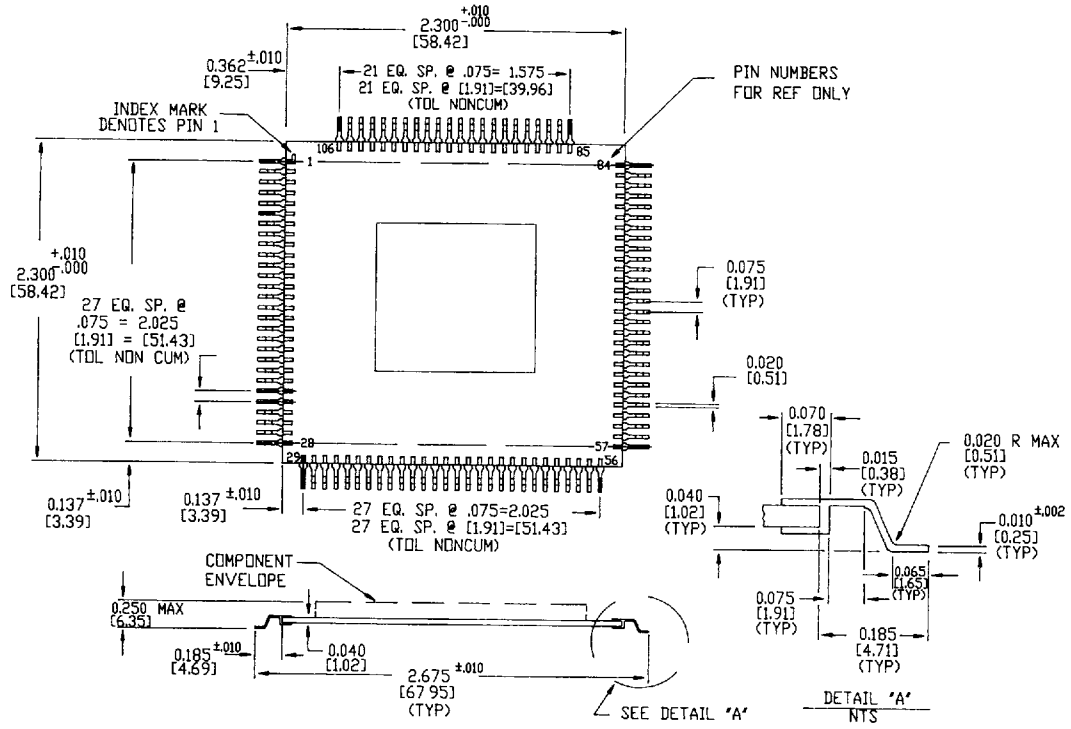


FIGURE 11. DD-03232 SURFACE MOUNT PACKAGE MECHANICAL OUTLINE

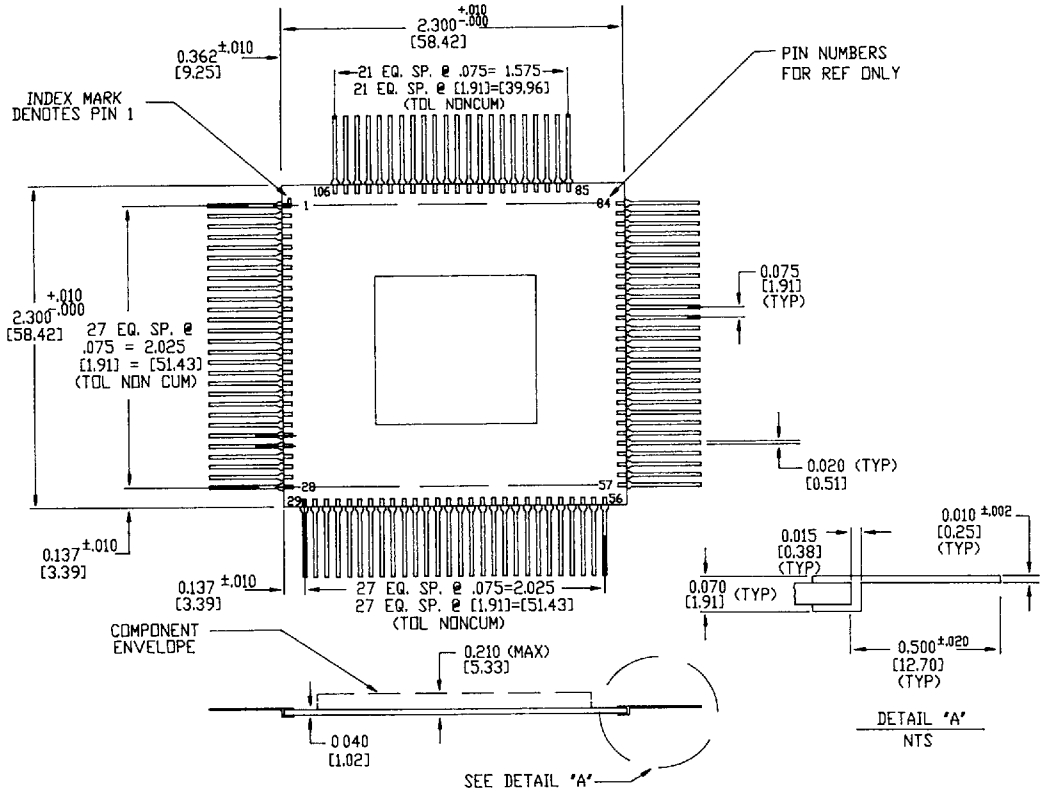


FIGURE 12. DD-03232 UNFORMED LEADS PACKAGE MECHANICAL OUTLINE

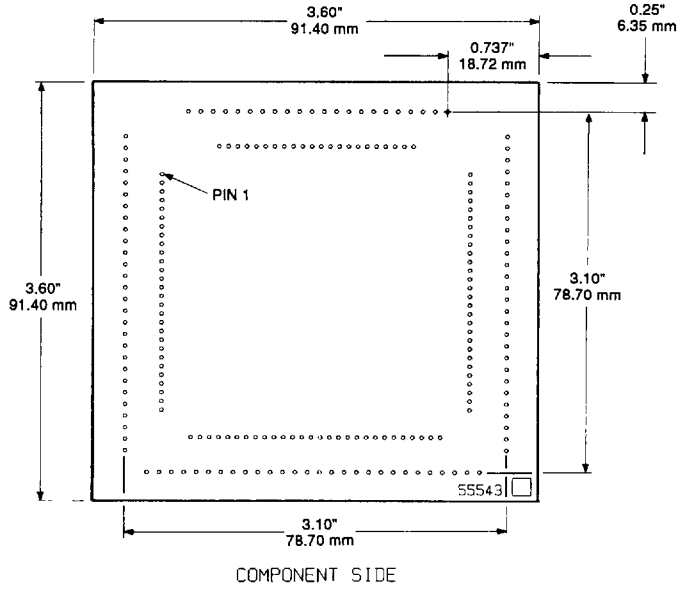


FIGURE 13. DD-03200 ADAPTER BOARD MECHANICAL OUTLINE

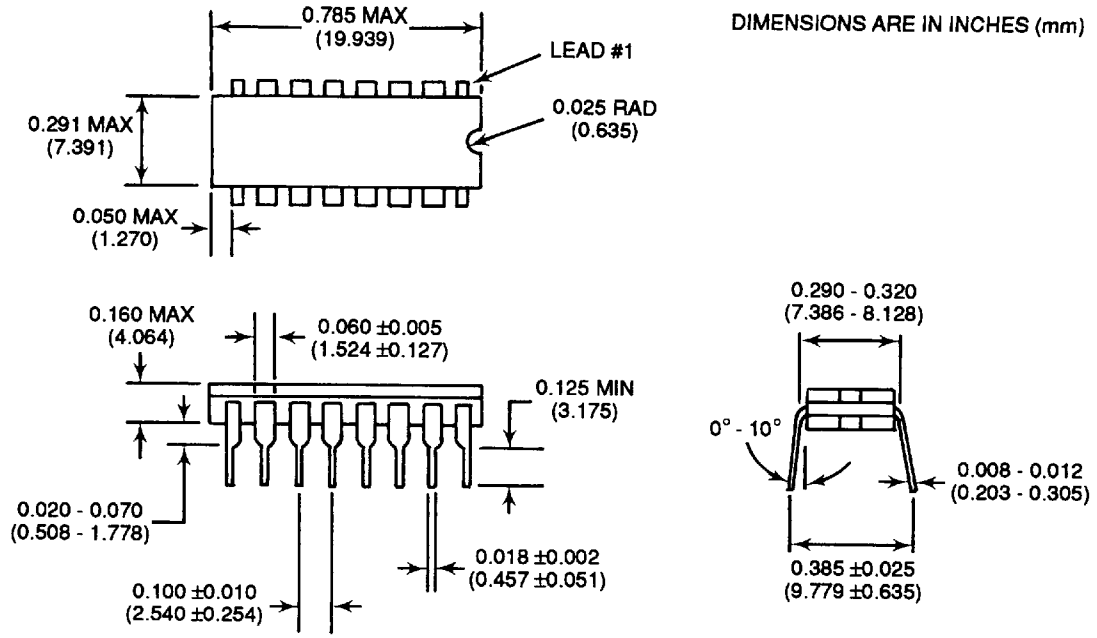


FIGURE 14. DD-03182 CERDIP (JE) MECHANICAL OUTLINE

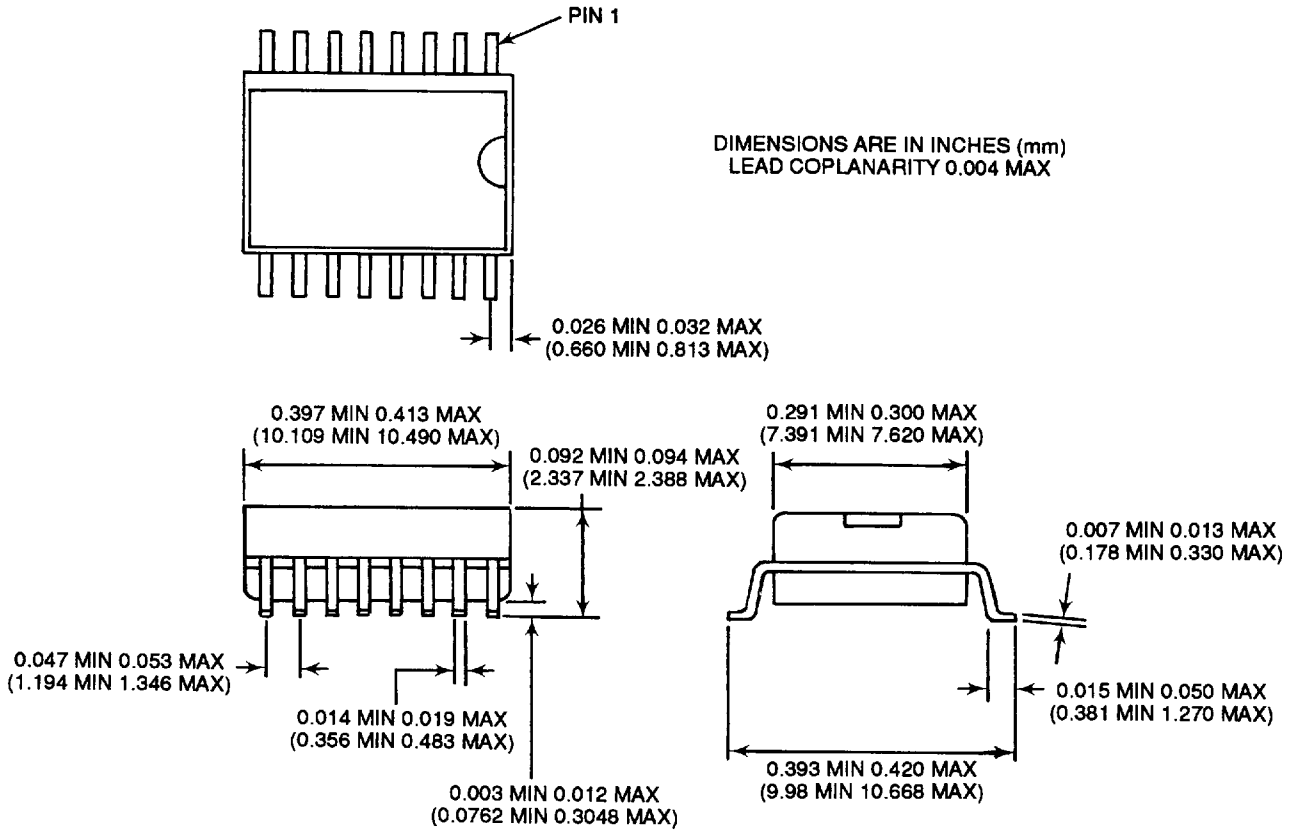


FIGURE 15. DD-03182 SURFACE MOUNT (SOIC) PACKAGE MECHANICAL OUTLINE

ORDERING INFORMATION

DD-03232DP-100

ARINC 429 Port Option:
0 = Without ARINC 429 output
4 = With ARINC 429 output

Screening:
0 = Standard DDC Procedures
1 = Military Processing available (ceramic only)
2 = Burn-in (ceramic only)

Temperature Range:
1 = –55 to +125 °C (ceramic only)
2 = –40 to +85 °C
3 = 0 to +70 °C

ASIC Package Type:
P = Plastic
C = Ceramic

Package Style:
D = Plug-in
F = Surface Mount
U = Unformed Leads

OPTIONAL HARDWARE

DD-03182DP-100 — ARINC 429 Line Driver

Not Used

Screening:
0 = Standard DDC Procedures
2 = Burn-in (ceramic only)

Temperature Range:
1 = –55 to +125 °C (ceramic only)
3 = 0 to +70 °C

Package Type:
P = Plastic
C = Ceramic

Package Style:
D = CERDIP (ceramic only)
G = Gull Wing (plastic only)

DD-03200 — DD-03232 Socket (Converts 75 mil. centers plug-in to 100 mil. centers plug-in)

OTHER APPLICABLE DOCUMENTS

RTCA/DO-160C: Environmental Conditions and Test Procedure for Airborne Equipment.

MIL-STD-883: Test Methods & Procedures for Microelectronics.

DDC
ILC DATA DEVICE CORPORATION®

105 Wilbur Place, Bohemia, New York 11716

For technical support: 1-800-DDC-1772, ext. 7384 or 7402 (outside N.Y.)
1-800-245-3413, ext. 7384 or 7402 (in Canada)
Headquarters - Tel: (516) 567-5600, ext. 7384 or 7402,
Fax: (516) 567-7358
West Coast - Tel: (714) 895-9777, Fax: (714) 895-4988
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