

FINAL



Advanced  
Micro  
Devices

# Am27X2048

2 Megabit (131,072 x 16-Bit) CMOS ExpressROM™ Device

## DISTINCTIVE CHARACTERISTICS

- **As an OTP EPROM alternative:**
  - Factory optimized programming
  - Fully tested and guaranteed
- **As a Mask ROM alternative:**
  - Shorter leadtime
  - Lower volume per code
- **Fast access time**
  - 100 ns
- **Single +5 V power supply**
- **Compatible with JEDEC-approved EPROM pinout**
- **±10% power supply tolerance**
- **High noise immunity**
- **Low power dissipation**
  - 100  $\mu$ A maximum CMOS standby current
- **Available in Plastic Dual In-Line Package (PDIP) and Plastic Leaded Chip Carrier (PLCC)**
- **Latch-up protected to 100 mA from -1 V to  $V_{CC} + 1$  V**
- **Versatile features for simple interfacing**
  - Both CMOS and TTL input/output compatibility
  - Two line control functions

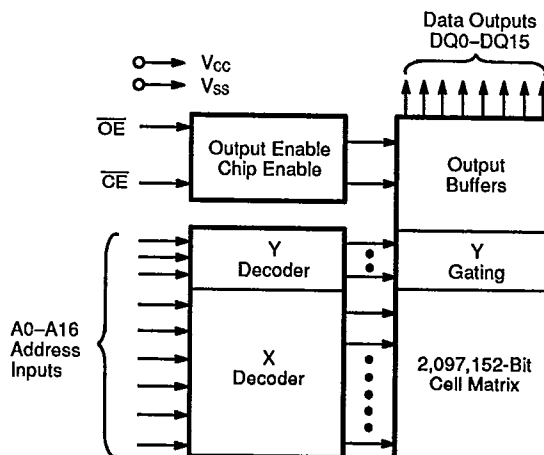
## GENERAL DESCRIPTION

The Am27X2048 is a factory programmed and tested OTP EPROM. It is programmed after packaging prior to final test. Every device is rigorously tested under AC and DC operating conditions to your stable code. It is organized as 131,072 by 16 bits and is available in plastic dual in-line (PDIP) as well as plastic leaded chip carrier (PLCC) packages. ExpressROM devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufacturers a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs.

Access times as fast as 100 ns allow operation with high-performance microprocessors with reduced WAIT states. The Am27X2048 offers separate Output Enable ( $\overline{OE}$ ) and Chip Enable ( $\overline{CE}$ ) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 125 mW in active mode, and 100  $\mu$ W in standby mode.

## BLOCK DIAGRAM



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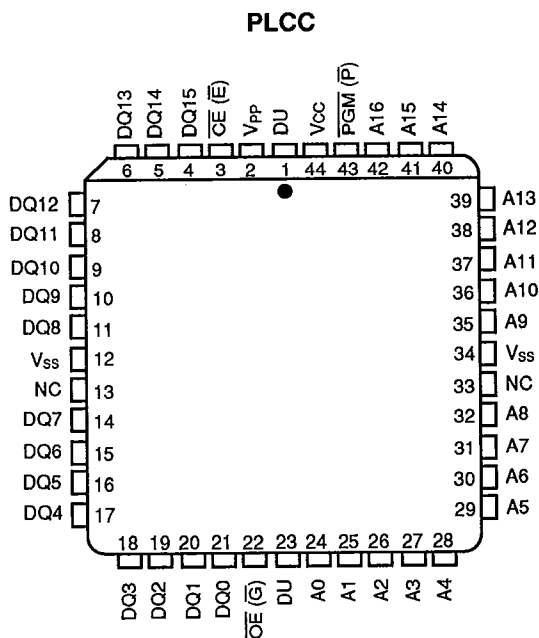
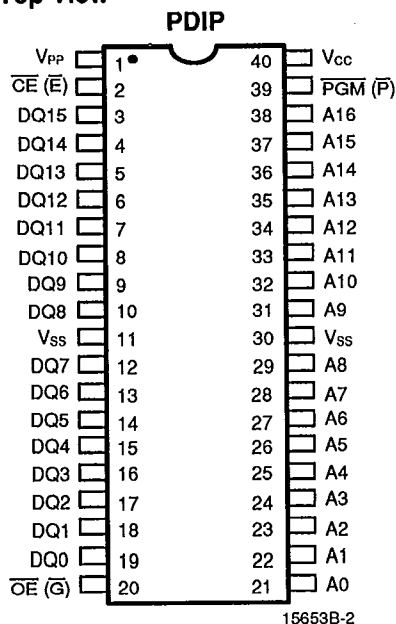


## PRODUCT SELECTOR GUIDE

Family Part No.	Am27X2048				
Ordering Part No:					
V <sub>CC</sub> ±5%	-105	-125			-255
V <sub>CC</sub> ±10%	-100	-120	-150	-200	
Max Access Time (ns)	100	120	150	200	250
$\overline{OE}$ (E) Access (ns)	100	120	150	200	250
$\overline{OE}$ (G) Access (ns)	50	50	65	75	100

## CONNECTION DIAGRAMS

### Top View



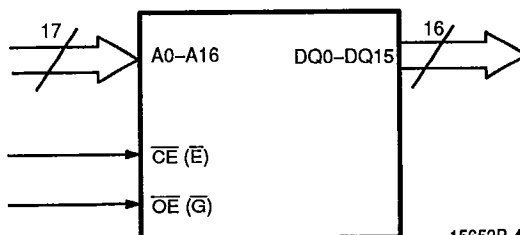
### Note:

1. JEDEC nomenclature is in parentheses.

## PIN DESIGNATIONS

A0-A16	= Address Inputs
$\overline{CE}$ (E)	= Chip Enable Input
DQ0-DQ15	= Data Inputs/Outputs
DU	= No External Connection (Do Not Use)
NC	= No Internal Connection
$\overline{OE}$ (G)	= Output Enable Input
$\overline{PGM}$ (P)	= Program Enable Input
V <sub>CC</sub>	= V <sub>CC</sub> Supply Voltage
V <sub>PP</sub>	= Program Supply Voltage
V <sub>SS</sub>	= Ground

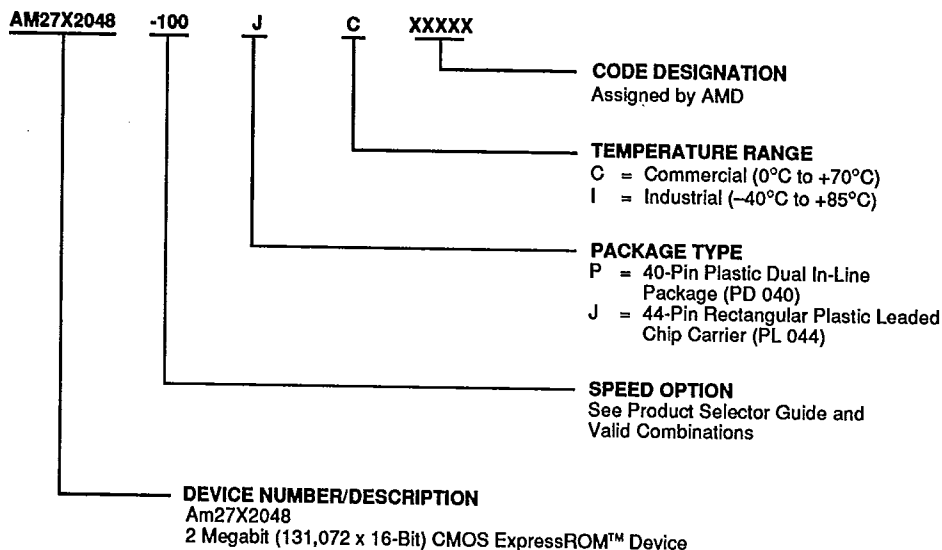
## LOGIC SYMBOL



## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM27X2048-100	PC, JC, PI, JI
AM27X2048-105	
AM27X2048-120	
AM27X2048-125	
AM27X2048-150	
AM27X2048-200	
AM27X2048-255	

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.



## FUNCTIONAL DESCRIPTION

### Read Mode

The Am27X2048 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ( $\overline{CE}$ ) is the power control and should be used for device selection. Output Enable ( $\overline{OE}$ ) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time ( $t_{ACC}$ ) is equal to the delay from  $\overline{CE}$  to output ( $t_{CE}$ ). Data is available at the outputs  $t_{OE}$  after the falling edge of  $\overline{OE}$ , assuming that  $\overline{CE}$  has been LOW and addresses have been stable for at least  $t_{ACC} - t_{OE}$ .

### Standby Mode

The Am27X2048 has a CMOS standby mode which reduces the maximum  $V_{CC}$  current to 100  $\mu A$ . It is placed in CMOS-standby when  $\overline{CE}$  is at  $V_{CC} \pm 0.3 V$ . The Am27X2048 also has a TTL-standby mode which reduces the maximum  $V_{CC}$  current to 1.0 mA. It is placed in TTL-standby when  $\overline{CE}$  is at  $V_{IH}$ . When in standby mode, the outputs are in a high-impedance state, independent of the  $\overline{OE}$  input.

### Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power dissipation
- Assurance that output bus contention will not occur

It is recommended that  $\overline{CE}$  be decoded and used as the primary device-selecting function, while  $\overline{OE}$  be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

### System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1  $\mu F$  ceramic capacitor (high frequency, low inherent inductance) should be used on each device between  $V_{CC}$  and  $V_{SS}$  to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on ExpressROM device arrays, a 4.7  $\mu F$  bulk electrolytic capacitor should be used between  $V_{CC}$  and  $V_{SS}$  for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

## MODE SELECT TABLE

Mode	Pins	$\overline{CE}$	$\overline{OE}$	PGM	$V_{PP}$	Outputs
Read		$V_{IL}$	$V_{IL}$	X	X	DOUT
Output Disable		X	$V_{IH}$	X	X	Hi-Z
Standby (TTL)		$V_{IH}$	X	X	X	Hi-Z
Standby (CMOS)		$V_{CC} \pm 0.3 V$	X	X	X	Hi-Z

#### Note:

1. X = Either  $V_{IH}$  or  $V_{IL}$

**ABSOLUTE MAXIMUM RATINGS**

Storage Temperature	
OTP Products	-65°C to +125°C
All Other Products	-65°C to +150°C
Ambient Temperature	
with Power Applied	-55°C to +125°C
Voltage with Respect to $V_{SS}$	
All pins except $V_{CC}$	-0.6 V to $V_{CC} + 0.6$ V
$V_{CC}$	-0.6 V to +7.0 V

**Note:**

1. Minimum DC voltage on input or I/O pins is -0.5 V. During transitions, the inputs may overshoot  $V_{SS}$  to -2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is  $V_{CC} + 0.5$  V which may overshoot to  $V_{CC} + 2.0$  V for periods up to 20 ns.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

**OPERATING RANGES****Commercial (C) Devices**

Case Temperature ( $T_C$ ) ..... 0°C to +70°C

**Industrial (I) Devices**

Case Temperature ( $T_C$ ) ..... -40°C to +85°C

**Supply Read Voltages**

$V_{CC}$  for Am27X2048-XX5 .... +4.75 V to +5.25 V

$V_{CC}$  for Am27X2048-XX0 .... +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.



# DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 2 and 4)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -400 \mu A$	2.4		V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 2.1 \text{ mA}$		0.45	V
$V_{IH}$	Input HIGH Voltage		2.0	$V_{CC} + 0.5$	V
$V_{IL}$	Input LOW Voltage		-0.5	+0.8	V
$I_{LI}$	Input Load Current	$V_{IN} = 0 \text{ V to } +V_{CC}$		1.0	$\mu A$
$I_{LO}$	Output Leakage Current	$V_{OUT} = 0 \text{ V to } +V_{CC}$		5.0	$\mu A$
$I_{CC1}$	$V_{CC}$ Active Current (Note 3)	$\overline{CE} = V_{IL}$ , $f = 5 \text{ MHz}$ , $I_{OUT} = 0 \text{ mA}$		50	mA
$I_{CC2}$	$V_{CC}$ TTL Standby Current	$\overline{CE} = V_{IH}$		1.0	mA
$I_{CC3}$	$V_{CC}$ CMOS Standby Current	$\overline{CE} = V_{CC} \pm 0.3 \text{ V}$		100	$\mu A$

## Notes:

- $V_{CC}$  must be applied simultaneously or before  $V_{PP}$ , and removed simultaneously or after  $V_{PP}$ .
- Caution:** The Am27X2048 must not be removed from (or inserted into) a socket when  $V_{CC}$  or  $V_{PP}$  is applied.
- $I_{CC1}$  is tested with  $\overline{CE} = V_{IH}$  to simulate open outputs.
- Minimum DC Input Voltage is -0.5 V. During transitions, the inputs may overshoot to -2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is  $V_{CC} + 0.5 \text{ V}$ , which may overshoot to  $V_{CC} + 2.0 \text{ V}$  for periods less than 20 ns.

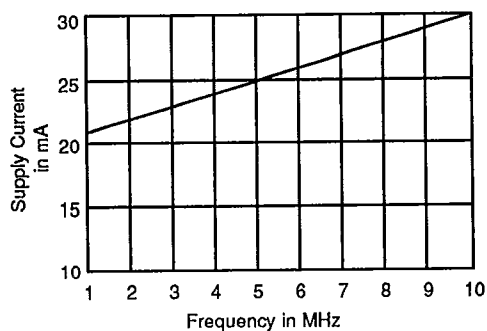


Figure 1. Typical Supply Current  
vs. Frequency  
 $V_{CC} = 5.5 \text{ V}$ ,  $T = 25^\circ\text{C}$

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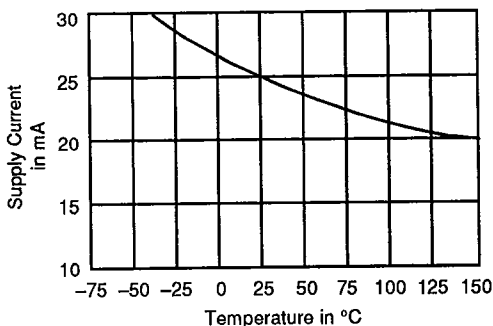


Figure 2. Typical Supply Current  
vs. Temperature  
 $V_{CC} = 5.5 \text{ V}$ ,  $f = 5 \text{ MHz}$

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**CAPACITANCE**

Parameter Symbol	Parameter Description	Test Conditions	PD 040		PL 044		Unit
			Typ	Max	Typ	Max	
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0 V	10	12	7	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0 V	12	15	12	14	pF

**Notes:**

1. This parameter is only sampled and not 100% tested.
2. T<sub>A</sub> = +25°C, f = 1 MHz.

**SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 3, and 4)**

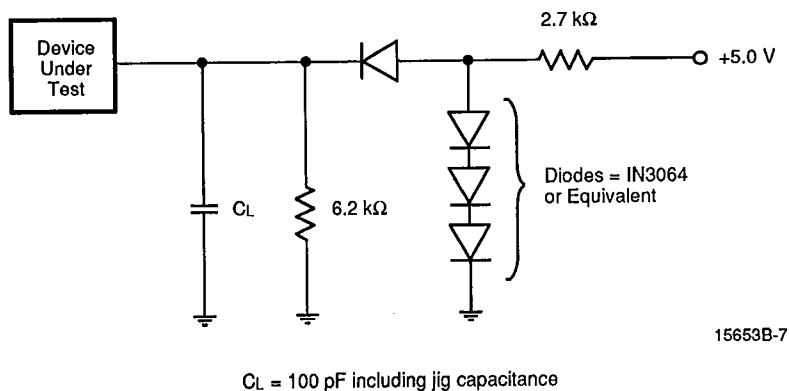
Parameter Symbols		Parameter Description	Test Conditions	Am27X2048					Unit
JEDEC	Standard			-100 -105	-120 -125	-150	-200	-255	
tAVQV	tACC	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$	Min	—	—	—	—	ns
				Max	100	120	150	200 250	
tELQV	tCE	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Min	—	—	—	—	ns
				Max	100	120	150	200 250	
tGLQV	tOE	Output Enable to Output Delay	$\overline{OE} = V_{IL}$	Min	—	—	—	—	ns
				Max	50	50	55	60 75	
tEHQZ	tdF (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min	0	0	0	0	ns
tGHQZ				Max	30	30	30	40 60	
tAXQX	tOH	Output Hold from Addresses, $\overline{CE}$ , or $\overline{OE}$ , whichever occurred first		Min	0	0	0	0	ns
				Max	—	—	—	—	

**Notes:**

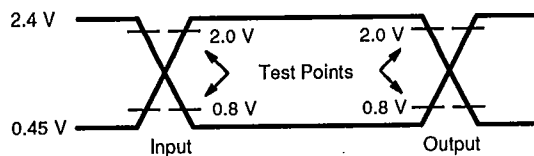
1. V<sub>CC</sub> must be applied simultaneously or before V<sub>PP</sub>, and removed simultaneously or after V<sub>PP</sub>.
2. This parameter is only sampled and not 100% tested.
3. **Caution:** The Am27X2048 must not be removed from (or inserted into) a socket or board when V<sub>PP</sub> or V<sub>CC</sub> is applied.
4. Output Load: 1 TTL gate and C<sub>L</sub> = 100 pF  
 Input Rise and Fall Times: 20 ns  
 Input Pulse Levels: 0.45 V to 2.4 V  
 Timing Measurement Reference Level: 0.8 V and 2 V for inputs and outputs



## SWITCHING TEST CIRCUIT



## SWITCHING TEST WAVEFORM





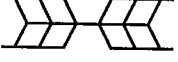


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AC Testing: Inputs are driven at 2.4 V for a Logic "1" and 0.45 V for a Logic "0." Input pulse rise and fall times are  $\leq 20$  ns.

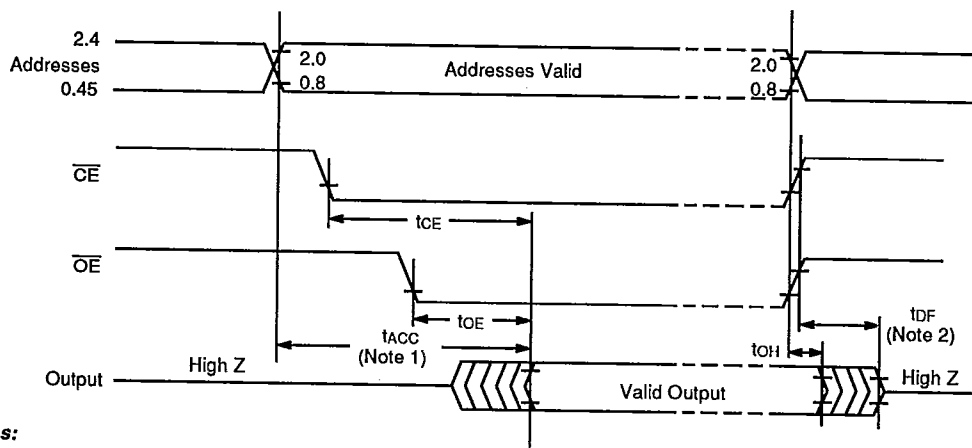


## KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

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## SWITCHING WAVEFORMS

**Notes:**

- $\overline{OE}$  may be delayed up to  $t_{ACC} - t_{OE}$  after the falling edge of the addresses without impact on  $t_{ACC}$ .
- $t_{DF}$  is specified from  $\overline{OE}$  or  $\overline{CE}$ , whichever occurs first.

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