TC55V328AJ-15/17/20

SILICON GATE CMOS

32,768 WORD x 8 BIT CMOS STATIC RAM

Description

The TC55V328AJ is a 262,144 bits high speed static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operated from a single 3.3-volt supply. Toshiba's CMOS technology and advanced circuit form provide low voltage operation and high speed feature.

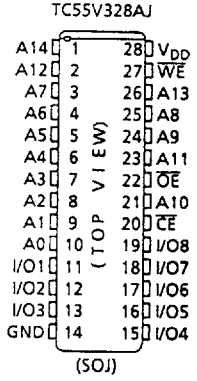
The TC55V328AJ has low power feature with device control using Chip Enable ($\overline{CE}$) and has an Output Enable Input ($\overline{OE}$) for fast memory access. The TC55V328AJ is suitable for use in cache memory where high speed is required, and high speed storage. All inputs and outputs are LVTTL compatible.

The TC55V328AJ is packaged in a 28-pin standard SOJ with 300mil width for high density surface assembly.

Features

- Fast access time
  - TC55V328AJ-15 15ns (max.)
  - TC55V328AJ-17 17ns (max.)
  - TC55V328AJ-20 20ns (max.)
- Low power dissipation
  - Operation:
  - TC55V328AJ-15 100mA (max.)
  - TC55V328AJ-17 100mA (max.)
  - TC55V328AJ-20 90mA (max.)
  - Standby: 300μA (max.)
- Fully static operation
- 3.3V single power supply: 3.3V ±0.3V
- Output buffer control: $\overline{OE}$
- All inputs and outputs:
  - LVTTL compatible
- Package:
  - TC55V328AJ: SOJ28-P-300A

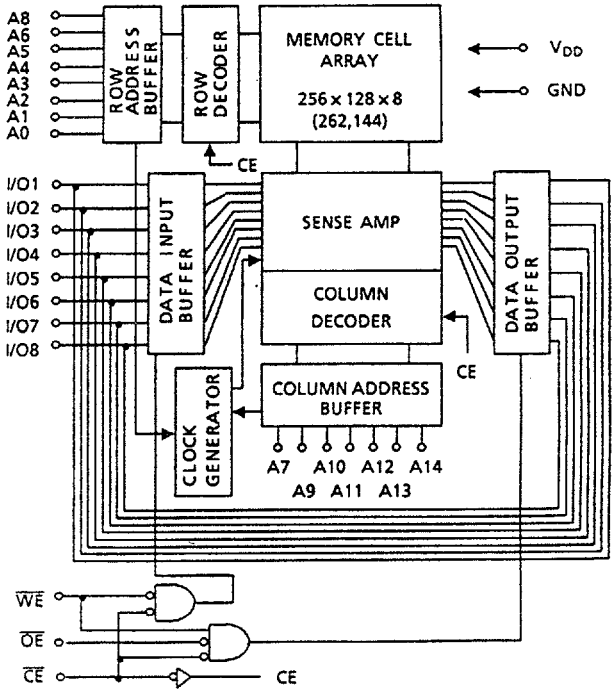
Pin Connection (Top View)



Pin Names

A0 ~ A14	Address Inputs
I/O1 ~ I/O8	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+3.3V)
GND	Ground

Block Diagram



Operating Mode

OPERATION MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O1 ~ I/O8	POWER
Read	L	L	H	Output	I_{DDO}
Write	L	*	L	Input	I_{DDO}
Output Disable	L	H	H	High Impedance	I_{DDO}
Standby	H	*	*	High Impedance	I_{DDS}

* High or Low

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ~ 4.6	V
V_{IN}	Input Voltage	-0.5* ~ 4.6	V
$V_{I/O}$	Input/Output Voltage	-0.5* ~ V_{DD} + 0.5**	V
P_D	Power Dissipation	0.5	W
T_{SOLDER}	Soldering Temperature (10s)	260	°C
T_{STRG}	Storage Temperature	-65 ~ 150	°C
T_{OPR}	Operating Temperature	-10 ~ 85	°C

* -2.0V with a pulse width of 10ns
** V_{DD} + 1.5V with a pulse width of 10ns

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.0	–	V_{DD} + 0.3**	V
V_{IL}	Input Low Voltage	-0.3*	–	0.8	V

* -1.5V with a pulse width of 10ns
**V_{DD} + 1.0V with a pulse width of 10ns

DC and Operating Characteristics (Ta = 0 ~ 70°C, V_{DD} = 3.3V±0.3V)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}		–	–	±1	µA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, V_{OUT} = 0 ~ V_{DD}		–	–	±1	µA
V_{OH}	Output High Voltage	I_{OH} = -2mA		2.4	–	–	V
		I_{OH} = -100µA		V_{DD} - 0.2	–	–	V
V_{OL}	Output Low Voltage	I_{OL} = 2mA		–	–	0.4	V
		I_{OL} = 100µA		–	–	0.2	V
I_{DDO}	Operating Current	t_{cycle} = Min cycle, $\overline{CE}$ = V_{IL} Other Inputs = V_{IH}/V_{IL}, I_{OUT} = 0 mA	-15	–	–	100	mA
			-17	–	–	100	
			-20	–	–	90	
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH} Other Inputs = V_{IH}/V_{IL}, t_{cycle} = Min cycle		–	–	20	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} - 0.2V Other Inputs = V_{DD} - 0.2V or 0.2V		–	–	300	µA

Capacitance (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = GND	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 3.3V±0.3V)

Read Cycle

SYMBOL	PARAMETER	TC55V328AJ-15		TC55V328AJ-17		TC55V328AJ-20		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	15	–	17	–	20	–	ns
t_{ACC}	Address Access Time	–	15	–	17	–	20	
t_{CO}	$\overline{CE}$ Access Time	–	15	–	17	–	20	
t_{OE}	$\overline{OE}$ Access Time	–	7	–	7	–	10	
t_{OH}	Output Data Hold Time from Address Change	5	–	5	–	5	–	
t_{COE}	Output Enable Time from $\overline{CE}$	5	–	5	–	5	–	
t_{COD}	Output Disable Time from $\overline{CE}$	–	8	–	8	–	8	
t_{OEE}	Output Enable Time from $\overline{OE}$	1	–	1	–	1	–	
t_{ODO}	Output Disable Time from $\overline{OE}$	–	8	–	8	–	8	

Write Cycle

SYMBOL	PARAMETER	TC55V328AJ-15		TC55V328AJ-17		TC55V328AJ-20		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	15	–	17	–	20	–	ns
t_{WP}	Write Pulse Width	10	–	10	–	13	–	
t_{AW}	Address Valid to End of Write	10	–	10	–	13	–	
t_{CW}	Chip Enable to End of Write	11	–	11	–	13	–	
t_{AS}	Address Setup Time	0	–	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	0	–	
t_{DS}	Data Setup Time	8	–	8	–	10	–	
t_{DH}	Data Hold Time	0	–	0	–	0	–	
t_{OEW}	Output Enable Time from $\overline{WE}$	1	–	1	–	1	–	
t_{ODW}	Output Disable Time from $\overline{WE}$	–	8	–	8	–	8	

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	Fig. 1

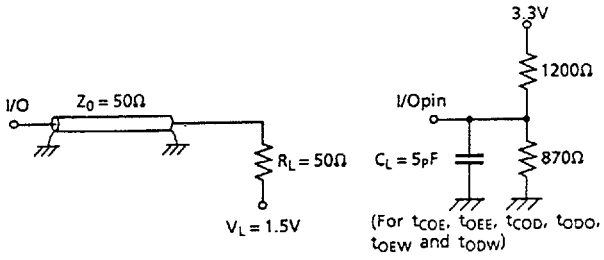
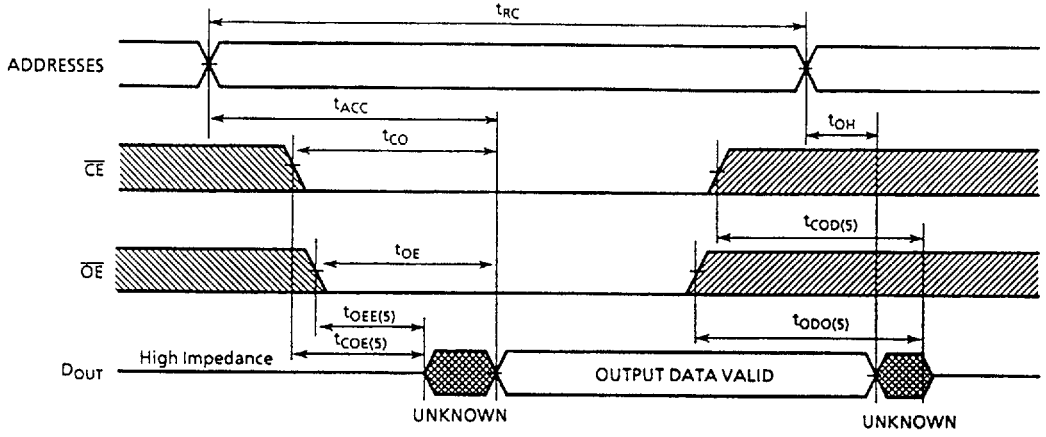


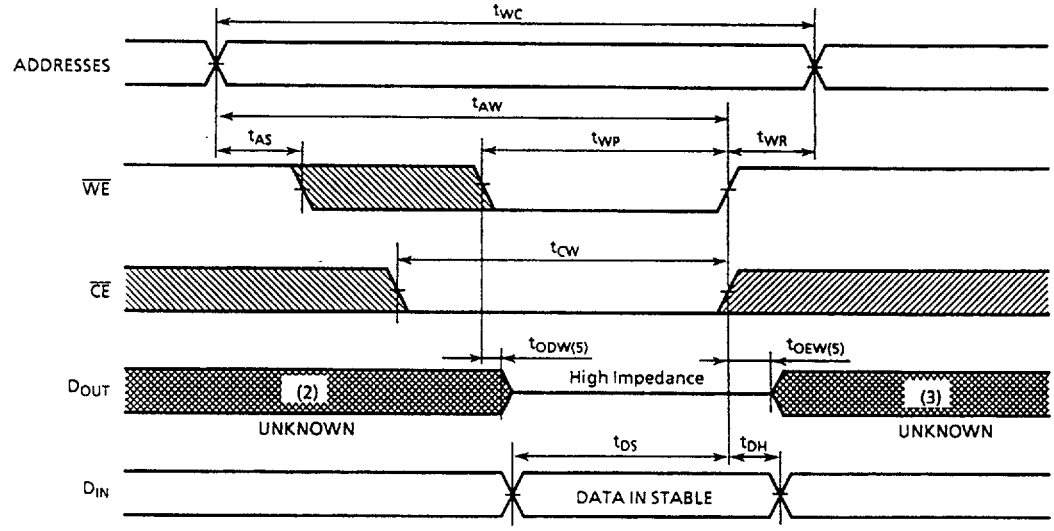
Figure 1.

Timing Waveforms

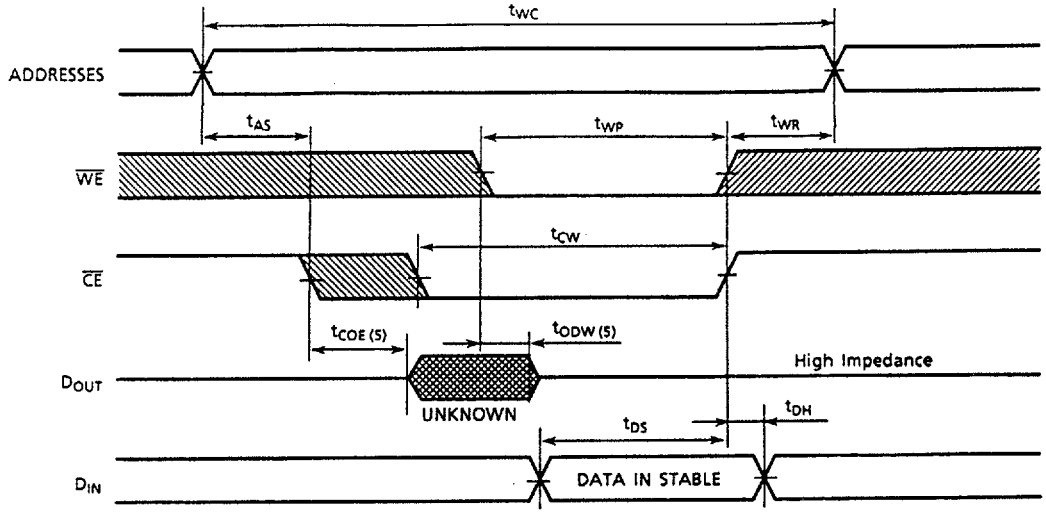
Read Cycle (1)



Write Cycle 1 (4) ($\overline{WE}$ Controlled Write)



Write Cycle 2 [4] ($\overline{CE}$ Controlled Write)



Notes:

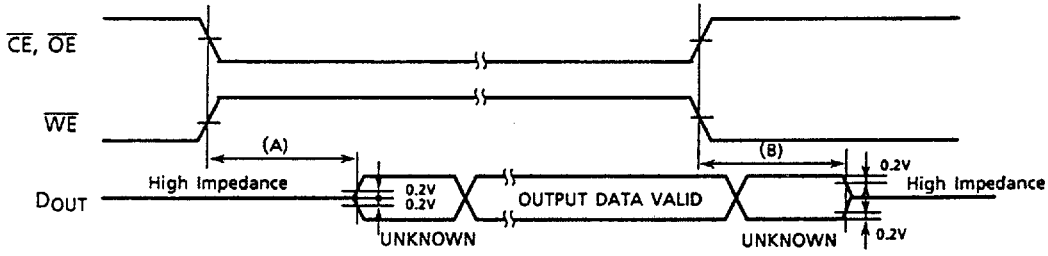
1. $\overline{WE}$ is High for Read Cycle.

2. Assuming that $\overline{CE}$ Low transition occurs coincident with or after the $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to the $\overline{WE}$ High transition, Outputs remain in a high impedance state.

4. Assuming that $\overline{OE}$ is High for a Write Cycle, the Outputs are in a high impedance state during this period.

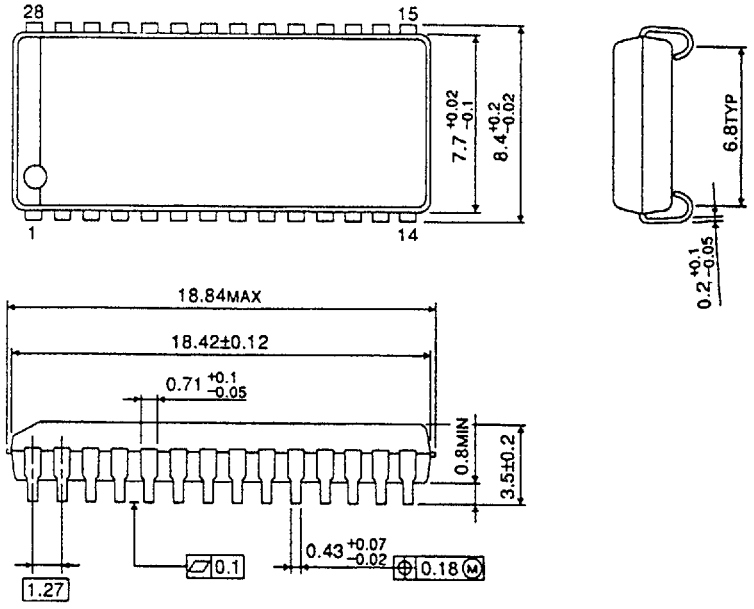
5. These parameters are specified as follows and measured by using the load shown in Figure 1.
   (A) t_{COE}, t_{OEE}, t_{OEW} . . . . Output Enable Time
   (B) t_{COD}, t_{ODO}, t_{ODW} . . . . Output Disable Time



Outline Drawings

Unit in mm

Plastic SOJ (SOJ28-P-300A)



Weight: 083g (Typ.)