iC-DC
## 2-CHANNEL BUCK/BOOST DC/DC CONVERTER

preliminary

iC Haus

FEATURES

Wide input voltage range of +4 to +36 V

Reverse polarity protection up to -36 V with autarky function

Universal buck/boost converter with high efficiency

Two back-end, adjustable linear regulators (1.5 V to 5.5 V) with a total of up to 300 mA of output current and a separate output voltage monitor

Low residual ripple with small capacitors in the µF range

Separate enable inputs for the linear regulators

Two switched linear regulator outputs

Integrated switching transistors and flyback diodes

Converter cut-off current can be set by an external resistor

Integrated 3 MHz oscillator with no external components

Active noise spectrum reduction

Error messaging with overtemperature, overvoltage, and undervoltage at the current-limited open-collector output

Wide temperature range of -40 °C to 125 °C

Protective circuitry against ESD
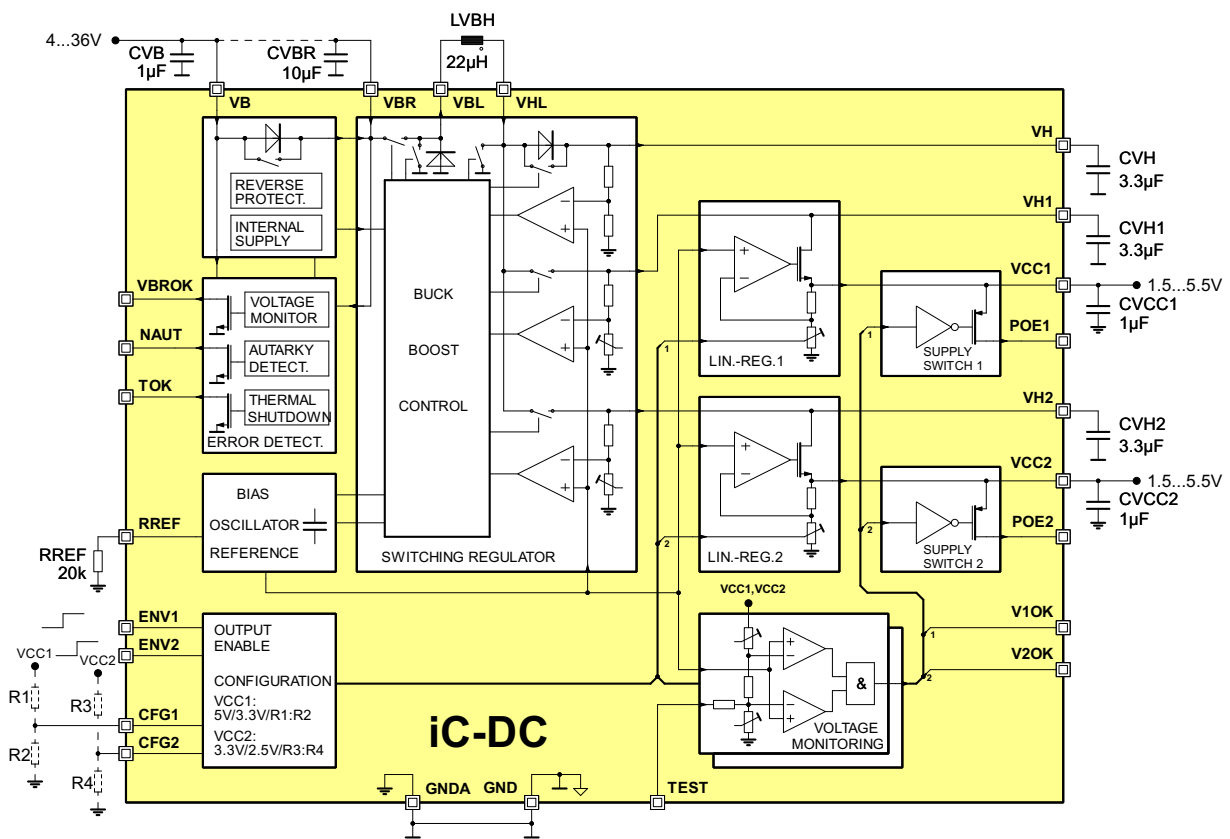
Space saving 24-pin QFN package

APPLICATIONS

Dual voltage supply by buck/boost converters with adjustable, back-end linear regulators

Power management for laser, encoder, and automotive applications

PACKAGES
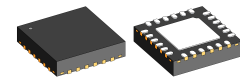
QFN24 4 mm x 4 mm
(RoHS compliant)

BLOCK DIAGRAM

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DESCRIPTION

iC-DC is a monolithic switching converter with two back-end linear regulators. The output voltages of the two linear regulators can be individually pin-configured within a range of 1.5 to 5.5 V. The switching converter supplies up to 300 mA which can be drawn from the two linear regulators in the ratio required.

The intermediate voltages of the two on-chip linear regulators are adjusted to minimize their drop-out voltages. These are approximately 400 mV above the set linear regulator output voltages.

The high efficiency of the buck/boost converter for an input voltage range of +4 V to +36 V makes iC-DC suitable for industrial applications. Using very few external components, a DC/DC power pack can be created with a stabilized supply voltage and minimum power dissipation.

iC-DC is ideal for sensor applications thanks to its minimal power loss, few components, and stabilized supply. Switching transistors, flyback diodes, and an oscillator are integrated in the device so that the only external elements needed are an inductor, the back-up capacitors, and a reference resistor.

The back-end linear regulators have a very low residual ripple with comparatively small filter capacitors in the single-digit µF range.

By using two independent regulators voltages can be decoupled from sensitive analog circuits and driver devices, for example.

The chip temperature, input voltage, and integrated reverse polarity protection are monitored and errors signaled by current-limited open-collector outputs. With overtemperature the switching converter is disabled to reduce the chip's power dissipation.

The linear regulator output voltages are monitored and once having reached the steady state they are also switched to outputs POE1 and POE2. The output voltages of the two linear regulators VCC1 and VCC2 can be switched on and off by two separate inputs.

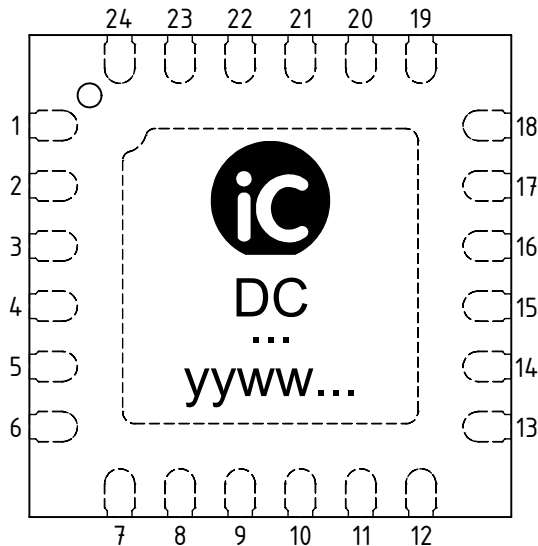The device's standby function can be activated to minimize the current consumption.

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PACKAGES

PIN CONFIGURATION
QFN24-4x4 (4 mm x 4 mm)

PIN FUNCTIONS

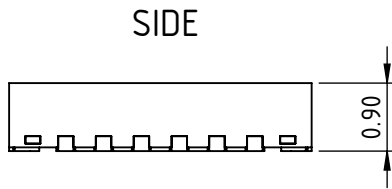| No.	Name	Function
1	RREF	Reference Resistor
2	GNDA	Analog Ground
3	CFG1	VCC1 Configuration 3.3/5.0 V or 1.5 V to 5.5 V with ext. R Divider
4	CFG2	VCC2 Configuration 2.5/3.3 V or 1.5 V to 5.5 V with ext. R Divider
5	TEST	Test Input
6	POE2	Power Output Enable VCC2 Voltage
7	V2OK	Error Output VCC2 Voltage
8	VCC2	1.5 V to 5.5 V Lin. Regulator Output 2
9	VH2	Intermediate Voltage 2 for VCC2 Regulator
10	VH1	Intermediate Voltage 1 for VCC1 Regulator
11	VCC1	1.5 V to 5.5 V Lin. Regulator Output 1
12	V1OK	Error Output VCC1 Voltage
13	POE1	Power Output Enable VCC1 Voltage
14	VH	Intermediate Voltage
15	VHL	Inductor Terminal VH
16	GND	Power Ground
17	VBL	Inductor Terminal VB
18	VBR	Reverse Protected Supply Voltage
19	VB	+4 V to +36 V Supply Voltage
20	ENV1	VCC1 Linear Regulator Activation
21	ENV2	VCC2 Linear Regulator Activation
22	VBROK	Error Output Supply Voltage
23	TOK	Error Output Overtemperature
24	NAUT	Error Output Autarky
	TP	Thermal Pad

The *Thermal Pad* on the underside of the package should be appropriately connected to GND for better heat dissipation (ground plane). GNDA should also be directly connected to neutral point GND. Ground loops should be avoided.

Only the Pin 1 mark on the front or reverse is determinative for package orientation (🄲 DC and code are subject to change).

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PACKAGE DIMENSIONS

RECOMMENDED PCB-FOOTPRINT

3.80
2.49
R0.15
2.49
3.80
0.70
0.50
0.30

SIDE

0.90

TOP

4
4

BOTTOM

2.45
2.45
0.40
0.50
0.25

dra_qfn24-1_pack_1, 10:1

All dimensions given in mm.

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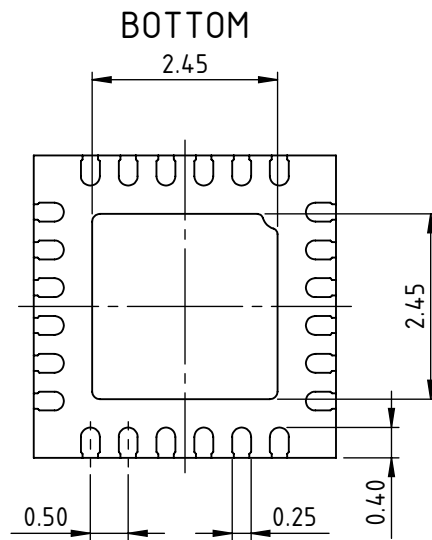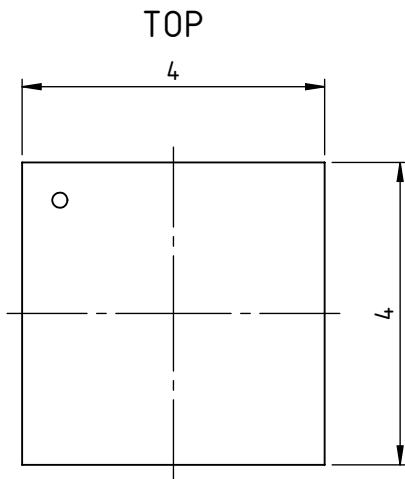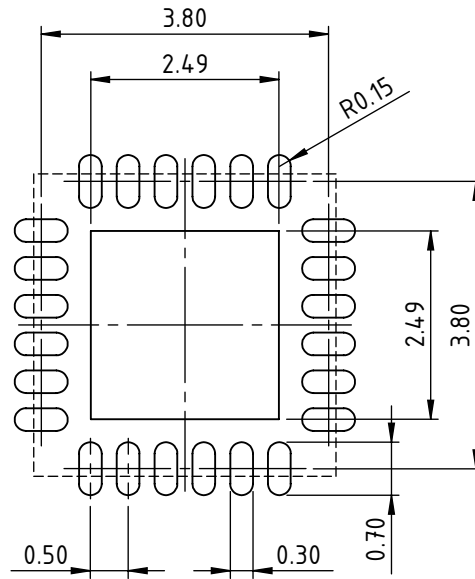
ABSOLUTE MAXIMUM RATINGS

Maximum ratings do not constitute permissible operating conditions; functionality is not guaranteed. Exceeding the maximum ratings can damage the device.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	V()	Voltage at VB		-40	42	V
G002	V()	Voltage at VBR, VBL, ENV1, ENV2		-0.3	42	V
G003	V()	Voltage at VHL, VH, VBROK, NAUT, TOK, TEST		-0.3	8.4	V
G004	V()	Voltage at VH1, VH2		-0.3	6.4	V
G005	V()	Voltage at VCC1, VCC2, V1OK, V2OK, CFG1, CFG2, POE1, POE2, RREF, GNDA		-0.3	5.6	V
G006	I(VB)	Current in VB		-50	800	mA
G007	I(VBR)	Current in VBR		-50	800	mA
G008	I(VBL)	Current in VBL		-800	50	mA
G009	I(VHL)	Current in VHL		-50	800	mA
G010	I()	Current in VH, VH1, VH2, VCC1, VCC2		-500	20	mA
G011	I()	Current in CFG1, CFG2, ENV1, ENV2, V1OK, V2OK, VBROK, NAUT, TOK, POE1, POE2, RREF, TEST, GNDA		-20	20	mA
G012	Vd()	ESD Susceptibility at all pins	HBM, 100 pF discharged through 1.5 kΩ		2	kV
G013	Tj	Chip-Temperature		-40	150	°C
G014	Ts	Storage Temperature Range		-40	150	°C

THERMAL DATA

Operating conditions: VB = +4 V to +36 V

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range		-40		125	°C
T02	Rthja	Thermal Resistance Chip to Ambient QFN24	Surface mounted, Thermal-Pad soldered to approx. 2 cm² copper area on the PCB		30	40	K/W

All voltages are referenced to ground (pin GND: power ground) unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating conditions: VB = +4 V to +36 V, RREF = 20 kΩ ±1 %, Tj = -40°C to +125°C, reference is GND (GNDA = GND), unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	VB	Permissible Supply Voltage		4		36	V
002	I()	Supply Current in VB	ENV1 = lo, ENV2 = lo, standby	20	100	200	µA
003	I()	Supply Current in VB	only one Linear Regulator active, no load current, no external voltage divider VB = 24 V VB = 12 V VB = 4 V	1.5 2.5 10	3 5.5 22	8 15 50	mA mA mA
004	I()	Supply Current in VB	both Linear Regulators active, no load current, no external voltage divider VB = 24 V VB = 12 V VB = 4 V	2 3 12	4 7 25	10 20 60	mA mA mA
007	Ipd()	Pull-Down Current in ENV1, ENV2	V() = 2...36 V	15		150	µA
009	Vt()hi	Input Threshold Voltage hi at ENV1, ENV2				2	V
010	Vt()lo	Input Threshold Voltage lo at ENV1, ENV2		0.8			V
011	Vt()hys	Input Hysteresis at ENV1, ENV2	Vt()hys = Vt()hi − Vt()lo	100	200	400	mV
012	Vc()lo	Clamp Voltage lo at all pins with exception of VB	versus GND, I() = -10 mA	-1.4		-0.3	V
013	Vc()lo	Clamp Voltage lo at VB	versus GND, I() = -2 mA	-60		-42	V
014	Vc()hi	Clamp Voltage hi at VB VBR, VBL, ENV1, ENV2	versus GND, I() = 2 mA	42		60	V
015	Vc()hi	Clamp Voltage hi at VBROK, NAUT, TOK, TEST	versus GND, I() = 1 mA	9		18	V
016	Vc()hi	Clamp Voltage hi at VH	versus GND, I() = 5 mA	8.3		18	V
017	Vc()hi	Clamp Voltage hi at VH1, VH2	versus GND, I() = 10 mA	6.2		18	V
018	Vc()hi	Clamp Voltage hi at VCC1, VCC2, POE1, POE2, CFG1, CFG2	versus GND, I() = 10 mA	5.6		18	V
019	Vc()hi	Clamp Voltage hi at GNDA, RREF	versus GND, I() = 10 mA	2.5		18	V
020	Vc()hi	Clamp Voltage hi at V1OK, V2OK	V1OK versus VCC1, V2OK versus VCC2, I() = 2 mA	0.3		1.4	V
021	Vc()hi	Clamp Voltage hi at VHL	versus VH, I() = 10 mA	0.3		1.4	V
Reverse Polarity Protection VB, VBR and Autarky Detection NAUT							
101	Vs()hi	Saturation Voltage hi at VBR	Vs(VBR)hi = VB − V(VBR), I(VBR) = -100 mA		0.3	0.6	V
103	Izu()	Maximum Permissible Current hi from VBR at Startup	V(VBR) = 0...3 V, VB increasing	-5		0	mA
104	Imax()	Maximum Current from VBR	V(VBR) = 2 V...VB − 0.6 V	-500	-250	-120	mA
105	Imax()	Maximum Current from VBR	V(VBR) = 0 V	-150		-10	mA
108	Ir()	Leakage Current from VB at Autarky	VBR > VB + 50 mV	-0.5		0	mA
109	d(VB,VBR)	Voltage Difference for Autarky	VBR versus VB; NAUT = lo	25	12.5	0	mV
110	Ir,max()	Maximum Current from VB	VB < VBR < VB + 50 mV	-10	-4	0	mA
111	Ir()	Reverse Current from VB	-36V < VB < GND	-1		0	mA
112	Vs()lo	Saturation Voltage lo at NAUT	I(NAUT) = 5 mA, NAUT = lo			0.4	V
113	Isc()lo	Short-Circuit Current lo in NAUT	V(NAUT) = 2...8 V, NAUT = lo		10	20	mA
114	Ilk()	Leakage Current in NAUT	V(NAUT) = 0...8 V, NAUT = hi	-10		10	µA
Voltage Monitoring VBR and Error Detection VBROK							
201	Vt1()hi	Lower Turn-on Threshold VBR	VBR increasing, VBROK: lo → open		3.75	3.95	V
202	Vt1()lo	Lower Turn-off Threshold VBR	VBR decreasing, VBROK: open → lo	2.8	3.15		V

ELECTRICAL CHARACTERISTICS

Operating conditions: VB = +4 V to +36 V, RREF = 20 kΩ ±1 %, Tj = -40°C to +125°C, reference is GND (GNDA = GND), unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
203	Vt1()hys	Hysteresis VBR	Vt1()hys = Vt1()hi − Vt1()lo	300	600		mV
204	Vt2()hi	Overvoltage Detection at VBR	VBR increasing, VBROK: open → lo		40.4	42	V
205	Vt2()lo	Reset Overvoltage Detection at VBR	VBR decreasing, VBROK: lo → open	35	37.6		V
206	Vt2()hys	Hysteresis VBR	Vt2()hys = Vt2()hi − Vt2()lo	1	2.8	4	V
210	Vs()lo	Saturation Voltage lo at VBROK	I(VBROK) = 5 mA, VBROK = lo			0.4	V
211	Isc()lo	Short-Circuit Current lo in VBROK	V(VBROK) = 2..8 V, VBROK = lo			50	mA
212	Ilk()	Leakage Current in VBROK	V(VBROK) = 0..8 V, VBROK = hi	-10		10	µA
213	V(VBR)	Minimal Supply Voltage for VBROK Function	I(VBROK) = 5 mA, VBROK = lo, Vs(VBROK)lo < 0.4 V	3.2			V
Switching Regulator VH, VH1, VH2							
305	V()	Voltage at VH	LVBH = 22 µH ±20 %, Ri(LVBH) < 1.1 Ω, CVH = 1 µF; VB ≤ 5 V, I(VH) = -50 mA, VB > 5 V, I(VH) = -100 mA, VB ≥ 12 V, I(VH) = -200 mA, VB ≥ 24 V, I(VH) = -300 mA	7 7.25 7.25 7.25	7.75 7.75 7.75 7.75	8 8 8 8	V V V V
307	CVH	Required Capacitor at VH	tolerance ±30 %	1			µF
308	RiVH	Permissible Internal Resistance of Capacitor at VH				1	Ω
309	V()	Voltage at VH1	versus VCC1, CVH1 = 1 µF, VB ≤ 5 V, I(VH1) = -50 mA, VB > 5 V, I(VH1) = -100 mA, VB ≥ 12 V, I(VH1) = -200 mA, VB ≥ 24 V, I(VH1) = -300 mA	300	400	600	mV
311	CVH1	Required Capacitor at VH1	tolerance ±30 %	1			µF
312	RiCVH1	Permissible Internal Resistance of Capacitor at VH1				1	Ω
313	V()	Voltage at VH2	versus VCC2, CVH2 = 1 µF, VB ≤ 5V, I(VH2) = -50 mA, VB > 5 V, I(VH2) = -100 mA, VB ≥ 12 V, I(VH2) = -200 mA, VB ≥ 24 V, I(VH2) = -300 mA	300	400	600	mV
315	CVH2	Required Capacitor at VH2	tolerance ±30 %	1			µF
316	RiCVH2	Permissible Internal Resistance of Capacitor at VH2				1	Ω
330	ηVH	Efficiency of Switching Converter VH	VB = 4 V, V(VH) > 7 V, VB = VBR, VH1 > VCC1 + 800 mV, VH2 > VCC2 + 800 mV	70			%
331	ηVH	Efficiency of Switching Converter VH	VB = 6.5 V, V(VH) > 7 V, VB = VBR, VH1 > VCC1 + 800 mV, VH2 > VCC2 + 800 mV	80			%
332	ηVH1	Efficiency of Switching Converter VH1	VB = 4 V, V(VH) > 8.1 V, VB = VBR, ENV1 = hi, ENV2 = lo	70			%
333	ηVH1	Efficiency of Switching Converter VH1		80			%
334	ηVH2	Efficiency of Switching Converter VH2	VB = 4 V, V(VH) > 8.1 V, VB = VBR, ENV1 = lo, ENV2 = hi	70			%
335	ηVH2	Efficiency of Switching Converter VH2	VB = 6.5 V, V(VH) > 8.1 V, VB = VBR, ENV1 = lo, ENV2 = hi	80			%
Bias, Oscillator and Reference RREF							
401	V()	Voltage at RREF	resistor RREF = 20 kΩ ±1 %, resistor RREF versus GNDA	1.18	1.24	1.3	V
402	R()	Permissible Resistor at RREF	±1 %	19.6		34	kΩ
403	Isc()	Short-Circuit Current lo in RREF	V(RREF) = 0 V	-3		-0.5	mA

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Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
404	fos	Oscillator Frequency	resistor RREF = 20 kΩ ±1 %, resistor RREF versus GNDA	2		7	MHz
Linear Regulator VCC1							
501	VCC1$_{nom,hi}$	Output Voltage	CFG1 = VCC1; VB < 5 V, I(VCC1) = -60...10 mA, VB $\geq$ 5 V, I(VCC1) = -100...10 mA, VB $\geq$ 6.5 V, I(VCC1) = -150...10 mA, VB $\geq$ 12 V, I(VCC1) = -200...10 mA, VB $\geq$ 24 V, I(VCC1) = -250...10 mA	4.75	5	5.25	V
502	VCC1$_{nom,lo}$	Output Voltage	CFG1 = GNDA; VB < 5 V, I(VCC1) = -100...10 mA, VB $\geq$ 5 V, I(VCC1) = -150...10 mA, VB $\geq$ 6.5 V, I(VCC1) = -200...10 mA, VB $\geq$ 16 V, I(VCC1) = -300...10 mA, VB $\geq$ 24 V, I(VCC1) = -350...10 mA,	3.135	3.3	3.465	V
503	Vr(CFG1)	Transmission Ratio of external Voltage Divider R(VCC1/CFG1) / R(CFG1/GNDA)	V(VCC1) = (1 + R(VCC1/CFG1) / R(CFG1/GNDA)) * V(RREF), R(VCC1/CFG1) + R(CFG1/GNDA) = 10 kΩ...50 kΩ ±1 %, V(VCC1) = 1.5...5.5 V	0.2		3.5	
504	CVCC1	Required Capacitor at VCC1 versus GNDA	tolerance ±30 %	1			µF
505	RiCVCC1	Permissible Internal Resistance of Capacitor at VCC1				1	Ω
506	VCC1,lir	Line Regulation	I(VCC1) = -100 mA, VB = 8...30 V	-20		20	mV
507	VCC1,lor	Load Regulation	VB = 24 V, I(VCC1) = 0...200 mA	-20		20	mV
508	VCC1rip	Output Ripple	I(VCC1) = -100mA		10		mVpp
Linear Regulator VCC2							
601	VCC2$_{nom,hi}$	Output Voltage	CFG2 = VCC2; VB < 5 V, I(VCC2) = -100...10 mA, VB $\geq$ 5 V, I(VCC2) = -150...10 mA, VB $\geq$ 6.5 V, I(VCC2) = -200...10 mA, VB $\geq$ 16 V, I(VCC2) = -300...10 mA, VB $\geq$ 24 V, I(VCC2) = -350...10 mA	3.135	3.3	3.465	V
602	VCC2$_{nom,lo}$	Output Voltage	CFG2 = GNDA; VB < 5 V, I(VCC2) = -150...10 mA, VB $\geq$ 5 V, I(VCC2) = -200...10 mA, VB $\geq$ 6.5 V, I(VCC2) = -250...10 mA, VB $\geq$ 12 V, I(VCC2) = -300...10 mA, VB $\geq$ 24 V, I(VCC2) = -350...10 mA	2.375	2.5	2.625	V
603	Vr(VCC2)	Transmission Ratio of external Voltage Divider R(VCC2/CFG2) / R(CFG2/GNDA)	V(VCC2) = (1 + R(VCC2/CFG2) / R(CFG2/GNDA)) * V(RREF), R(VCC2/CFG2) + R(CFG2/GNDA) = 10 kΩ...50 kΩ ±1 %, V(VCC2) = 1.5...5.5 V	0.2		3.5	
604	CVCC2	Required Capacitor at VCC2 versus GNDA	tolerance ±30 %	1			µF
605	RiCVCC2	Permissible Internal Resistance of Capacitor at VCC2				1	Ω
606	VCC2,lir	Line Regulation	I(VCC2) = -100 mA, VB = 8...30 V	-20		20	mV
607	VCC2,lor	Load Regulation	VB = 24 V, I(VCC2) = 0...200 mA	-20		20	mV
608	VCC2rip	Output Ripple	I(VCC2) = -100mA		10		mVpp

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Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Voltage Monitoring V1OK, V2OK (x = 1, 2)							
701	VtU()lo	Lower Undervoltage Threshold VCCx for VxOK = lo	versus VCCxnom	90	92	94	%VCC2
702	VtU()hi	Upper Undervoltage Threshold VCCx for VxOK = hi	versus VCCxnom	91	93	95	%VCC2
703	VtO()lo	Lower Overvoltage Threshold VCCx for VxOK = hi	versus VCCxnom	105	107	109	%VCC2
704	VtO()hi	Upper Overvoltage Threshold VCCx for VxOK = lo	versus VCCxnom	106	108	110	%VCC2
705	Vt()hys	Hysteresis Under-/Overvoltage VCCx	versus VCCxnom	0.25	1	1.5	%VCC2
706	Vs()lo	Saturation Voltage lo	VxOK = lo; I() = 4 mA, VCCx ≥ 3 V; I() = 1 mA, VCCx < 3 V			0.4; 0.4	V; V
707	Vs()hi	Saturation Voltage hi	Vs()hi = VCCx − V(), VxOK = hi; I() = -4 mA, VCC2 ≥ 3 V; I() = -1 mA, VCC2 < 3 V			0.4; 0.4	V; V
708	Isc()lo	Short-Circuit Current lo	V() = VCCx, VxOK = lo; VCCx ≥ 3 V; VCCx < 3 V	6; 1		80; 30	mA; mA
709	Isc()hi	Short-Circuit Current hi	V() = 0 V, VxOK = hi; VCCx ≥ 3 V; VCCx < 3 V	-100; -30		-6; -1	mA; mA
Supply Switches POE1, POE2 (x = 1, 2)							
801	Vs()hi	Saturation Voltage hi	Vs()hi = VCCx − V(POEx); V(VCCx) ≥ 2.5 V, I(POEx) = -10 mA, V1OK, V2OK = hi			0.2	V
802	Vs()hi	Saturation Voltage hi	Vs()hi = VCCx − V(POEx); V(VCCx) < 2.5 V; I(POEx) = -5 mA, V1OK, V2OK = hi			0.2	V
803	Isc()hi	Short-Circuit Current hi	V(POEx) = 0 V; V(VCCx) ≥ 2.5 V, POEx = hi, V1OK, V2OK = hi	-40		-12	mA
804	Isc()hi	Short-Circuit Current hi	V(POEx) = 0 V; V(VCCx) < 2.5 V, POEx = hi, V1OK, V2OK = hi	-30		-6	mA
Thermal Shutdown and Error Detection TOK							
901	Toff	Thermal Shutdown Threshold		150	160	175	°C
902	Ton	Restart Temperature		135	150	165	°C
903	Thys	Temperature Hysteresis	Thys = Toff − Ton	5	10	20	°C
904	Vs()lo	Saturation Voltage lo	I(TOK) = 5 mA; TOK = lo			0.4	V
905	Isc()lo	Short-Circuit Current lo	V(TOK) = 2..8 V; TOK = lo		10	20	mA
906	Ik()	Leakage Current	V(TOK) = 0..8 V; TOK = hi	-10		10	µA
Test Input TEST							
A01	Vt()hi	Threshold Voltage hi for Comparator test			0.64	0.7	V
A02	Vt()lo	Threshold Voltage lo for Comparator test		0.54	0.6		V
A03	Vt()hys	Hysteresis at TEST	Vt() = Vt(TEST)hi − Vt(TEST)lo	10	40	100	mV
A05	Ipd()	Pull-Down Current in TEST	V() = 5.5 V	20		200	µA
A07	tsu(TEST)	Settling Time at V1OK, V2OK	V1OK, V2OK changing hi → lo	10	20	30	µs
A08	tsu(TEST)	Settling Time at V1OK, V2OK	V1OK, V2OK changing of lo → hi	2	4	8	µs

DESCRIPTION OF FUNCTIONS

DC/DC converter iC-DC generates two regulated voltages of VH1 and VH2 from voltage VBR. These prestabilize the two linear regulators VCC1 and VCC2. A third voltage of VH, also regulated, is generated to drive these linear regulators. Voltage supply VB may be either above or below the output voltages. Figure 1 shoes the basic function principle of iC-DC. Switches S1 to S6 and diode D1 have been implemented on the chip. The inductor, capacitors, and load resistors are external devices.

Another feature of iC-DC is that bias voltages VH1 and VH2 adjust themselves automatically to approximately 400 mV using the selected VCC1 or VCC2 voltage. This results in minimum power dissipation as only a low amount of voltage is lost through each of the linear regulators.

Charge/discharge phase
During the charge phase switches S_1 and S_2 close with the internal clock. A linearly increasing current flows through coil LVBH. The energy from supply VBR is stored in the coil's magnetic field.

Switches S_1 and S_2 open for discharging. Switch S_3 and one of the switches S_4/S_5/S_6 are closed. The current can continue to flow in the coil and is supplied to the relevant capacitor and relevant load. Figure 2 describes the resulting course of the current and voltage. The current rise and fall times depend on the inductor voltage.
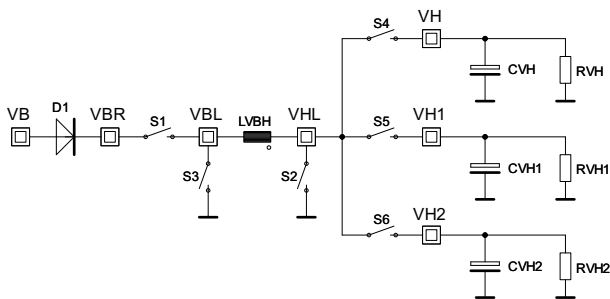
Figure 1: Principle of operation of the converter

Figure 2: Converter current/voltage characteristics (VB = 4 V)

Intermittent flow / continuous flow

If the inductor is recharged in the next cycle before the coil current has run free, there is no gap in the current. This *continuous flow* occurs when the supply voltage is low or the load current high.

If the charge and discharge processes are concluded within one clock cycle and the coil current drops to zero each time, *intermittent flow* prevails. This is the case when the supply voltage is sufficiently high or the load current sufficiently low.

When no more current flows through the coil, after flyback in *intermittent operation* both ends of the inductor are switched to ground. This prevents the oscillations in no-load operation that are typical of many converters (RLC resonating circuit). This helps to achieve better EMC behavior.

Startup behavior

During startup and with low supply voltages the coil's maximum cut-off current is reduced (soft start) until the nominal voltage is reached at VH. Figure 3 shows the startup behavior for VH, VCC1 (5 V), and VCC2 (3.3 V) with the voltage monitor outputs V1OK and V2OK.

As three output voltages are generated with this switching converter topology using just one single in-ductor, the sequence must allow that all three converter outputs are respectively supplied with the required current. The core of the converter consists of three independent converters. Each converter has its own regulated cut-off and restart current and its own voltage monitor. During the startup phase the VH converter ramps up until a voltage of approximately 7 V is obtained. Here, the cut-off current is initially limited to lower values so that a *soft start* with a low startup current ripple is achieved.

When a high enough VH voltage is available, the VH1 and VH2 converters are also switched on and the voltages rise to their nominal values. Once in a steady state, the individual converters are cyclically supplied by the inductor with precisely the amount of current that is required at that moment. The maximum load current can thus be drawn from each of the voltages VH, VH1, VH2, VCC1, or VCC2.

Standby

The converters can be individually activated by pins ENV1 and ENV2. If neither of the two inputs are triggered, the device is in standby mode and the current consumption is reduced to a minimum. As soon as one of the two inputs becomes active, the VH voltage is also available.
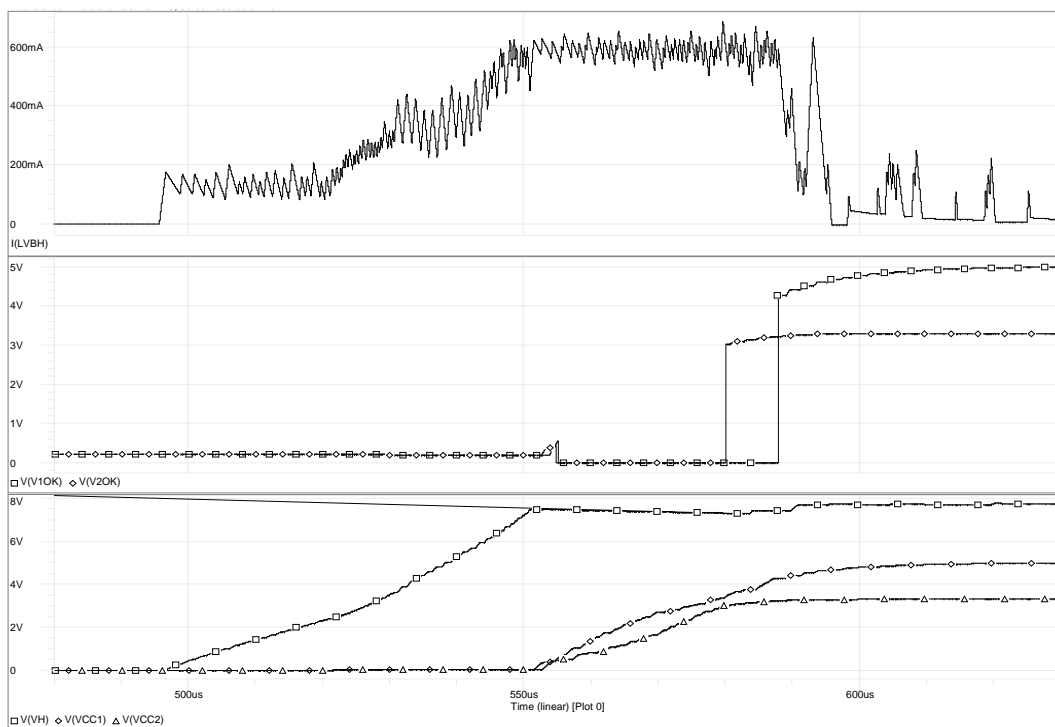

Figure 3: Startup principle for voltages VH, VCC1, VCC2, V1OK, and V2OK

LINEAR REGULATORS VCC1 AND VCC2

To achieve as low an interference voltage as possible, even with small filter capacitors C_{VH1} and C_{VH2}, an independent linear regulator is connected after each of the intermediate voltages VH1 und VH2.

Output voltages VCC1 and VCC2 can each be adjusted using a voltage divider at CFG1 and CFG2 within a range of 1.5 to 5.5 V ±5 % and according to Equations 1 and 2.

$$V_{VCC1} = V(RREF) \times (1 + \frac{R_1}{R_2}) \qquad (1)$$

and

$$V_{VCC2} = V(RREF) \times (1 + \frac{R_3}{R_4}) \qquad (2)$$

NB: $R_1 + R_2$ bzw. $R_3 + R_4 = 10\,k\Omega$ bis $50\,k\Omega$

Inputs CFG1 and CFG2 can also be directly connected to the relevant output voltage VCCx or GNDA. The resulting voltages are given in Tables 4 and 5.

VCC1 output voltage	
Potential at CFG1	VCC1
GNDA	3.3 V
VCC1	5.0 V
Voltage divider	1.5 V to 5.5 V

Table 4: VCC1 settings

VCC2 output voltage	
Potential at CFG2	VCC2
GNDA	2.5 V
VCC2	3.3 V
Voltage divider	1.5 V to 5.5 V

Table 5: VCC2 settings

The regulators have been compensated internally so that they are stable in no-load operation without an external capacitor. Stability across the entire load range is guaranteed by the minimum capacitances for C_{VCC1} and C_{VCC2} given in the electrical characteristics. The outputs are current limited to protect them against destruction in the event of a short circuit.

The two linear regulators can be switched on and off independently by inputs ENV1 and ENV2. If both reg-

ulators are deactivated, iC-DC is in standby mode (see DESCRIPTION OF FUNCTIONS/Standby).

Switched output voltages
The two pins POE1 and POE2 are triggered by monitor outputs V1OK and V2OK and provide voltages drawn from VCC1 or VCC2. This enables the supply of specific circuitry in a component group (e.g. EEPROMs) to be switched on only after VCC1 or VCC2 have reached their steady state.

Voltage monitor self-test
Using pin TEST the voltage monitoring comparators at V1OK and V2OK can be tested during ongoing operation. The undervoltage and overvoltage thresholds of V1OK and V2OK are checked in turn with each test. For this purpose, pin TEST is increased to above the threshold voltage by an external driver. Correct functioning is signaled by low signals at pins V1OK and V2OK. The function of the connected POE1 and POE2 outputs remains unaffected.

Current carrying capacity
iC-DC's current carrying capacity depends on set output voltage VCCx and input voltage VB. Figure 4 shows the current carrying capacity dependent on the input voltage for various output voltages, measured on the iC-DC EVAL DC1D evaluation board. The internal reverse polarity protective circuit was bridged (VB = VBR) to increase the current carrying capacity.
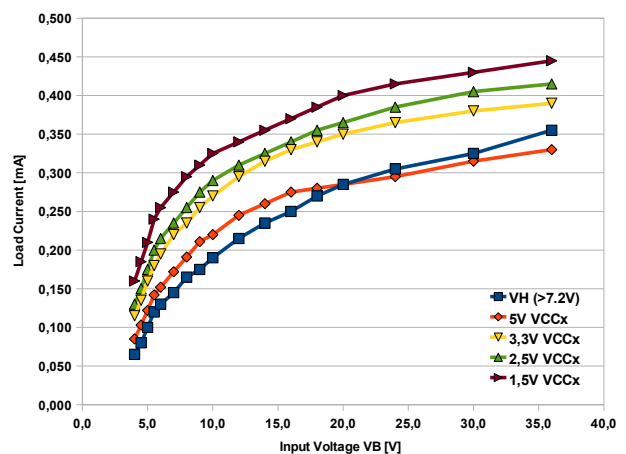

Figure 4: Current carrying capacity for various output voltages dependent on VB (VB = VBR)

REVERSE POLARITY PROTECTION

A protective switch inserted between supply VB and pin VBR protects the entire system against reverse polarity. This can also be used to implement an Autarky function (see AUTARKY FUNCTION). By connecting VB to VBR the reverse polarity protection circuit can be bridged to improve the current carrying capacity and the overall efficiency, especially if low supply voltages are used (Figure 5).
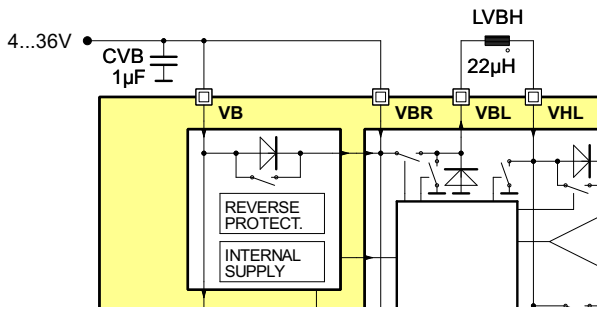

Figure 5: Protection against reverse polarity bridges VB to VBR

Figure 6: Protection against reverse polarity active, CVBR for VB = 24 V
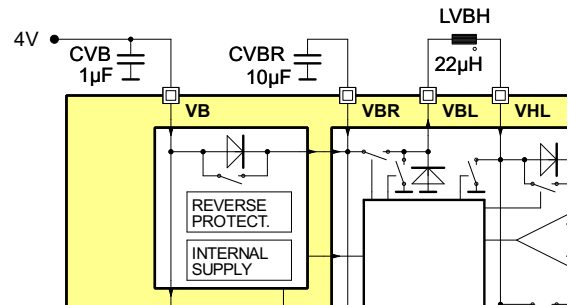
Figure 7: Protection against reverse polarity active, CVBR for VB = 4 V

The reverse polarity protection switch is current limited to the maximum mean current consumption of the system (Electrical Characteristics 104). A capacitor (CVBR) must be connected to pin VBR if higher coil cut-off currents are to be supplied.

This capacitor should have a value of at least 1 µF at a supply voltage of VB = 24 V (Figure 6). With very small supply voltages the value must be greater in order to cater for the higher power consumption during startup. The voltage at VBR must no longer drop below the lower shutdown threshold (Electrical Characteristics 202) to ensure safe converter startup. A capacitor of approx. 10 µF should thus be selected for CVBR at a supply voltage of VB = 4 V (Figure 7).

It is possible to use the protective switch at pin VBR to provide further circuitry with protection against reverse polarity (Figure 9, Page 17). Here, it must noted that the current carrying capacity of the reverse polarity protection (VBR) is limited on startup. As the device powers itself from VBR, the load at VBR must not be too high as otherwise converter operation cannot be initiated. The current carrying capacity on startup can be approximately described by Equation 3:

$$I(VBR) = V(VB) * \frac{-1mA}{V} \qquad (3)$$

iC-DC
2-CHANNEL BUCK/BOOST DC/DC CONVERTER

preliminary iC-Haus

ERROR EVALUATION

Supply voltage monitor
Supply voltage VBR is monitored. If the normal voltage range is overshot or undershot, this is signaled at open-drain pin VBROK. The bias current generated by an external reference resistor is also monitored and an error signaled at VBROK should the permissible range be exceeded. If an error has occurred, pin VBROK is switched to GND.

Output voltage monitor
The two linear regulator output voltages VCC1 and VCC2 are also monitored. If the overvoltage threshold is overshot or the undervoltage threshold undershot (e.g. due to overload), a message is generated at the current-limited push-pull outputs V1OK and V2OK. Voltage outputs POE1 and POE2 are shut down.

Output voltage monitor self-test
Using pin TEST the voltage monitoring comparators at V1OK and V2OK can be tested during ongoing operation. The undervoltage and overvoltage thresholds of V1OK and V2OK are checked in turn with each test. For this purpose, pin TEST is increased to above the threshold voltage by an external driver. Correct functioning is signaled by low signals at pins V1OK and V2OK. The function of the connected POE1 and POE2 outputs remains unaffected.

Temperature monitor
The internal chip temperature is monitored. If the monitor indicates overtemperature, all switches on the switching converter are shut down. These are automatically re-enabled when the chip temperature has dropped below the restart temperature. A message is signaled at open-drain pin TOK for as long as the converter is shut down due to chip overtemperature.

The protective switch (VB / VBR) has its own over temperature protection, which is also operative during standby mode.

As error outputs VBROK and TOK are current limited, an LED can be directly connected up for visual message display. However, the additional power dissipation this causes in the IC must be taken into account. By placing resistor R_{LED} in series with the LED, this additional chip power loss can be reduced in the event of error. CMOS or TTL-compatible logic inputs can be activated by pull-up resistors at VBROK and TOK.

AUTARKY FUNCTION

By inserting a capacitor at VBR, an Autarky function can be realized should the supply fail at VB. This Autarky function guarantees the linear regulator output voltages for some time. If the voltage at VBR is greater than at VB (elec. char. no. 109), this is signaled by current-limited open-drain output NAUT. To ensure that VBR > VB should the supply voltage fail, it is recom-mended that a resistor be switched between VB and GND in order to generate the required differential voltage of $d_{VBR, VB}$.

With this capacitor acting as a buffer, the effect of current spikes feeding back into the supply voltage VB is also reduced.

DESCRIPTION OF THE APPLICATION

Selecting the coil

The coil should be designed for a maximum cut-off current of 1 A. A small internal resistor in the coil reduces loss and increases converter efficiency. At a low supply voltage this internal resistor can determine the maximum available output current.

The EMI caused by the coil should be taken into consideration. Toroidal core coils have little noise radiation yet are expensive and difficult to install. Bar core coils are reasonably priced and easier to use yet have a higher noise emittance. For modest EMI requirements inexpensive radio interference suppression coils of several tens of µH are suitable*.

Selecting the capacitors

Selecting back-up capacitors C_{VH}, C_{VH1} and C_{VH2} is unproblematic. As the residual ripple of intermediate voltages VH1 and VH2 does not affect output voltages VCC1 and VCC2 thanks to the back-end linear regulators, a small capacitor is sufficient without any specific demands being made of the internal resistor. A combination of electrolytic and ceramic capacitors (e.g. 3.3 µF || 100 nF) is recommended. Before using tantalum capacitors, the user must verify whether these are suitable for the residual AC amplitude (residual ripple) at pins VH1 and VH2.

Stability of the linear regulators across the entire load area is guaranteed if the values given in the electrical characteristics are selected for CVCC1 and CVCC2. The suppression of interference voltage is improved by using small capacitor series resistors. A combination of tantalum and ceramic capacitors is also recommended in this case. If one of the two outputs remains open, this capacitor can be omitted.

To avoid feedback of interference from supply voltage VB onto output voltages VCC1 and VCC2, blocking should be provided directly at pin VB. A combination of tantalum and ceramic capacitors (e.g. 1 µF || 100 nF) is also recommended in this case.

Printed circuit board layout

The GND path from the switching converter and from each linear regulator should be strictly separated to avoid cross couplings. The neutral point of all GND paths is the GND connection at iC-DC. It is possible and not critical, however, to route GND from supply VB and the base point of capacitors C_{VH}, C_{VH1} and C_{VH2} together to the neutral point. The capacitors should be very close to their relevant pins, however.

Blocking capacitors for supply VB should be arranged as close as possible to pins VB and GND. The capacitors for outputs VCC1 and VCC2 should be placed directly at the load and not at the IC to also block interferences which are coupled via the wiring to the load.

The ground planes underneath the wiring of output voltages VCC1, VCC2, POE1, and POE2 should be kept separate from the ground planes of switching converters VH, VH1, and VH2. The ground planes must be connected up at a neutral point (see Figure 8).

The thermal pad should be connected to the PCB by an appropriate ground plane. The resulting power dissipation can be transferred to a different wiring layer, e.g. a ground plane, by vias directly underneath the IC.
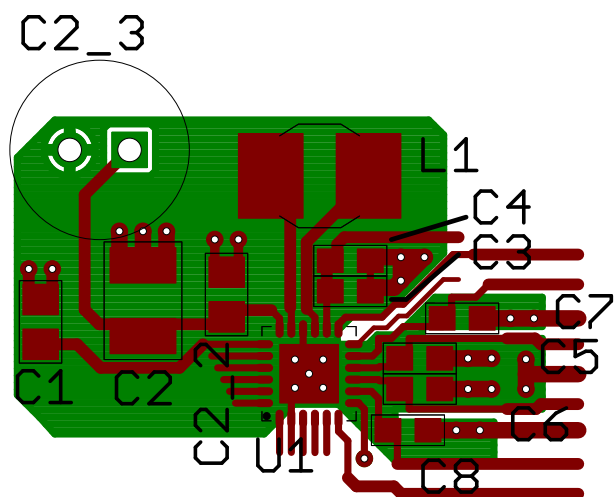

Figure 8: Example layout: evaluation board DC1D

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* e.g.: Siemens Matsushita B78108-S1224-J (22 µH/1 A, axial), TDK series NLC565050T-... (SMD), TOKO series 10RF459-... (SMD shielded)
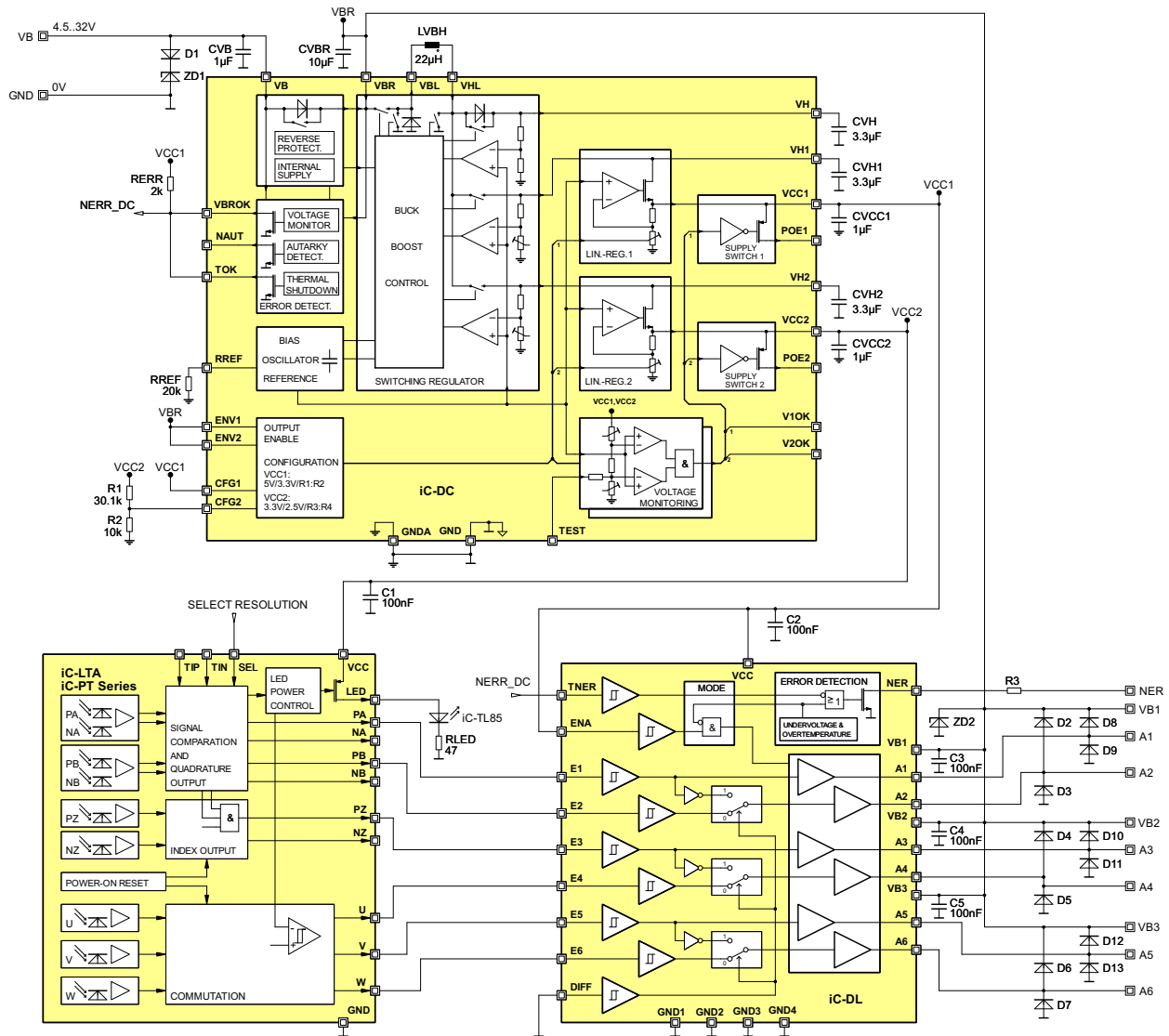
EXAMPLE APPLICATION

Figure 9: Application with iC-DC, iC-PT, and iC-DL

The application diagram in Figure 9 shows an example circuit featuring the DC/DC converter iC-DC. The input voltage range is set to between 4.5 V and 32 V by line driver iC-DL. The output voltages of the two linear regulators are each configured to 5 V. VCC2 supplies the optical 6-channel incremental scanner iC-LTA/iC-PT and VCC1 the 5 V section of 24 V line driver iC-DL. This creates a separation in the supply voltage between the sensing mechanism and the digital switching section of the circuitry.

The status signals for overvoltage (VBROK) and overtemperature (TOK) in iC-DC are connected to iC-DL's error message input TNER. This links the iC-DC error messages to iC-DL's own undervoltage and overtemperature monitor. iC-DL's open-drain error message output NER thus provides the error messages for both ICs.

This example circuit makes use of iC-DC's integrated reverse polarity protection feature. The illustrated diodes ZD1, ZD2, D2 to D13 and resistor R3 form the basis for a protective circuit against overvoltage for all outputs. No specific designations are given for these components as these protective circuits are to be individually configured and dimensioned according to the application and requirement.

DESIGN REVIEW: Notes On Chip Functions

iC-DC Z		
Nr.	Function, Parameter/Code	Description and Application Hints
1	**Vc(VB)lo**	Clamp Voltage lo at VB (elec. char. no. 013) can have a maximum of -40 V at low temperature.

Table 6: Notes on chip functions regarding iC-DC chip release Z

ORDERING INFORMATION

Type	Package	Order Designation
iC-DC	QFN24 4 mm x 4 mm	iC-DC QFN24-4x4
	Evaluation Board	iC-DC EVAL DC1D

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