DAC1653Q/DAC1658Q

Quad 16-bit DAC: 10 Gbps JESD204B interface: up to 1.50 Gsps; x2, x4 and x8 interpolating

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1. General description

The DAC1658Q and the DAC1653Q are high-speed high-performance 16-bit quad channel digital-to-analog converter (DAC) with high and low common-mode output. The devices provide a sample rate up to 1.50 Gsps with selectable ×2, ×4 and ×8 interpolation filters optimized for multi-carrier and broadband wireless transmitters.

When both devices are referred to in this data sheet, the following convention will be used: DAC165xQ.

The DAC165xQ integrates a JESD204B high-speed serial input data interface running up to 10 Gbps allowing quad channel input sampling at up to 750 Msps over eight differential lanes. It offers numerous advantages over traditional parallel digital interfaces:

- Easier Printed-Circuit Board (PCB) layout
- Lower radiated noise
- Lower pin count
- Self-synchronous link
- Skew compensation
- Deterministic latency
- Multiple Device Synchronization (MDS); JESD204B subclass 1 support
- Harmonic clocking support
- Assured FPGA interoperability

There are two versions of the DAC165xQ:

- Low common-mode output voltage (part identification DAC1653Q)
- High common-mode output voltage (part identification DAC1658Q)

Two optional on-chip digital modulators convert the complex I/Q pattern from baseband to IF. The mixer frequency is set by writing to the Serial Peripheral Interface (SPI) control registers associated with the on-chip 40-bit Numerically Controlled Oscillator (NCO). This accurately places the IF carrier in the frequency domain. The 13-bit phase adjustment feature, the 12-bit digital gain and the 16-bit digital offset enable full control of the analog output signals.

The DAC165xQ is fully compatible with device subclass 1 of the JEDEC JESD204B standard, guaranteeing deterministic and repeatable interface latency using the differential SYSREF signal. The device also supports harmonic clocking to reduce system-level clock synthesis and distribution challenges.

Multiple Device Synchronization (MDS) enables multiple DAC channels to be sample synchronous and phase coherent to within one DAC clock period. MDS is ideal for LTE and LTE-A MIMO transceiver applications.

The DAC165xQ includes an internal regulation to adjust the full-scale output current. The internal regulator adjusts the full-scale output current between 8.1 mA and 34 mA. The device is available in a HLA72 package (10 mm × 10 mm). It is supported by customer demo boards that are supplied with or without FPGA logic devices.

2. Features and benefits

- quad channel 16-bit resolution
- 1.50 GSps maximum output update rate
- JEDEC JESD204B device subclass I compatible: SYSREF based deterministic and repeatable interface latency
- Multiple Device Synchronization (MDS) enables multiple DAC channels to be sample synchronous and phase coherent to within one DAC clock period
- 8 configurable JESD204B serial input lanes running up to 10 Gbps with embedded termination and programmable equalization gain
- 750 Msps maximum baseband input data rate
- SPI interface (3-wire or 4-wire mode) for control setting and status monitoring
- differential scalable output current from 8.1 mA to 34 mA
- two embedded NCOs with 40-bit programmable frequency and 16-bit phase adjustment
- embedded complex (IQ) digital modulator
- 1.2 V and 2.5 V or 3.3 V power supplies
- flexible SPI power supply (1.8 V or 1.2 V) ensuring compatibility with on-board SPI bus
- flexible differential signals (SYNC) power supply (1.8 V or 1.2 V) ensuring compatibility with on-board devices
- $SFDR_{RBW}$ = 85 dBc typical (f_s = 1.47456 Gsps; interpolation ×2; bandwidth = 250 MHz; f_{out} = 150 MHz)
- NSD = −162 dBm/Hz typical (f_o = 20 MHz)
- IMD3 = 85 dBc typical (f_s = 1.47456 Gsps; interpolation ×2; f_{o1} = 152 MHz; f_{o2} = 153 MHz)
- one carrier ACLR = 77 dB typical (f_s = 1.47456 Gsps; f_{NCO} = 230 MHz)
- RF enable/disable pin and RF automatic mute. The RF enable feature is available via one of the IO pins
- very low noise bypassable integrated Phase-Locked Loop (PLL); no external capacitors
- clock divider by 2, 4, 6 or 8 available at the input of the clock path
- group delay compensation
- power-down mode control
- on-chip 0.7 V reference
- industrial temperature range −40 °C to +85 °C
- HLA72 package (10 mm × 10 mm)

3. Applications

- Wireless infrastructure radio base station transceivers, including: LTE-A, LTE, MC_GSM, W-CDMA, TD-SCDMA
- LMDS/MMDS, point-to-point microwave backhaul
- Direct Digital Synthesis (DDS) instruments
- High-definition video broadcast production equipment
- Automated Test Equipment (ATE)

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
DAC1653Q1G5NAGA	HLA72	HLA 10 × 10 × 0.85 mm	PSC-4438
DAC1653Q1G25NAGA	HLA72	HLA 10 × 10 × 0.85 mm	PSC-4438
DAC1653Q1G0NAGA	HLA72	HLA 10 × 10 × 0.85 mm	PSC-4438
DAC1658Q1G5NAGA	HLA72	HLA 10 × 10 × 0.85 mm	PSC-4438
DAC1658Q1G25NAGA	HLA72	HLA 10 × 10 × 0.85 mm	PSC-4438
DAC1658Q1G0NAGA	HLA72	HLA 10 × 10 × 0.85 mm	PSC-4438

5. Block diagram

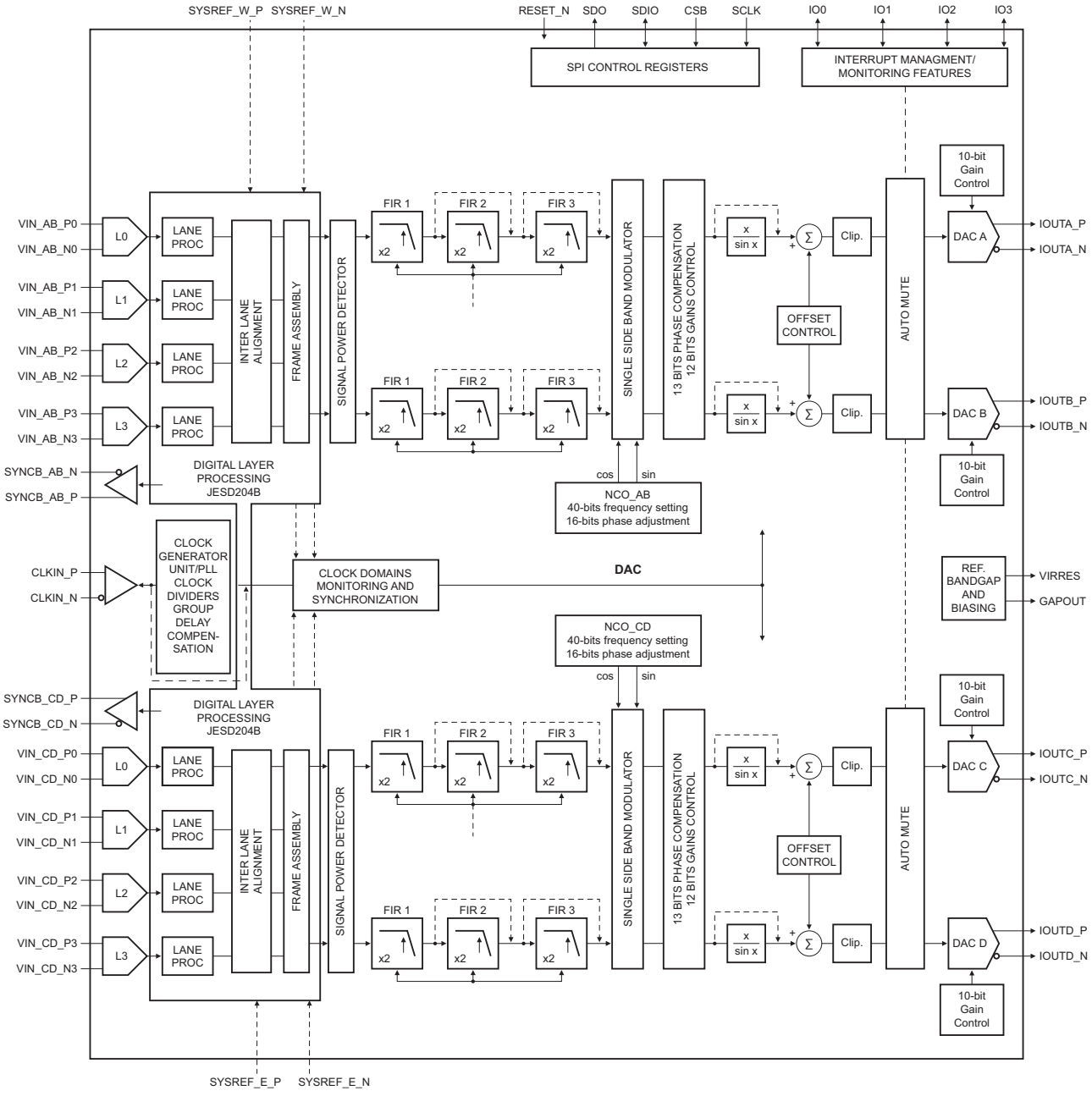
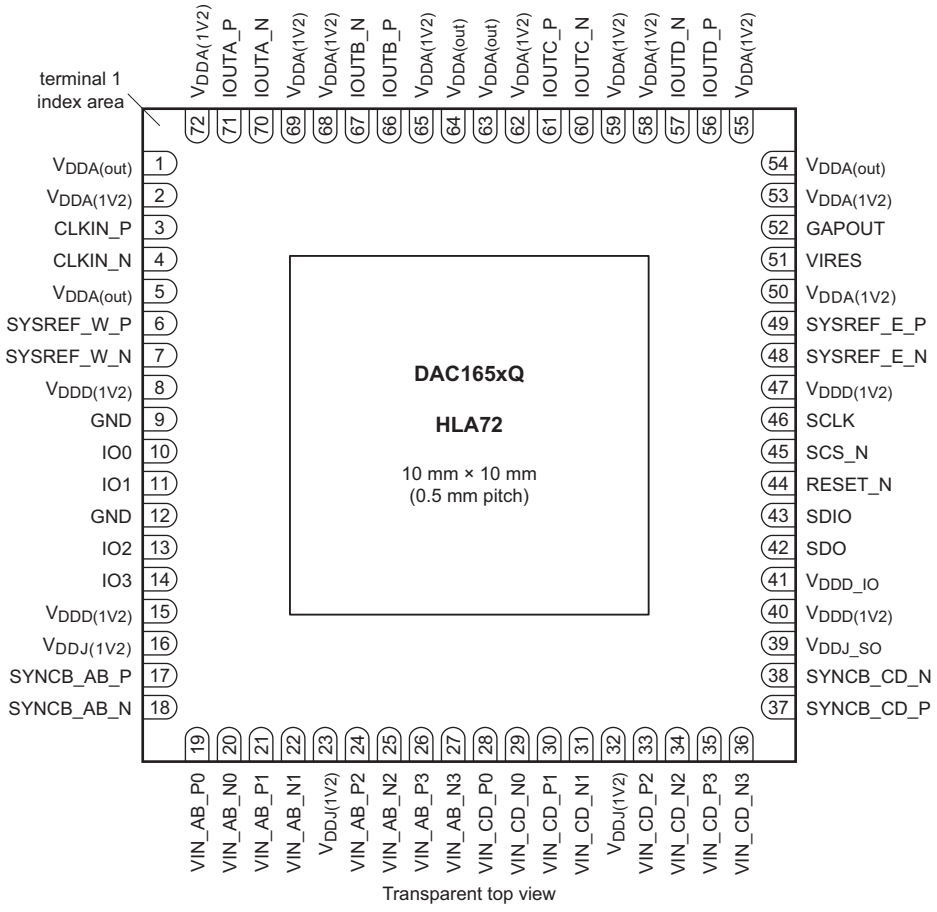


Fig 1. DAC165xQ block diagram

6. Pinning information

6.1 Pinning



$V_{DDA(out)}$ (pins 47 and 52):
DAC1658Q: 3.3 V.
DAC1653Q: 2.5 V or 3.3 V.

Fig 2. DAC165xQ pin configuration

6.2 Pin description

Table 2. Pin description

Pin	Symbol	Type	Description
1	$V_{DDA(out)}$	P	DAC1658Q: 3.3 V analog power supply
			DAC1653Q: 2.5 V or 3.3 V analog power supply
2	$V_{DDA(1V2)}$	P	1.2 V analog power supply
3	CLKIN_P	I	clock input (positive)
4	CLKIN_N	I	clock input (negative)

Table 2. Pin description *…continued*

Pin	Symbol	Type	Description
5	$V_{DDA(out)}$	P	DAC1658Q: 3.3 V analog power supply
			DAC1653Q: 2.5 V or 3.3 V analog power supply
6	SYSREF_W_P	I/O	multiple devices synchronization positive signal, west side
7	SYSREF_W_N	I/O	multiple devices synchronization negative signal, west side
8	$V_{DDD(1V2)}$	P	1.2 V digital power supply
9	GND	G	ground
10	IO0	I/O	IO port bit 0
11	IO1	I/O	IO port bit 1
12	GND	I	ground
13	IO2	I/O	IO port bit 2
14	IO3	I/O	IO port bit 3
15	$V_{DDD(1V2)}$	P	1.2 V digital power supply
16	$V_{DDJ(1V2)}$	P	1.2 V JEDEC204B interface power supply
17	SYNCB_AB_P	O	JESD204B SYNC signal for DACs A/B (positive)
18	SYNCB_AB_N	O	JESD204B SYNC signal for DACs A/B (negative)
19	VIN_AB_P0	I	DAC A/B lane 0 serial interface, positive input
20	VIN_AB_N0	I	DAC A/B lane 0 serial interface, negative input
21	VIN_AB_P1	I	DAC A/B lane 1 serial interface, positive input
22	VIN_AB_N1	I	DAC A/B lane 1 serial interface, negative input
23	$V_{DDJ(1V2)}$	P	1.2 V JEDEC204B interface power supply
24	VIN_AB_P2	I	DAC A/B lane 2 serial interface, positive input
25	VIN_AB_N2	I	DAC A/B lane 2 serial interface, negative input
26	VIN_AB_P3	I	DAC A/B lane 3 serial interface, positive input
27	VIN_AB_N3	I	DAC A/B lane 3 serial interface, negative input
28	VIN_CD_P0	I	DAC C/D lane 0 serial interface, positive input
29	VIN_CD_N0	I	DAC C/D lane 0 serial interface, negative input
30	VIN_CD_P1	I	DAC C/D lane 1 serial interface, positive input
31	VIN_CD_N1	I	DAC C/D lane 1 serial interface, negative input
32	$V_{DDJ(1V2)}$	P	1.2 V JEDEC204B interface power supply
33	VIN_CD_P2	I	DAC C/D lane 2 serial interface, positive input
34	VIN_CD_N2	I	DAC C/D lane 2 serial interface, negative input
35	VIN_CD_P3	I	DAC C/D lane 3 serial interface, positive input
36	VIN_CD_N3	I	DAC C/D lane 3 2serial interface, negative input
37	SYNCB_1_P	O	JESD204B SYNC signal for DACs C/D (positive)
38	SYNCB_1_N	O	JESD204B SYNC signal for DACs C/D (negative)
39	V_{DDJ_SO}	P	JEDEC204B SYNC output buffer power supply (1.2 V or 1.8 V)
40	$V_{DDD(1V2)}$	P	1.2 V digital power supply
41	V_{DDD_IO}	P	digital IO power supply (1.2 V or 1.8 V) (including SPI)
42	SDO	O	SPI data output
43	SDIO	I/O	SPI data input/output

Table 2. Pin description *…continued*

Pin	Symbol	Type	Description
44	RESET_N	I	general reset (active LOW)
45	SCS_N	I	SPI chip select (active LOW)
46	SCLK	I	SPI clock input
47	$V_{DDD(1V2)}$	P	1.2 V digital power supply
48	SYSREF_E_N	I/O	multiple devices synchronization negative signal, east side
49	SYSREF_E_P	I/O	multiple devices synchronization positive signal, east side
50	$V_{DDA(1V2)}$	P	1.2 V analog power supply
51	VIRES	I/O	vi-biasing resistor
52	GAPOUT	I/O	bandgap output voltage
53	$V_{DDA(1V2)}$	P	1.2 V analog power supply
54	$V_{DDA(out)}$	P	DAC1658Q: 3.3 V analog power supply
			DAC1653Q: 2.5 V or 3.3 V analog power supply
55	$V_{DDA(1V2)}$	P	1.2 V analog power supply
56	IOUTD_P	O	DAC D output current
57	IOUTD_N	O	complementary DAC D output current
58	$V_{DDA(1V2)}$	P	1.2 V analog power supply
59	$V_{DDA(1V2)}$	P	1.2 V analog power supply
60	IOUTC_N	O	complementary DAC C output current
61	IOUTC_P	O	DAC C output current
62	$V_{DDA(1V2)}$	P	1.2 V analog power supply
63	$V_{DDA(out)}$	P	DAC1658Q: 3.3 V analog power supply
			DAC1653Q: 2.5 V or 3.3 V analog power supply
64	$V_{DDA(out)}$	P	DAC1658Q: 3.3 V analog power supply
			DAC1653Q: 2.5 V or 3.3 V analog power supply
65	$V_{DDA(1V2)}$	P	1.2 V analog power supply
66	IOUTB_P	O	DAC B output current
67	IOUTB_N	O	complementary DAC B output current
68	$V_{DDA(1V2)}$	P	1.2 V analog power supply
69	$V_{DDA(1V2)}$	P	1.2 V analog power supply
70	IOUTA_N	O	complementary DAC A output current
71	IOUTA_P	O	DAC A output current
72	$V_{DDA(1V2)}$	P	1.2 V analog power supply

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DDA(out)}$	analog output supply voltage	DAC1658Q: 3.3 V	–0.5	+4.6	V
		DAC1653Q: 2.5 V or 3.3 V	–0.5	+4.6	V
$V_{DDD(1V2)}$	digital supply voltage (1.2 V)		–0.5	+1.5	V
$V_{DDA(1V2)}$	analog supply voltage (1.2 V)		–0.5	+1.5	V
V_I	input voltage	input pins referenced to GND	–0.5	<tbd>	V
V_O	output voltage	pins IOUTA_P, IOUTA_N, IOUTB_P, IOUTB_N, IOUTC_P, IOUTC_N, IOUTD_P, IOUTD_N; IO0; IO1; IO2; IO3; referenced to GND	–0.5	+4.6	V
$V_{DDD(IO)}$	I/O digital supply voltage	pins SDO, SDIO,SCLK, SCS_N, RESET_N, JTAG, IO0, RF_ENABLE/IO1	–0.5	2.1	V
$V_{DDD(SO)}$	differential SYNC voltage	pins SYNC_AB_P/N and SYNC_CD_P/N	–0.5	2.1	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–40	+85	°C
T_j	junction temperature		–40	+125	°C

8. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
JEDEC 4L board					
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	<tbd>	K/W
$R_{th(j-c)}$	thermal resistance from junction to case		[1]	<tbd>	K/W
Application board					
$R_{th(j-a)}$	thermal resistance from junction to ambient	6 layers	[2]	<tbd>	K/W
		8 layers	[2]	<tbd>	K/W
		12 layers	[2]	<tbd>	K/W

[1] In compliance with JEDEC test board; in free air with 64 thermal vias, class 5.

[2] In free air with 64 thermal vias, class 5.

9. Static characteristics

9.1 Common characteristics

Table 5. Characteristics

$V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; R_L = 50 Ω ; $I_{O(fs)}$ = 20 mA; maximum sample rate used; external PLL; no inverse (sinus x) / x; no output correction; output level = 1 V (p-p); unless otherwise specified.

Symbol	Parameter	Conditions	Test[1]	Min	Typ	Max	Unit
V_{DDA}	analog supply voltage (3.3 V)	DAC1658Q: 3.3 V	C	3.15	3.3	3.45	V
		DAC1653Q: 2.5 V or 3.3 V	C	2.38	2.5 or 3.3	3.45	V
$V_{DDD(1V2)}$	digital supply voltage (1.2 V)		C	1.14	1.2	1.26	V
$V_{DDA(1V2)}$	analog supply voltage (1.2 V		C	1.1	1.2	1.3	V
$V_{DDD(IO)}$	I/O digital supply voltage	1.2 V or 1.8 V for IOs and SPI signals	C	1.14	1.2	2.1	V
			C	1.14	1.8	2.1	V
$V_{DDD(SO)}$	differential digital supply voltage		C	1.14	1.2	2.1	V
			C	1.14	1.8	2.1	V
Clock inputs (pins CLKIN_P, CLKIN_N)							
V_i	input voltage	$\|V_{gpd}\|$ < 50 mV	C	[2] 825	-	<tbd>	mV
V_{idth}	input differential threshold voltage	$\|V_{gpd}\|$ < 50 mV	C	[2] −100	-	+100	mV
R_i	input resistance		D	-	100	-	Ω
C_i	input capacitance		D	-	<tbd>	-	pF
Digital inputs/outputs (SYSREF_W_P/SYSREF_W_N, SYSREF_E_P/SYSREF_E_N)							
V_i	input voltage	$\|V_{gpd}\|$ < 50 mV	C	[2] 825	-	<tbd>	mV
V_{idth}	input differential threshold voltage	$\|V_{gpd}\|$ < 50 mV	C	[2] −100	-	+100	mV
R_i	input resistance		D	-	100	-	Ω
C_i	input capacitance		D	-	<tbd>	-	pF
Digital inputs (pins SDO, SDIO, SCLK, SCS_N, RESET_N, IO0, IO1, IO2, IO3)							
V_{IL}	LOW-level input voltage		C	GND	-	$0.3V_{DDD(IO)}$	V
V_{IH}	HIGH-level input voltage		C	$0.7V_{DDD(IO)}$	-	$V_{DDD(IO)}$	V
Digital inputs (VINx_P/VINx_N) following the LV-OIF-11G-SR; CML format							
V_{cm}	common-mode voltage	AC coupling is mandatory; controlled by SPI register	C	0.580	-	1.126	V

Table 5. Characteristics *...continued*

$V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; R_L = 50 Ω ; $I_{O(fs)}$ = 20 mA; maximum sample rate used; external PLL; no inverse (sinus x) / x; no output correction; output level = 1 V (p-p); unless otherwise specified.

Symbol	Parameter	Conditions	Test[1]	Min	Typ	Max	Unit
$V_{pp-diff}$	differential peak-to-peak voltage	at 6 Gbps	C	80	-	-	mV
		at 7.5 Gbps	C	80	-	-	mV
		at 10 Gbps	C	110	-	-	mV
Z_{diff}	differential impedance	controlled by SPI register	I	71	100	190	Ω
Hi-Z_{diff}	tri-state observed impendance		D	-	64	-	kΩ
DR	data rate		D	1	-	10	Gbps
Digital outputs (pins SYNC_OUT_P and SYNC_OUT_N)							
V_{cm}	common-mode voltage	controlled by SPI register			-		
		V_{DDDdif} = 1.8 V	D	1.0	-	1.7	V
		V_{DDDdif} = 1.3 V	D	0.4	-	1.2	V
		V_{DDDdif} = 1.2 V	D	0.4	-	1.1	V
$V_{O(diff)(swing)}$	swing differential output voltage		D	100	-	1200	mV
Digital outputs (pins SDO, SDIO)							
V_{OL}	LOW-level output voltage		C	-	-	$0.3V_{DDDIO}$	V
V_{OH}	HIGH-level output voltage		C	$0.7V_{DDDIO}$	-	-	V
Reference voltage output (pin GAPOUT)							
$V_{O(ref)}$	reference output voltage	T_{amb} = 25 °C	I	-	0.70	-	V
$I_{O(ref)}$	reference output current	external voltage = 0.70 V	D	-	<tbd>	-	µA
$\Delta V_{O(ref)}$	reference output voltage variation		D	-	<tbd>	-	ppm/°C
Analog auxiliary outputs (only for DAC1653Q: connected internally to the outputs pins OUTx_P/OUTx_N)							
$I_{O(fs)}$	full-scale output current	auxiliary DACs; differential inputs (normal resolution)	I	-	4.4	-	mA
		auxiliary DACs; differential inputs (high resolution)	I	-	77.2	-	µA
$V_{O(aux)}$	auxiliary output voltage		C	0	-	2	V
$N_{DAC(aux)mono}$	auxiliary DAC monotonicity	guaranteed	D	-	10	-	bits

Table 5. Characteristics *…continued*

$V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; R_L = 50 Ω ; $I_{O(fs)}$ = 20 mA; maximum sample rate used; external PLL; no inverse (sinus x) / x; no output correction; output level = 1 V (p-p); unless otherwise specified.

Symbol	Parameter	Conditions	Test[1]	Min	Typ	Max	Unit
DAC output timing							
f_s	sampling rate	DAC165xQ1G5	C	-	-	1500	Msps
		DAC165xQ1G25	C	-	-	1250	Msps
		DAC165xQ1G0	C	-	-	1000	Msps
t_s	settling time	to = ±0.5LSB	D	-	20	-	ns

[1] D = guaranteed by design; C = guaranteed by characterization; I = 100 % industrially tested.

[2] $|V_{gpd}|$ represents the ground potential difference voltage. This is the voltage that results from current flowing through the finite resistance and the inductance between the receiver and the driver circuit ground voltages.

9.2 Specific characteristics

Table 6. Specific characteristics

V_{DDA1V2} = 1.2 V; V_{DDD1V2} = 1.2 V; Typical values measured at T_{amb} = +25 °C; R_L = 50 Ω; $I_{O(fs)}$ = 20 mA; maximum sample rate used; no inverse (sinus x) / x; no output correction; output level = 1 V (p-p); unless otherwise specified.

Symbol	Parameter	Conditions	Test	DAC1658Q: High common-mode			DAC1653Q: Low common-mode			Unit
				Min	Typ	Max	Min	Typ	Max	
Currents										
I_{DDA}	analog supply current (3.3 V)	all use cases	C	-	126	-	-	246	-	mA
$I_{DDD(IO)}$	digital supply current for IO pins	Link to SPI IO0/IO1/IO2/IO3 activity	C	-	2	-	-	2	-	mA
$I_{DDD(SYNC)}$	digital supply current for SYNC pins	$V_{DDD(diff)}$ = 1.2 V	C	-	22	-	-	22	-	mA
		$V_{DDD(diff)}$ = 1.8 V	C	-	38	-	-	38	-	mA
I_{DDD}	digital supply current	NCO off;×2 interpolation;; MDS off; invsinc off, phase correction off								
		f_s = 983.04 Msps	C	-	394	-	-	394	-	mA
		f_s = 1228.8 Msps	C	-	<tbd>	-	-	<tbd>	-	mA
		f_s = 1474.56 Msps	C	-	548	-	-	548	-	mA
		f_s = 1760.00 Msps	C	-	<tbd>	-	-	<tbd>	-	mA
		NCO on at 150 MHz;×2 interpolation;; MDS off; invsinc off, phase correction on								
		f_s = 983.04 Msps	C	-	<tbd>	-	-	<tbd>	-	mA
		f_s = 1228.8 Msps	C	-	<tbd>	-	-	<tbd>	-	mA
		f_s = 1474.56 Msps	C	-	680	-	-	680	-	mA
		f_s = 1760.00 Msps	C	-	<tbd>	-	-	<tbd>	-	mA
$I_{DDA(1V2)}$	analog supply current	$V_{DDA(1V2)}$ = 1.2 V	C	-	412	-	-	412	-	mA

Table 6. Specific characteristics *…continued*

V_{DDA1V2} = 1.2 V; V_{DDD1V2} = 1.2 V; Typical values measured at T_{amb} = +25 °C; R_L = 50 Ω; $I_{O(fs)}$ = 20 mA; maximum sample rate used; no inverse (sinus x) / x; no output correction; output level = 1 V (p-p); unless otherwise specified.

Symbol	Parameter	Conditions	Test	DAC1658Q: High common-mode			DAC1653Q: Low common-mode			Unit
				Min	Typ	Max	Min	Typ	Max	
Power										
P_{tot}	total power dissipation	NCO off;×2 interpolation;; MDS off; invsinc off, phase correction off								
		V_{DDA} = 3.3 V; all V_{DDD} = 1.2 V								
		f_s = 983.04 Msps; eight JESD204B lanes at 4.9152 Gbps	C	-	1486	-	-	1982	-	mW
		f_s = 1228.8 Msps; eight JESD204B lanes at 6.144 Gbps	C	-	<tbd>	-	-	<tbd>	-	mW
		f_s = 1474.56 Msps; eight JESD204B lanes at 7.3728 Gbps	C	-	1770	-	-	2166	-	mW
		V_{DDA} = 2.5 V; all V_{DDD} = 1.2 V								
		f_s = 983.04 Msps; eight JESD204B lanes at 4.9152 Gbps	C		n.a.		-	1786	-	mW
		f_s = 1228.8 Msps; eight JESD204B lanes at 6.144 Gbps	C		n.a.		-	<tbd>	-	mW
		f_s = 1474.56 Msps; eight JESD204B lanes at 7.3728 Gbps	C		n.a.		-	1970	-	mW
		full power-down	C	-	12	-	-	12	-	mW
Analog outputs (pins IOUTA_P, IOUTA_N, IOUTB_P, IOUTB_N)										
$I_{O(fs)}$	full-scale output current		D	8.1	-	34	8.1	-	34	mA
$I_{O(dc)}$	DC output current	this DC offset is to be taken into account into filter design and component connection	D	-	4	-	-	4	-	mA

Table 6. Specific characteristics *…continued*

V_{DDA1V2} = 1.2 V; V_{DDD1V2} = 1.2 V; Typical values measured at T_{amb} = +25 °C; R_L = 50 Ω; $I_{O(fs)}$ = 20 mA; maximum sample rate used; no inverse (sinus x) / x; no output correction; output level = 1 V (p-p); unless otherwise specified.

Symbol	Parameter	Conditions	Test	DAC1658Q: High common-mode			DAC1653Q: Low common-mode			Unit
				Min	Typ	Max	Min	Typ	Max	
V_O	output voltage		D	1.5	-	V_{DDA}	0	-	1.8	V
$V_{O(cm)}$	common-mode output voltage		D	2.2	3.05	-	-	0.25	-	V
R_o	output resistance		D	-	250	-	-	250	-	kΩ
C_o	differential output capacitance		D	-	5	-	-	5	-	pF

[1] D = guaranteed by design; C = guaranteed by characterization; I = 100 % industrially tested.

10. Dynamic characteristics

Table 7. Dynamic characteristics DAC165xQ1G5

V_{DDA1V2} = 1.2 V; V_{DDD1V2} = 1.2 V; Typical values measured at T_{amb} = +25 °C; RL = 50 Ω ; $I_{O(fs)}$ = 20 mA; maximum sample rate used; no auxiliary DAC; no inverse (sinus x) / x; no output correction; output level = 1 V (p-p); unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	DAC1658Q: High common-mode			DAC1653Q: Low common-mode			Unit
				Min	Typ	Max	Min	Typ	Max	
SFDR	spurious-free dynamic range	f_{data} = 737.28 MHz; f_s = 1474.56 Msps; B = f_s / 2								
		V_{DDA} = 3.3 V; f_o = 20 MHz								
		at −1 dBFS	I	-	85	-	-	85	-	dBc
		at −7 dBFS	I	-	<tbd>	-	-	<tbd>	-	dBc
		at −14 dBFS	I	-	<tbd>	-	-	<tbd>	-	dBc
		V_{DDA} = 3.3 V; f_o = 150 MHz								
		at −1 dBFS	I	-	83	-	-	81	-	dBc
		at −7 dBFS	I	-	<tbd>	-	-	<tbd>	-	dBc
		at −14 dBFS	I	-	<tbd>	-	-	<tbd>	-	dBc
		V_{DDA} = 2.5 V; f_o = 20 MHz								
		at −1 dBFS	I		n.a.		-	83	-	dBc
		at −7 dBFS	I		n.a.		-	<tbd>	-	dBc
		at −14 dBFS	I		n.a		-	<tbd>	-	dBc
		V_{DDA} = 2.5 V; f_o = 150 MHz								
		at −1 dBFS	I		n.a.		-	81	-	dBc
		at −7 dBFS	I		n.a.		-	<tbd>	-	dBc
		at −14 dBFS	I		n.a.		-	<tbd>	-	dBc
$SFDR_{(RBW)}$	spurious-free dynamic range restricted bandwidth	V_{DDA} = 3.3 V; f_o = 230 MHz B = 300 MHz								
		at −1 dBFS	I	-	<tbd>	-	-	<tbd>	-	dBc
IMD3	third-order intermodulation distortion	V_{DDA} = 3.3 V; f_{o1} = 20 MHz; f_{o2} = 21 MHz; −7 dBFS per tone	I	-	86	-	-	86	-	dBc
		V_{DDA} = 3.3 V; f_{o1} = 230 MHz; f_{o2} = 231 MHz; −7 dBFS per tone	I	-	84	-	-	82	-	dBc

Table 7. Dynamic characteristics DAC165xQ1G5 *…continued*

V_{DDA1V2} = 1.2 V; V_{DDD1V2} = 1.2 V; Typical values measured at T_{amb} = +25 °C; RL = 50 Ω ; $I_{O(fs)}$ = 20 mA; maximum sample rate used; no auxiliary DAC; no inverse (sinus x) / x; no output correction; output level = 1 V (p-p); unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	DAC1658Q: High common-mode			DAC1653Q: Low common-mode			Unit
				Min	Typ	Max	Min	Typ	Max	
ACPR	adjacent channel power ratio	f_o = 40 MHz								
		1 WCDMA carrier; B = 5 MHz	C	-	82	-	-	82	-	dBc
		4 WCDMA carriers; B = 20 MHz	C	-	75	-	-	75	-	dBc
ALT-ACPR	Alternate channel power ratio	f_o = 40 MHz								
		1 WCDMA carrier; B = 5 MHz	C	-	<tbd>	-	-	<tbd>	-	dBc
		4 WCDMA carriers; B = 20 MHz	C	-	<tbd>	-	-	<tbd>	-	dBc
NSD	noise spectral density	f_o = 20 MHz at −1 dBFS	C	-	-164	-	-	−162	-	dBm/Hz

[1] D = guaranteed by design; C = guaranteed by characterization; I = 100 % industrially tested.

Table 8. Dynamic characteristics DAC165xQ1G25

V_{DDA1V2} = 1.2 V; V_{DDD1V2} = 1.2 V; Typical values measured at T_{amb} = +25 °C; RL = 50 Ω ; $I_{O(fs)}$ = 20 mA; maximum sample rate used; no auxiliary DAC; no inverse (sinus x) / x; no output correction; output level = 1 V (p-p); unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	High common-mode			Low common-mode			Unit
				Min	Typ	Max	Min	Typ	Max	
SFDR	spurious-free dynamic range	f_{data} = 614.4 MHz; f_s = 1228.8 Msps; B = f_s / 2								
		V_{DDA} = 3.3 V; f_o = 20 MHz								
		at −1 dBFS	I	-	85	-	-	85	-	dBc
		at −7 dBFS	I	-	<tbd>	-	-	<tbd>	-	dBc
		at −14 dBFS	I	-	<tbd>	-	-	<tbd>	-	dBc
		V_{DDA} = 3.3 V; f_o = 150 MHz								
		at −1 dBFS	I	-	83	-	-	81	-	dBc
		at −7 dBFS	I	-	<tbd>	-	-	<tbd>	-	dBc
		at −14 dBFS	I	-	<tbd>	-	-	<tbd>	-	dBc
		V_{DDA} = 2.5 V; f_o = 20 MHz								
		at −1 dBFS	I		n.a.		-	83	-	dBc
		at −7 dBFS	I		n.a.		-	<tbd>	-	dBc
		at −14 dBFS	I		n.a		-	<tbd>	-	dBc
		V_{DDA} = 2.5 V; f_o = 150 MHz								
		at −1 dBFS	I		n.a.		-	81	-	dBc
		at −7 dBFS	I		n.a.		-	<tbd>	-	dBc
		at −14 dBFS	I		n.a.		-	<tbd>	-	dBc
$SFDR_{(RBW)}$	spurious-free dynamic range restricted bandwidth	V_{DDA} = 3.3 V; f_o = 230 MHz B = 300 MHz								
		at −1 dBFS	I	-	<tbd>	-	-	<tbd>	-	dBc
IMD3	third-order intermodulation distortion	V_{DDA} = 3.3 V; f_{o1} = 20 MHz; f_{o2} = 21 MHz; −7 dBFS per tone	I	-	86	-	-	86	-	dBc
		V_{DDA} = 3.3 V; f_{o1} = 230 MHz; f_{o2} = 231 MHz; −7 dBFS per tone	I	-	84	-	-	82	-	dBc
ACPR	adjacent channel power ratio	f_o = 40 MHz								
		1 WCDMA carrier; B = 5 MHz	C	-	82	-	-	82	-	dBc
		4 WCDMA carriers; B = 20 MHz	C	-	75	-	-	75	-	dBc

Table 8. Dynamic characteristics DAC165xQ1G25 *…continued*

V_{DDA1V2} = 1.2 V; V_{DDD1V2} = 1.2 V; Typical values measured at T_{amb} = +25 °C; RL = 50 Ω ; $I_{O(fs)}$ = 20 mA; maximum sample rate used; no auxiliary DAC; no inverse (sinus x) / x; no output correction; output level = 1 V (p-p); unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	High common-mode			Low common-mode			Unit
				Min	Typ	Max	Min	Typ	Max	
ALT-ACPR	Alternate channel power ratio	f_o = 40 MHz								
		1 WCDMA carrier; B = 5 MHz	C	-	<tbd>	-	-	<tbd>	-	dBc
		4 WCDMA carriers; B = 20 MHz	C	-	<tbd>	-	-	<tbd>	-	dBc
NSD	noise spectral density	f_o = 20 MHz at −1 dBFS	C	-	-164	-	-	−162	-	dBm/Hz

[1] D = guaranteed by design; C = guaranteed by characterization; I = 100 % industrially tested.

Table 9. Dynamic characteristics DAC16QxD1G0

V_{DDA1V2} = 1.2 V; V_{DDD1V2} = 1.2 V; Typical values measured at T_{amb} = +25 °C; RL = 50 Ω ; $I_{O(fs)}$ = 20 mA; maximum sample rate used; no auxiliary DAC; no inverse (sinus x) / x; no output correction; output level = 1 V (p-p); unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	High common-mode			Low common-mode			Unit
				Min	Typ	Max	Min	Typ	Max	
SFDR	spurious-free dynamic range	f_{data} = 491.52 MHz; f_s = 983.04 Msps; B = f_s / 2								
		V_{DDA} = 3.3 V; f_o = 20 MHz								
		at −1 dBFS	I	-	85	-	-	85	-	dBc
		at −7 dBFS	I	-	<tbd>	-	-	<tbd>	-	dBc
		at −14 dBFS	I	-	<tbd>	-	-	<tbd>	-	dBc
		V_{DDA} = 3.3 V; f_o = 150 MHz								
		at −1 dBFS	I	-	83	-	-	81	-	dBc
		at −7 dBFS	I	-	<tbd>	-	-	<tbd>	-	dBc
		at −14 dBFS	I	-	<tbd>	-	-	<tbd>	-	dBc
		V_{DDA} = 2.5 V; f_o = 20 MHz								
		at −1 dBFS	I		n.a.		-	83	-	dBc
		at −7 dBFS	I		n.a.		-	<tbd>	-	dBc
		at −14 dBFS	I		n.a		-	<tbd>	-	dBc
		V_{DDA} = 2.5 V; f_o = 150 MHz								
		at −1 dBFS	I		n.a.		-	81	-	dBc
		at −7 dBFS	I		n.a.		-	<tbd>	-	dBc
		at −14 dBFS	I		n.a.		-	<tbd>	-	dBc
$SFDR_{(RBW)}$	spurious-free dynamic range restricted bandwidth	V_{DDA} = 3.3 V; f_o = 230 MHz B = 300 MHz								
		at −1 dBFS	I	-	<tbd>	-	-	<tbd>	-	dBc
IMD3	third-order intermodulation distortion	V_{DDA} = 3.3 V; f_{o1} = 20 MHz; f_{o2} = 21 MHz; −7 dBFS per tone	I	-	86	-	-	86	-	dBc
		V_{DDA} = 3.3 V; f_{o1} = 230 MHz; f_{o2} = 231 MHz; −7 dBFS per tone	I	-	84	-	-	82	-	dBc
ACPR	adjacent channel power ratio	f_o = 40 MHz								
		1 WCDMA carrier; B = 5 MHz	C	-	82	-	-	82	-	dBc
		4 WCDMA carriers; B = 20 MHz	C	-	75	-	-	75	-	dBc

Table 9. Dynamic characteristics DAC16QxD1G0 *…continued*

V_{DDA1V2} = 1.2 V; V_{DDD1V2} = 1.2 V; Typical values measured at T_{amb} = +25 °C; RL = 50 Ω ; $I_{O(fs)}$ = 20 mA; maximum sample rate used; no auxiliary DAC; no inverse (sinus x) / x; no output correction; output level = 1 V (p-p); unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	High common-mode			Low common-mode			Unit
				Min	Typ	Max	Min	Typ	Max	
ALT-ACPR	Alternate channel power ratio	f_o = 40 MHz								
		1 WCDMA carrier; B = 5 MHz	C	-	<tbd>	-	-	<tbd>	-	dBc
		4 WCDMA carriers; B = 20 MHz	C	-	<tbd>	-	-	<tbd>	-	dBc
NSD	noise spectral density	f_o = 20 MHz at −1 dBFS	C	-	-164	-	-	−162	-	dBm/Hz

[1] D = guaranteed by design; C = guaranteed by characterization; I = 100 % industrially tested.

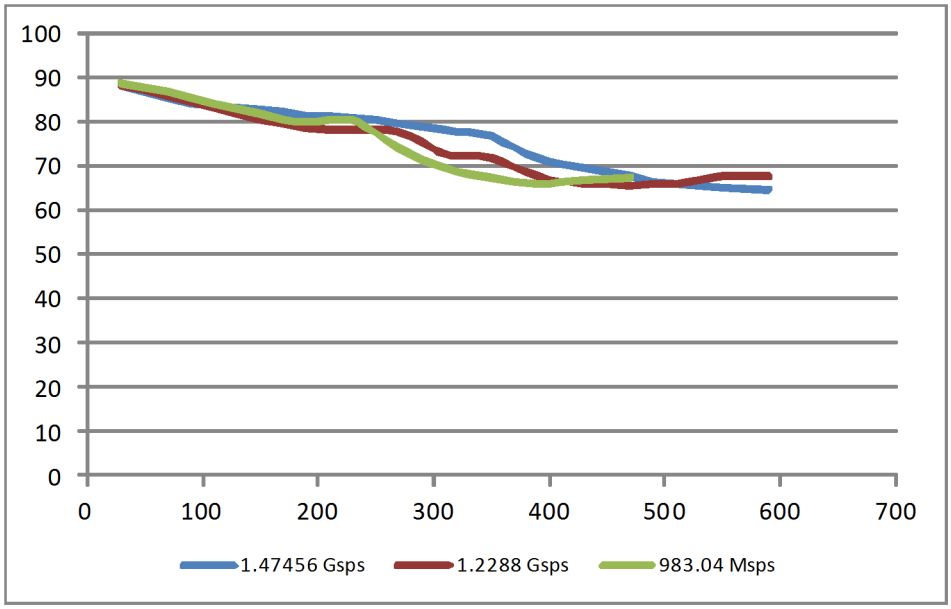


Fig 3. SFDR(dBc) over Nyquist depending of fout (MHz)

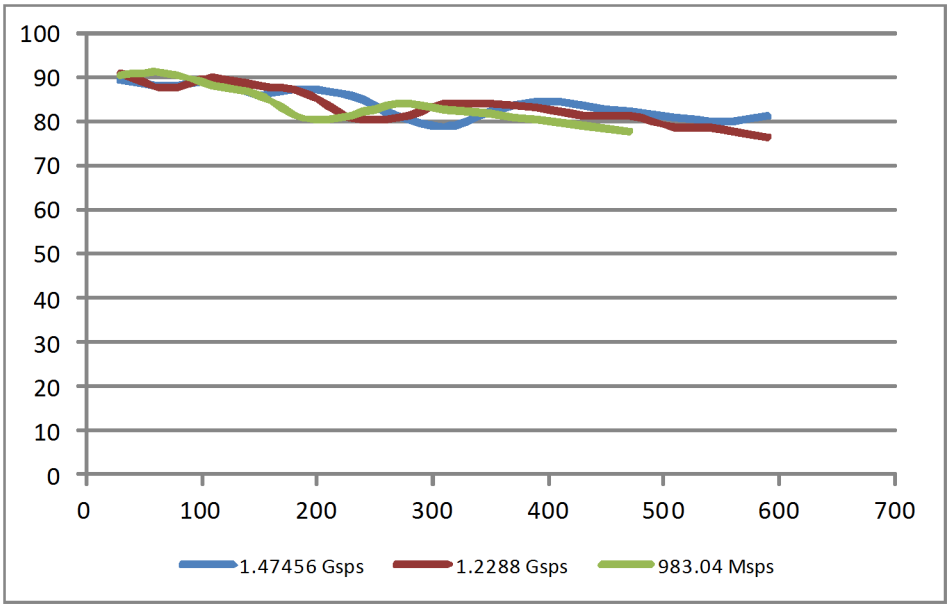


Fig 4. SFDR(dBc) ecxluding HD2 and HD3 over Nyquist depending of fout (MHz)

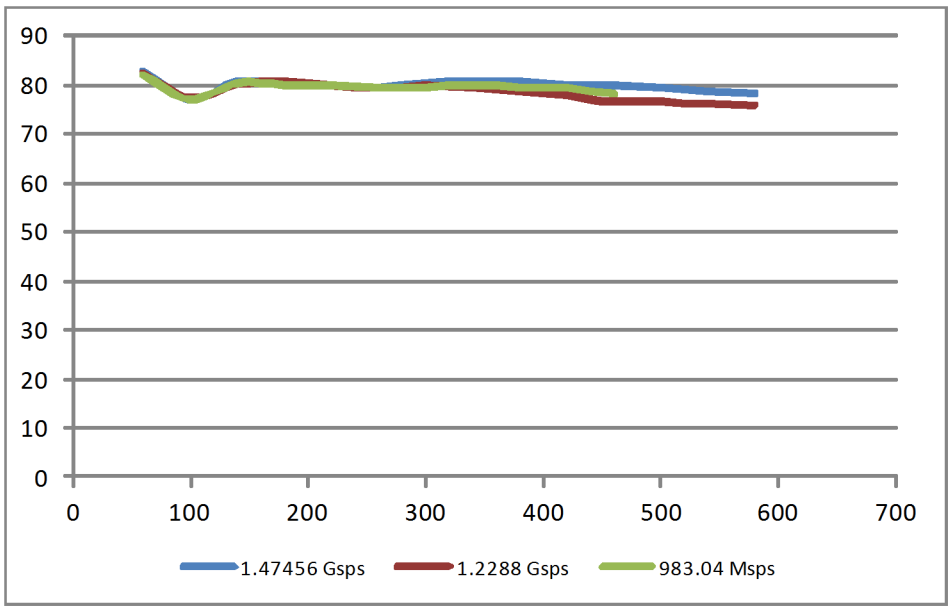


Fig 5. ACPR(dBc) LTE 1 carrier 5 MHz depending of fout (MHz)

11. Application information

11.1 General description

The DAC165xQ is a quad 16-bit DAC operating up to 1.50 Gsps. A maximum input data rate up to 750 Msps is supported to enable more capability for wideband and multicarrier systems. The incorporated quadrature modulators and 40-bit Numerically Controlled Oscillators (NCOs) simplify the frequency selection of the system. This is also possible because of the ×2, ×4 or ×8 interpolation filters which remove undesired images.

The DAC165xQ embeds four DAC channels (A, B, C and D) that can be configured as a single quad DAC (A/B/C/D) or two dual DACs (A/B and C/D). The two NCOs are linked to the A/B and the C/D dual DACs, respectively. Regarding the quad/dual mode used, the eight JESD204B lanes are configured as one single link configuration JESD204 link (one SYNC signal for a specified number of lanes), or dual link configuration JESD204B links (two SYNC signals associated with a specified number of lanes).

The DAC165xQ supports the following JESD204B key features:

- 10-bit/8-bit decoding
- Code group synchronization
- Initial-Lane Alignment (ILA)
- $1 + x^{14} + x^{15}$ scrambling polynomial
- Character replacement
- TX/RX synchronization management via synchronization signals
- Multiple Converter Device Alignment-Multiple Lanes (MCDA-ML) device
- Number L of serial lanes: 1, 2, 4, 8 (see LMF configuration table)
- Number M of data converters: 1, 2 or 4 (see LMF configuration table)
- Number F of octets per frame: 1, 2, 4, 6, 8 (see LMF configuration table)
- Number S of samples per frame: 1, 2 (see LMF configuration table)
- Embedded test pattern (PRBS7; PRBS15; PRBS23, PRBS31, JTSPAT, STLTP)

The DAC165xQ can be interfaced with any logic device that features high-speed SERializer/DESerializer (SERDES) functionality. This macro is now widely available in Field-Programmable Gate Array (FPGA) of different vendors. Standalone SERDES ICs can also be used.

The device includes polarity swapping for each of the lanes and additionally offers lane swapping to enhance the intrinsic board layout simplification of the JESD204B standard. Each physical lane can be configured logically as any lane number.

This device is MCDA-ML compliant, offering inter-lane alignment between several devices. An IDT proprietary mechanism in combination with the JESD204B subclass I clause enables maintenance of sample alignment between devices up to the final analog output stage. Output samples are automatically aligned to the SYSREF signal generated by a dedicated IC or by the FPGA itself. A system with several DAC165xQs can produce data with a guaranteed alignment of 1 DAC output clock period. The DAC165xQ incorporates two differential SYSREF ports (located on opposite sides of the IC). These

can be programmed to act as an input or an output regarding the mode expected for the system (Normal mode, Daisy chain mode). The device also enables independent link reinitialization.

The DAC165xQ generates four complementary current outputs on pins IOUTA_P/IOUTA_N and IOUTB_P/IOUTB_N, IOUTC_P/IOUTC_N, and IOUTD_P/IOUTD_N corresponding to channel 'A', 'B', 'C', and 'D', respectively, providing a nominal full-scale output current of 20 mA. An internal reference is available for the reference current which is externally adjustable using pin VIRES.

The DAC165xQ requires configuration before operating. It features an SPI slave interface to access the internal registers. Some of these registers also provide information about the JESD204B interface status. Optionally, an interrupt capability can be programmed using those registers to ensure ease of use of the device.

Because of the JESD204B standardization, the DAC165xQ does not require any adjustment from the Transmit Logic Device (TLD) to capture the input data streams. Some autolock features can be monitored using the SPI registers.

The DAC165xQ supports the following LMF configuration as described in the JESD204B standard.

Table 10. LMF configuration if DAC165xQ configures in dual JEDS204B links

Link configuration	L-M-F	S[1]	HD[2]
dual link	1-2-4	1	0
dual link	2-2-2	1	0
dual link	4-2-2	2	0
dual link	4-2-1	1	1
single link	2-4-4	1	0
single link	4-2-2	1	0
single link	8-4-2	2	0
single link	8-4-1	1	1

[1] S is the number of samples per frame.

[2] HD is the High-Density bit as described in the JESD204B specification.

A new IDT auto-mute feature enables switching off of the RF output signal as a result of various internal events occurring.

A signal level detector allows auto-muting of the DAC outputs if they exceed the detection limit.

The DAC165xQ requires supplies of 2.5 V or 3.3 V and 1.2 V. The 1.2 V supply has separate digital and analog power supply pins .

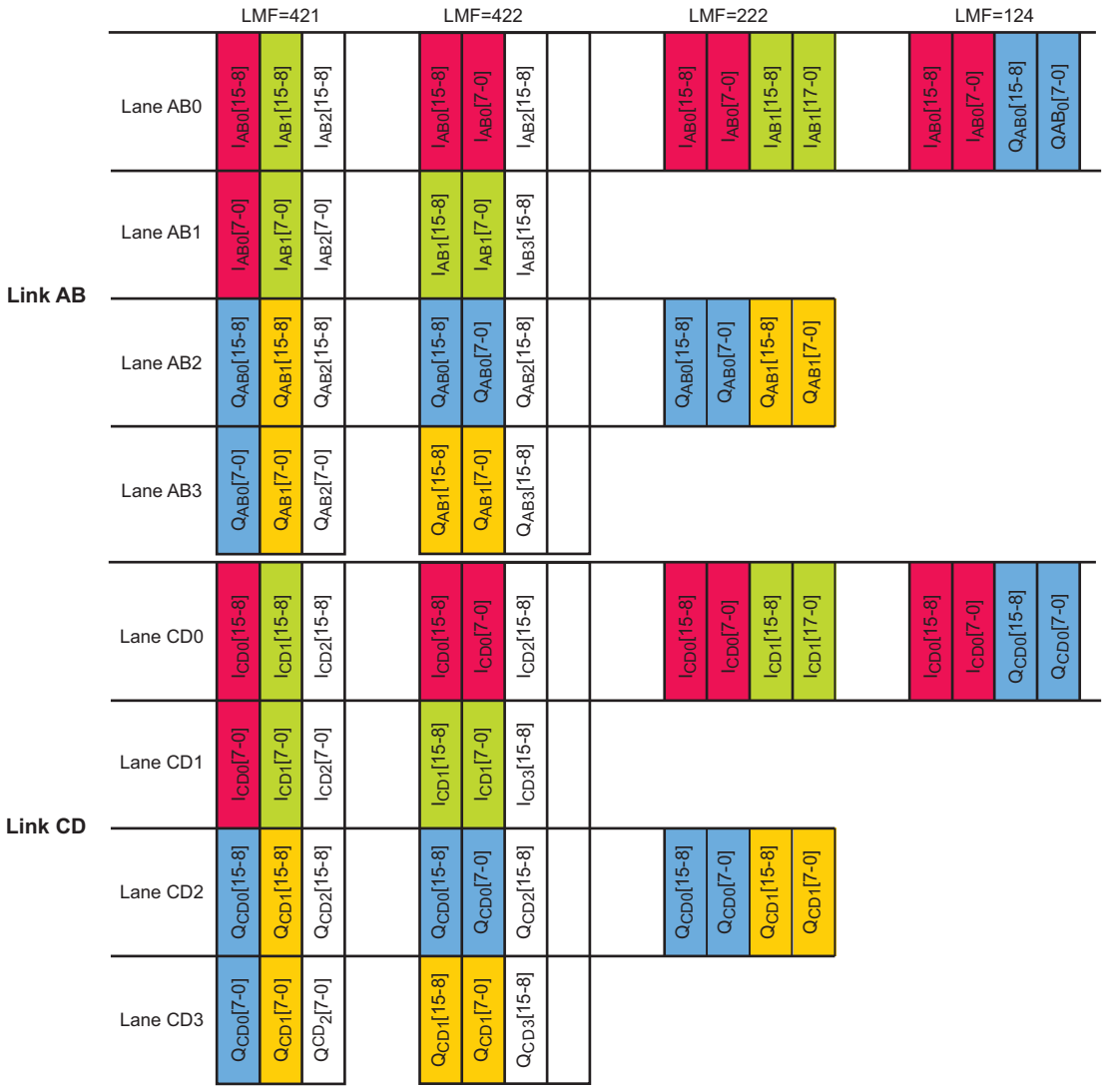


Fig 6. Independent/dual link configuration

11.2 Device operation

The DAC165xQ provides a lot of flexibility in its way of working through its SPI registers. The SPI registers are divided in blocks of registers. Each block is associated with some global functions which are described below.

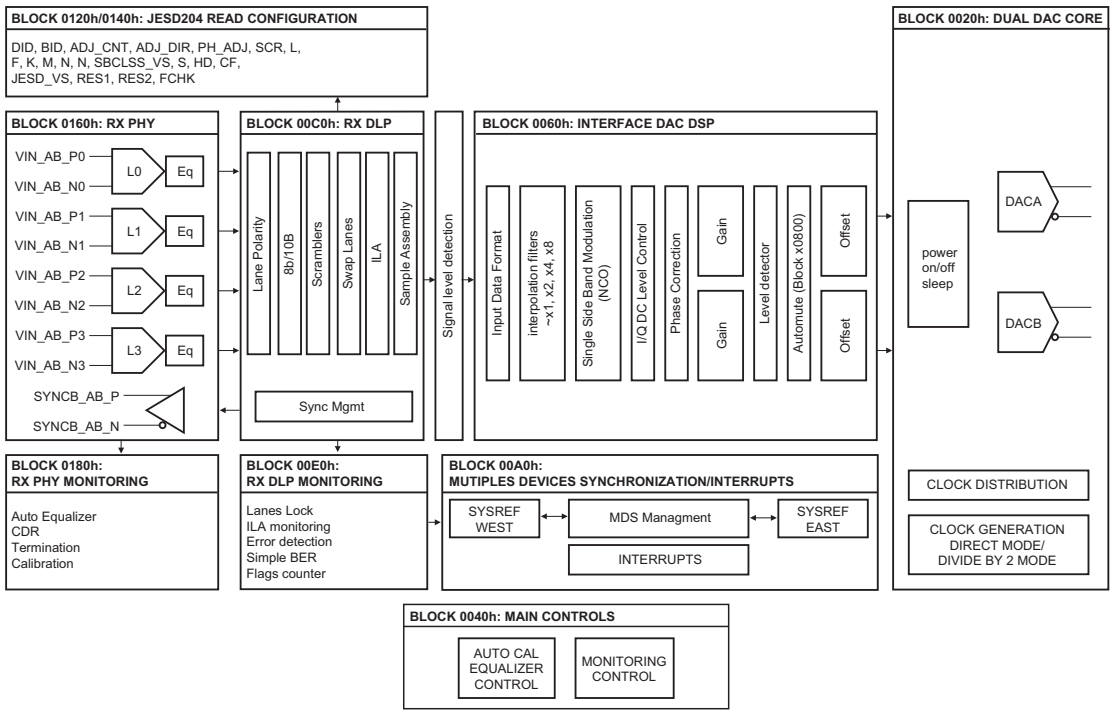


Fig 7. SPI register blocks partition: DAC A/B

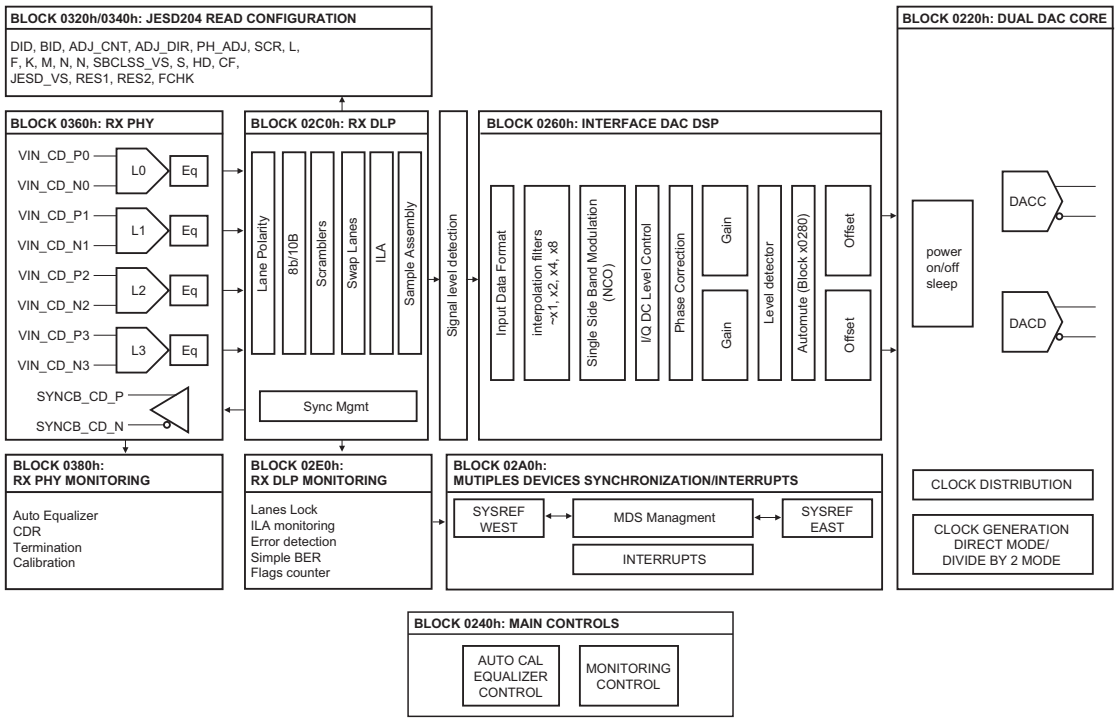


Fig 8. SPI register blocks partition: DAC C/D

11.2.1 SPI configuration block

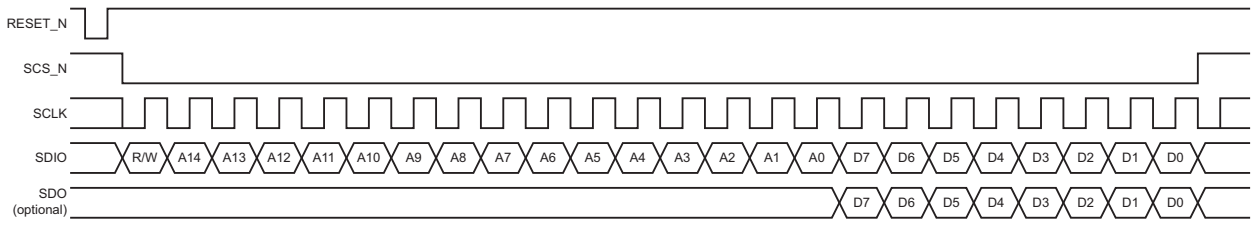
This block of registers specifies how the SPI controller and the identification of the chip work.

11.2.1.1 Protocol description

The DAC165xQ serial interface is a synchronous serial communication port allowing easy interfacing with many industry microprocessors. It provides access to the registers that define the operating modes of the chip in both Write mode and Read mode. The reference voltage of the interface is $V_{DDD(IO)}$. Depending on the power supply level of the SPI master device, it can be set to either 1.2 V or 1.8 V.

This interface can be configured as a 3-wire type (SDIO as bidirectional pin) or a 4-wire type (SDIO and SDO as unidirectional pins, input and output ports, respectively). In both configurations, SCLK acts as the serial clock and SCS_N acts as the serial chip select.

The DAC165xQ SPI-interface is a slave-device. Multiple slave-devices can be attached to the same master interface as long as each device has its own serial chip select signal (SCS_N).



R/W indicates the mode access.

The RESET_N signal is not linked to the SPI interface but enable the reset of the registers to the default values.

Fig 9. SPI protocol

Table 11. Read mode or Write mode access description

R/W	Description
0	Write mode operation
1	Read mode operation

A[14:0] indicates which register is being addressed. If a multiple transfer occurs, this address points to the first register to be accessed.

11.2.1.2 SPI controller configuration

The 3-wire or 4-wire mode is set by bit SPI_4W of register SPI_CFG_A . The default mode is 3-wire mode.

A software SPI reset can be called via bit SPI_RST of register SPI_CFG_A . This reset reinitializes all SPI registers, except register SPI_CFG_A and SPI_CFG_B, to their default settings. Reset the device to its default value at start-up time to avoid any uncontrolled states, even if the DAC165xQ uses the Power-On Reset (POR) module. Only a hardware reset on pin RESET_N can reset to their default values.

The SPI streaming mode is enabled by default. In this mode, the Read or Write process carries on as long as the SCS_N signal is low. The streaming mode requires a first address 'n' to be set at the beginning of the SPI sequence. The following data are associated from this address in an ascending (auto-increment) or descending (auto-decrement) mode. This ascending/descending mode is specified by bit SPI_ASC of register SPI_CONFIG_A . Figure 10 and Figure 11 show the read back of 2 bytes data in a 3-wire mode for the ascendant and descendant mode.

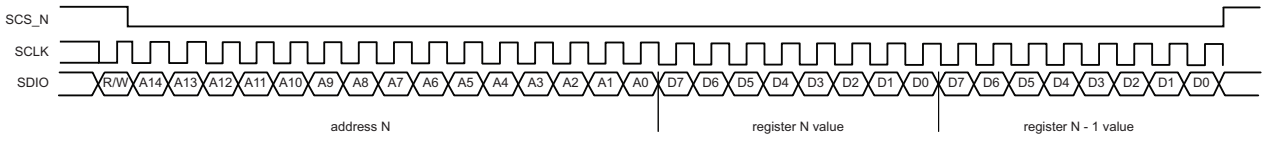


Fig 10. Consecutive 2-byte data readback under descending address

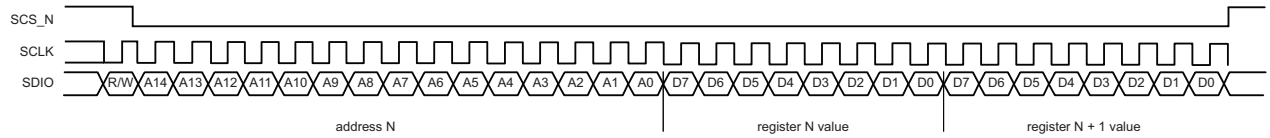


Fig 11. Consecutive 2-byte data readback under ascending address

The streaming mode can be disabled by setting bit SPI_SNGL of register SPI_CONFIG_B . In this single-byte mode, only 1 byte of data can be written or read, whatever the state of the SCS_N signal.

11.2.1.3 Double buffering and Transfer mode

Some register functions (like the NCO frequency value) are split over multiple registers. If this is the case, the first address consists of the LSB byte and the highest address in the MSB byte. When programming these registers sequentially, some unexpected behavior can occur at the DAC output. it is preferable to program this set of registers simultaneously. A double buffering feature is available on some registers allowing sequential programming of the first buffers and transfering the values to the final register simultaneously.

The transfer request is done by setting the TRANSFER_BIT bit of register SPI_CONFIG_C register . The device clears this bit (autoclear) indicating to the SPI master device that the transfer is complete.

The SPI_RBACK_BUFF bit of register SPI_CONFIG_B allows the reading back of the first stage of buffers (in case the register is double buffered)

The following registers are double buffered:

Table 12. Double buffered registers

Address	Register
0062h/0262h/046Ah	NCO_PH_OFFSET_XY_LSB
0063h/0263h/0463h	NCO_PH_OFFSET_XY_MSB
0064h/0264h/0464h	NCO_FREQ_XY_B0
0065h/0265h/0465h	NCO_FREQ_XY_B1
0066h/0266h/0466h	NCO_FREQ_XY_B2
0067h/0267h/0467h	NCO_FREQ_XY_B3
0068h/0268h/0468h	NCO_FREQ_XY_B4
0069h/0269h/0469h	PH_CORR_XY_CTRL_0
006Ah/026Ah/046Ah	PH_CORR_XY_CTRL_1
006Bh/026Bh/046Bh	DAC_X_DGAIN_LSB
006Ch/026Ch/046Ch	DAC_X_DGAIN_MSB
006Dh/026Dh/046Dh	DAC_Y_DGAIN_LSB
006Eh/026Eh/046Eh	DAC_Y_DGAIN_MSB
006Fh/026Fh/046Fh	DAC_OUT_CTRL_XY
0070h/0270h/0470h	DAC_LVL_DET_XY
0071h/0271h/0471h	DAC_X_OFFSET_LSB
0072h/0272h/0472h	DAC_X_OFFSET_MSB

Table 12. Double buffered registers *…continued*

Address	Register
0073h/0273h/0473h	DAC_Y_OFFSET_LSB
0074h/0274h/0474h	DAC_Y_OFFSET_MSB
0075h/0275h/0475h	IQ_LVL_CTRL
0076h/0276h/0476h	I_DC_LVL_XY_LSB
0077h/0277h/0477h	I_DC_LVL_XY_MSB
0078h/0278h/0478h	Q_DC_LVL_XY_LSB
0079h/0279h/0479h	Q_DC_LVL_XY_MSB

11.2.1.4 Device description

Registers CHIP_TYPE, CHIP_ID_0, CHIP_ID_1 and CHIP_VS represent the ID card of the device.

Registers VEND_ID_LSB and VEND_ID_MSB represent the IDT manufacturer identifier.

11.2.1.5 SPI timing description

The SPI interface can operate at a frequency of up to 25 MHz. Figure 12 shows the SPI timing.

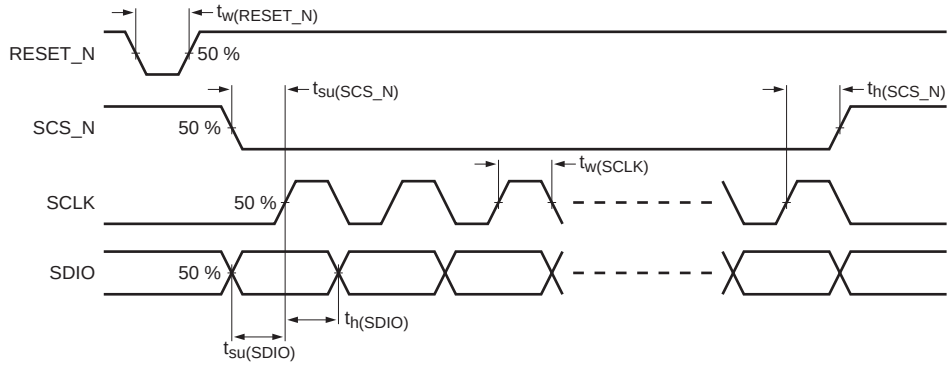


Fig 12. SPI timing diagram

The SPI timing characteristics are given in Table 13.

Table 13. SPI timing characteristics

Symbol	Parameter		Min	Typ	Max	Unit
f_{SCLK}	SCLK frequency		-	-	25	MHz
$t_{w(SCLK)}$	SCLK pulse width		30	-	-	ns
$t_{su(SCS\_N)}$	SCS_N set-up time		20	-	-	ns
$t_{h(SCS\_N)}$	SCS_N hold time		20	-	-	ns
$t_{su(SDIO)}$	SDIO set-up time		10	-	-	ns
$t_{h(SDIO)}$	SDIO hold time		5	-	-	ns
$t_{w(RESET\_N)}$	RESET_N pulse width	[1]	30	-	-	ns

[1] The RESET_N signal is not linked to the SPI interface, but enables the reset of the registers to the default values.

11.2.2 Main device configuration

The registers of block MAIN are used for the main configuration of the DAC165xQ.

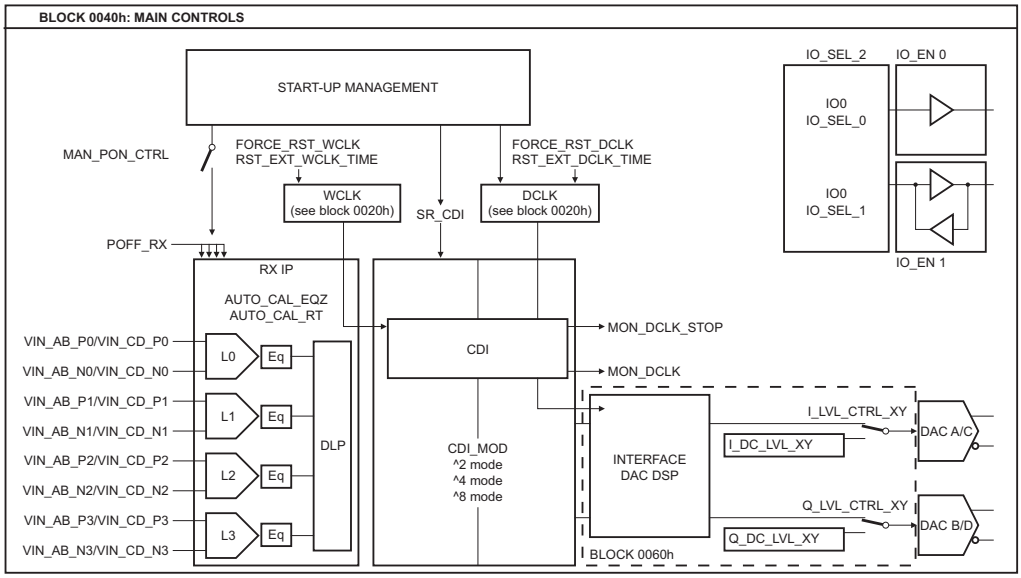


Fig 13. Main controls

At start-up, the two clocks WCLK and DCLK are forced to reset states to avoid that the DAC outputs any dummy signal through bits FORCE_RST_DCLK and FORCE_RST_WCLK of the MAIN_CTRL register . The device configuration has to be done before releasing these two clocks.

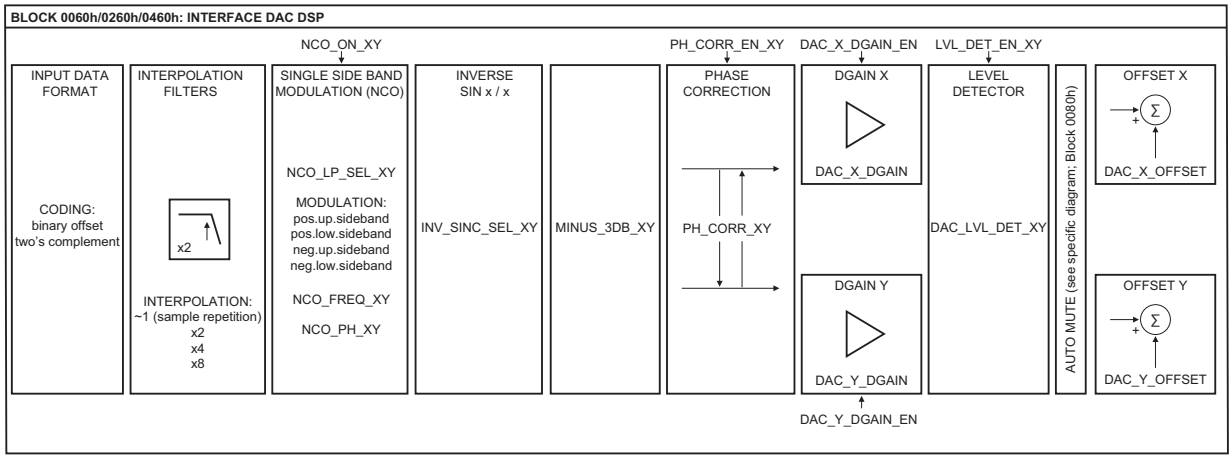
Here are some guidelines to ensure correct SPI programming. As DCLK and WCLK are kept to reset the programming sequence of the registers is not important:

<tbd>

Other SPI configurations can be added using these basic settings.

11.2.3 Interface DAC DSP block

This module is the interface between the data processing in the high-speed serial receiver and the dual DAC core. The controls of the Digital Signal Processing (DSP) of the DAC are specified to set up the interpolation filter, and enable or disable the various gains and offsets of the data digital path. The data signals have already been processed by the Digital Lane Processing . They are provided to this module through the Clock Domain Interface . This module is clocked by the digital clock DCLK.



Block 0060h = DAC A/B

Block 0260h = DAC C/D

Block 0460h = All DACs

Fig 14. Interface DAC DSP overview

11.2.3.1 Input data format

After decoding in the high-speed serial receiver, the data representation can be specified as binary offset coding or as two's complement coding using register CODING_XY_IQ .

11.2.3.2 Finite Impulse Response (FIR) filters

The DAC165xQ provides three interpolation filters described by their coefficients in Table 15. The three interpolation FIR filters have a stop band attenuation of at least 80 dBc and a pass band ripple of less than 0.0005 dB.

The interpolation ratio can be set through register TX_CFG_XY .

Table 14. Interpolation

Symbol	Access	Value	Description
INTERPOLATION[1:0]	R/W		interpolation
		00	no interpolation/~×1 interpolation
		01	×2 interpolation
		10	×4 interpolation
		11	×8 interpolation

The 'no interpolation' or '~×1' (quasi ×1) mode is in fact a degenerated ×2 interpolation mode where the samples are repeated twice.

Remark: The INTERPOLATION setting must be coupled with the DCLK and WCLK clock configurations and with CDI mode .

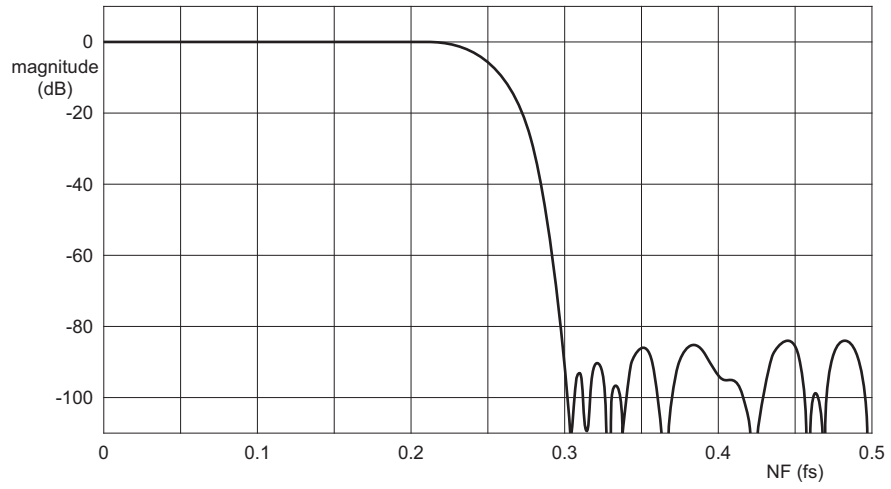


Fig 15. First stage half-band filter response (used in ×2, ×4, and ×8 interpolation)

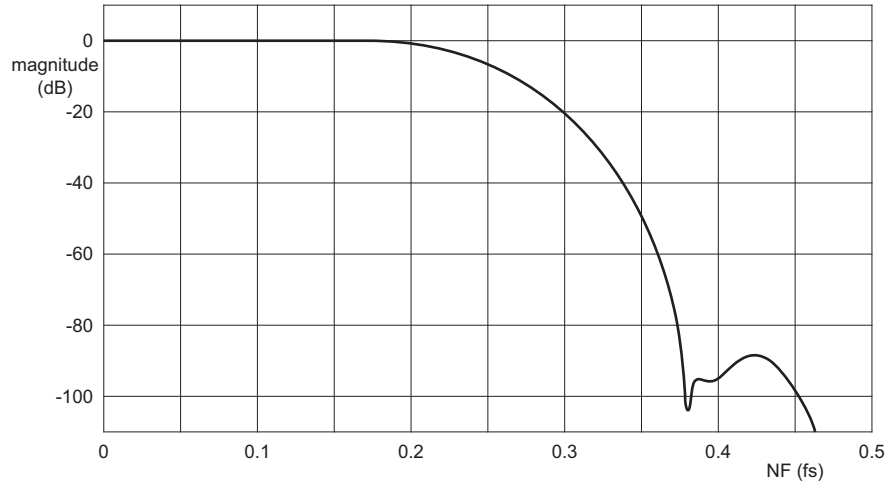


Fig 16. Second stage half-band filter response (used in ×2, ×4, and ×8 interpolation)

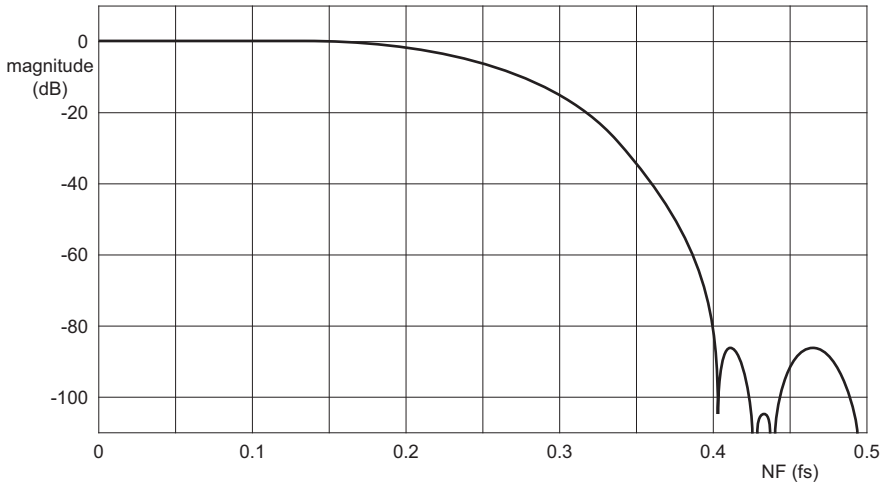


Fig 17. Third stage half-band filter response (used in ×2, ×4, and ×8 interpolation)

Table 15: Interpolation filter coefficients

First interpolation filter			Second interpolation filter			Third interpolation filter		
Lower	Upper	Value	Lower	Upper	Value	Lower	Upper	Value
-	H(27)	+65536	H(11)	-	+32768	H(7)	-	+1024
H(26)	H(28)	+41501	H(10)	H(12)	+20272	H(6)	H(8)	+615
H(25)	H(29)	0	H(9)	H(13)	0	H(5)	H(9)	0
H(24)	H(30)	−13258	H(8)	H(14)	−5358	H(4)	H(10)	−127
H(23)	H(31)	0	H(7)	H(15)	0	H(3)	H(11)	0
H(22)	H(32)	+7302	H(6)	H(16)	+1986	H(2)	H(12)	+27
H(21)	H(33)	0	H(5)	H(17)	0	H(1)	H(13)	0
H(20)	H(34)	−4580	H(4)	H(18)	−654	H(0)	H(14)	−3
H(19)	H(35)	0	H(3)	H(19)	0	-	-	-
H(18)	H(36)	+2987	H(2)	H(20)	+159	-	-	-
H(17)	H(37)	0	H(1)	H(21)	0	-	-	-
H(16)	H(38)	−1951	H(0)	H(22)	−21	-	-	-
H(15)	H(39)	0	-	-	-	-	-	-
H(14)	H(40)	+1250	-	-	-	-	-	-
H(13)	H(41)	0	-	-	-	-	-	-
H(12)	H(42)	-773	-	-	-	-	-	-
H(11)	H(43)	0	-	-	-	-	-	-
H(10)	H(44)	+456	-	-	-	-	-	-
H(9)	H(45)	0	-	-	-	-	-	-
H(8)	H(46)	−252	-	-	-	-	-	-
H(7)	H(47)	0	-	-	-	-	-	-
H(6)	H(48)	+128	-	-	-	-	-	-
H(5)	H(49)	0	-	-	-	-	-	-
H(4)	H(50)	−58	-	-	-	-	-	-

Table 15: Interpolation filter coefficients *...continued*

First interpolation filter			Second interpolation filter			Third interpolation filter		
Lower	Upper	Value	Lower	Upper	Value	Lower	Upper	Value
H(3)	H(51)	0	-	-	-	-	-	-
H(2)	H(52)	+22	-	-	-	-	-	-
H(1)	H(53)	0	-	-	-	-	-	-
H(0)	H(54)	–6	-	-	-	-	-	-

The dependency of the FIR1 output y(m) on its inputs x(m) is defined by Equation 1:

$$y(m) = \frac{1}{H(27)} \times \sum_{n=0}^{n=54} [H(n):x(m-n)] \quad (1)$$

The dependency of the FIR2 output Y(m) on its inputs X(m) is defined by Equation 2:

$$y(m) = \frac{1}{H(11)} \times \sum_{n=0}^{n=22} [H(n):x(m-n)] \quad (2)$$

The dependency of the FIR3 output Y(m) on its inputs X(m) is defined by Equation 3:

$$y(m) = \frac{1}{H(7)} \times \sum_{n=0}^{n=14} [H(n):x(m-n)] \quad (3)$$

11.2.3.3 Single SideBand Modulator (SSBM)

The single sideband modulator is a quadrature modulator that enables the mixing of the I_XY data and Q_XY data with the sine and cosine signals generated by the NCO to generate path X and Y as described in Figure 18.

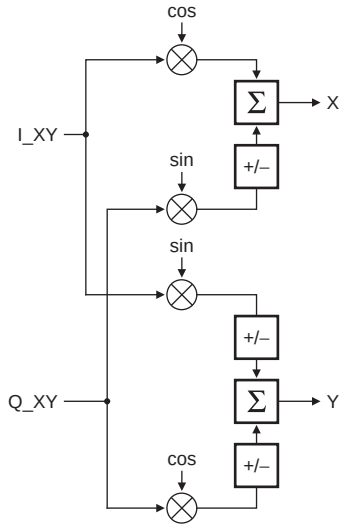


Fig 18. Single sideband modulator principle

Table 16 shows the various possibilities set by register MODULATION .

Table 16. Complex modulator operation mode

MODULATION[2:0]	Mode	Path X	Path Y
000	bypass	$I\_XY(t)$	$Q\_XY(t)$
001	positive upper sideband	$I\_XY(t) \times cos(\omega_{NCO\_XY} \times t) - Q\_XY(t) \times sin(\omega_{NCO\_XY} \times t)$	$I\_XY(t) \times sin(\omega_{NCO\_XY} \times t) + Q\_XY(t) \times cos(\omega_{NCO\_XY} \times t)$
010	positive lower sideband	$I\_XY(t) \times cos(\omega_{NCO\_XY} \times t) + Q\_XY(t) \times sin(\omega_{NCO\_XY} \times t)$	$I\_XY(t) \times sin(\omega_{NCO\_XY} \times t) - Q\_XY(t) \times cos(\omega_{NCO\_XY} \times t)$
011	negative upper sideband	$I\_XY(t) \times cos(\omega_{NCO\_XY} \times t) - Q\_XY(t) \times sin(\omega_{NCO\_XY} \times t)$	$-I\_XY(t) \times sin(\omega_{NCO\_XY} \times t) - Q\_XY(t) \times cos(\omega_{NCO\_XY} \times t)$
100	negative lower sideband	$I\_XY(t) \times cos(\omega_{NCO\_XY} \times t) + Q\_XY(t) \times sin(\omega_{NCO\_XY} \times t)$	$-I\_XY(t) \times sin(\omega_{NCO\_XY} \times t) + Q\_XY(t) \times cos(\omega_{NCO\_XY} \times t)$
others	not defined	-	-

The effect of the MODULATION parameter is better viewed after mixing the X and Y signal with a LO frequency through an IQ modulator.

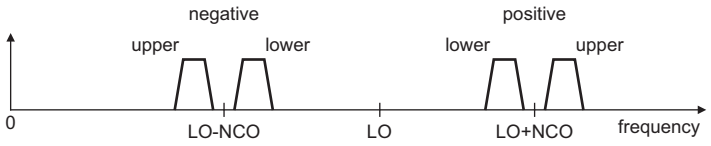


Fig 19. Complex modulation after LO mixing

11.2.3.4 40-bit NCO

The SSBM used the complex signals coming from the NCO (Numeric Complex Oscillator) to mix the I and Q signals. The 5 registers NCO_FREQ_XY_B0 to NCO_FREQ_XY_B4 over 40 bits can set the frequency.

The frequency is calculated with Equation 4:

$$f_{NCO} = \frac{M \times f_s}{2^{40}} \quad (4)$$

Where:

- M is the value set in the bits NCO_FREQ_XY[39:0] of the NCO frequency registers .
- f_s is the final DAC output clock sampling frequency

The registers NCO_PH_OFFSET_XY_LSB and NCO_PH_OFFSET_XY_MSB over 16 bits from 0° to 360° can set the phase of the NCO.

The default settings represent an NCO frequency of 96 MHz when using a DAC clock of 640 Msps. For other DAC clock frequencies, use Equation 4 to define the associated NCO frequency.

11.2.3.5 NCO low power

When using NCO low power (bit NCO_LP_SEL_XY), the five most significant bits of register NCO_FREQ_XY_B4 (bits NCO_FREQ_XY[39:32]; bits [31:0] are masked by zero) can set the frequency.

The frequency is calculated with Equation 5:

$$f_{NCO} = \frac{M \times f_s}{2^{40}} \quad (5)$$

Where:

- M is the value set in the bits NCO_FREQ_XY[39:0] of the NCO frequency registers .
- f_s is the DAC clock sampling frequency

11.2.3.6 Inverse sinx / x

A selectable FIR filter is incorporated to compensate the sinx / x effect caused by the roll-off effect of the DAC. The coefficients are represented in Table 17. This feature is controlled by register INV_SINC_SEL_XY

Table 17. Inversion filter coefficients

Inversion filter		
Lower	**Upper**	**Value**
H(1)	H(9)	+1
H(2)	H(8)	–4
H(3)	H(7)	+13
H(4)	H(6)	–51
H(5)	-	+610

Remark: The transfer function of this features adds some gain to the signals and some saturation can occur with a level of distortion in the output spectrum as result. Update the digital gain accordingly to avoid this saturation.

11.2.3.7 Minus 3dB

During normal operation, a full-scale pattern is also full-scale at the DAC output. When the I data and the Q data approach full-scale simultaneously, saturation can occur. The Minus 3dB function (bit MINUS_3DB_XY of register DAC_OUT_CTRL_XY) can be used to reduce the 3 dB gain in the modulator. It retains a full-scale range at the DAC output without added interferers.

11.2.3.8 Phase correction

The IQ modulator which follows the DACs can have a phase imbalance resulting in undesired sidebands. By adjusting the phase between the I and Q channels, the unwanted sideband can be reduced.

Without compensation the I and Q channels have a phase difference of π / 2 (90°). The registers PH_CORR_XY_CTRL_0 and PH_CORR_XY_CTRL_1 ensure a phase variation from 75.7° to 104.3° by steps 0.0035°. The two registers define a signed value that ranges from –4096 to +4095. The equation: PH_CORR[12:0] / 16384 gives the resulting phase compensation (in radians). The phase correction can be enabled by register PH_CORR_EN_XY .

11.2.3.9 Digital gain

The full-scale output current for each DAC is the sum of the two complementary current outputs:

- $I_{OA(fs)} = I_{IOUTA\_P} + I_{IOUTA\_N}$
- $I_{OB(fs)} = I_{IOUTB\_P} + I_{IOUTB\_N}$
- $I_{OB(fs)} = I_{IOUTC\_P} + I_{IOUTC\_N}$
- $I_{OB(fs)} = I_{IOUTD\_P} + I_{IOUTD\_N}$

The IQ-modulator can have an amplitude imbalance which results in undesired sidebands. The unwanted sideband can be reduced by adjusting the amplitude of signals A and B. The two gains are purely digital and could be enabled by registers DAC_X_DGAIN_EN and DAC_Y_DGAIN_EN .

The output current of DAC X depends on the digital input data and the gain factor defined by bits DAC_X_DGAIN[11:0] of register DAC_X_DGAIN_MSB and register DAC_X_DGAIN_LSB .

$$I_{IOUTA\_P} = I_{OA(fs)} \times \frac{(DAC\_X\_DGAIN)}{4096} \times \left(\frac{DATA}{65535}\right) \quad (6)$$

$$I_{IOUTA\_N} = I_{OA(fs)} \times \left(1 - \frac{(DAC\_X\_DGAIN)}{4096} \times \left(\frac{DATA}{65535}\right)\right) \quad (7)$$

$$I_{IOUTC\_P} = I_{OA(fs)} \times \frac{(DAC\_X\_DGAIN)}{4096} \times \left(\frac{DATA}{65535}\right) \quad (8)$$

$$I_{IOUTC\_N} = I_{OA(fs)} \times \left(1 - \frac{(DAC\_X\_DGAIN)}{4096} \times \left(\frac{DATA}{65535}\right)\right) \quad (9)$$

The output current of DAC B depends on the digital input data and the gain factor defined by bits DAC_Y_DGAIN[11:0] of register DAC_Y_DGAIN_MSB and DAC_Y_DGAIN_LSB .

$$I_{IOUTB\_P} = I_{OB(fs)} \times \frac{(DAC\_Y\_DGAIN)}{4096} \times \left(\frac{DATA}{65535}\right) \quad (10)$$

$$I_{IOUTB\_N} = I_{OB(fs)} \times \left(1 - \frac{(DAC\_Y\_DGAIN)}{4096} \times \left(\frac{DATA}{65535}\right)\right) \quad (11)$$

$$I_{IOUTD\_P} = I_{OB(fs)} \times \frac{(DAC\_Y\_DGAIN)}{4096} \times \left(\frac{DATA}{65535}\right) \quad (12)$$

$$I_{IOUTD\_N} = I_{OB(fs)} \times \left(1 - \frac{(DAC\_Y\_DGAIN)}{4096} \times \left(\frac{DATA}{65535}\right)\right) \quad (13)$$

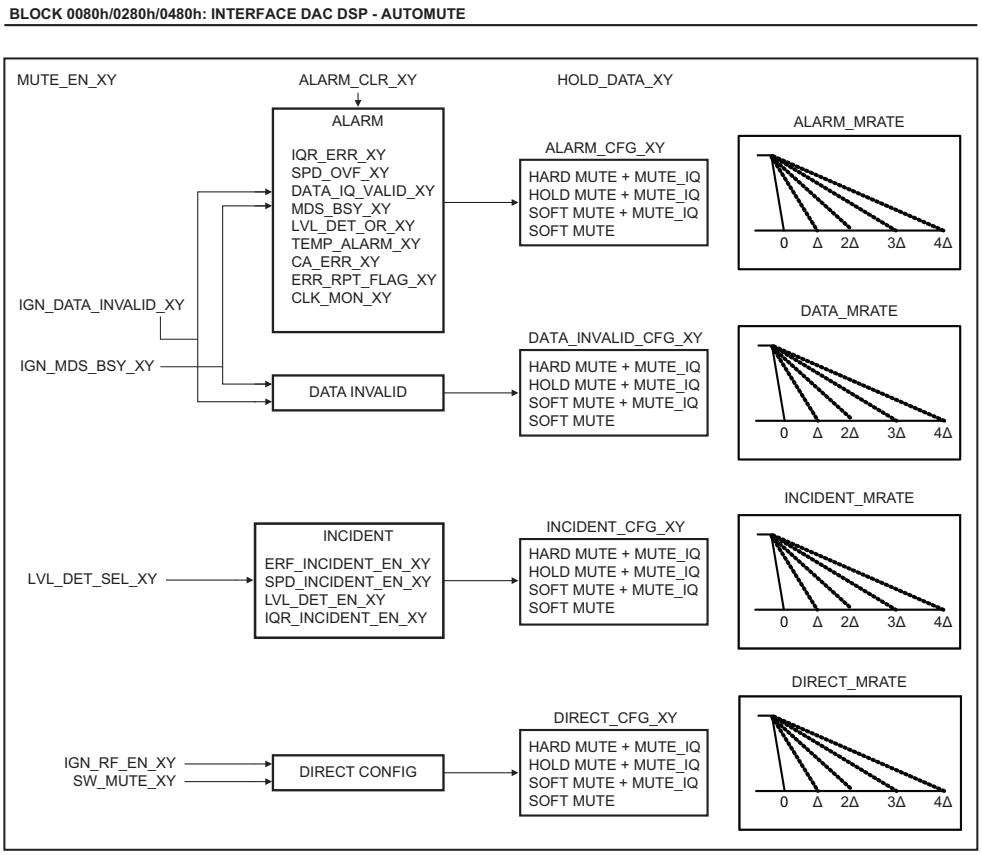
Table 18 shows the output current as a function of the input data, when $I_{OA(fs)} = I_{OB(fs)} = 20$ mA.

Table 18. DAC transfer function

Data	I15 to I0/Q15 to Q0 (binary coding)	I15 to I0/Q15 to Q0 (two's complement coding	IOUTA_P/ IOUTB_P	IOUTA_N/ IOUTB_N
0	0000 0000 0000 0000	1000 0000 0000 0000	0 mA	20 mA
...	...	...	...	....
32768	1000 0000 0000 0000	0000 0000 0000 0000	10 mA	10 mA
...	...	...	...	...
65535	1111 1111 1111 1111	0111 1111 1111 1111	20 mA	0 mA

11.2.3.10 Auto-mute

The DAC165xQ provides a new auto-mute feature allowing muting the DAC analog output if a conditional event occurs. The auto-mute feature is based on a state machine as described in Figure 21 and on the control of the digital gains.



Block 0080h = DAC A/B
Block 0280h = DAC C/D
Block 0480h = All DACs

Fig 20. Automute overview

In normal operating mode, the state machine is in IDLE state. The digital gains are specified by the user.

Various mute events can be detected in the DAC. These trigger the MUTE state. Once the MUTE state is entered, the DAC automatically sets the digital gains to zero using several mute actions. The mute actions SOFT mute and HOLD mute drop to zero gradually. The mute action HARD mute drop to zero instantly (see Figure 22).

When the digital gains have been set to zero, the state machine enters the WAIT state. In this state, the gains are kept at zero. The state machine stays in this mode until the end of the wait period and the mute event is not deasserted.

When the mute event is cleared and the wait period elapsed, the state machine enters the DEMUTE state. In this state, the digital gains are set again to the initial values. This is done relatively to the mute rate setting. If during this state, a new mute event is triggered, the state machine enters the MUTE state again. The gain decreases from the current gains values, not from the initial ones.

When the digital gains reach the initial values, the state machine enters the IDLE state again.

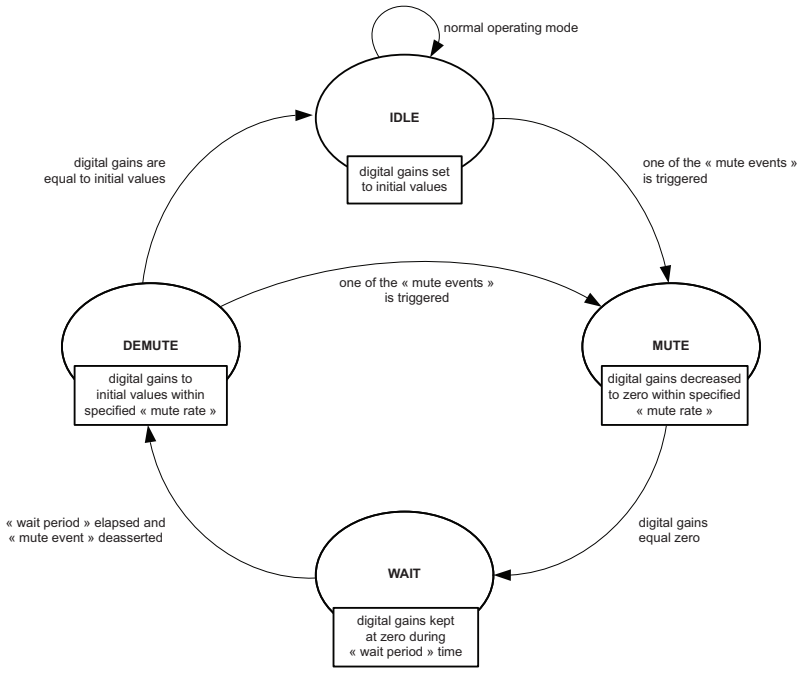


Fig 21. Auto-mute state machine

The mute feature is set by enabling bit MUTE_EN_XY in register MUTE_CTRL_0_XY .

Mute events

The MUTE action is triggered by one of the following mute events. Each of them is linked to either an error detection, a status change or signal power monitoring:

- SPI_SW_MUTE_XY:

  Software event that can be requested by the host interface through the SPI bus.
- RF_EN_XY:

  Hardware event that can be requested by the host interface through pins SR_TG_AB and SR_TG_CD.
- CLK_MON_XY:

  Event linked to the monitoring of the clocks in the receiver physical layer control block.
- MON_DCLK_ERR_XY:

  Event triggered when a clock error occurs in the CDI .
- CA_ERR_XY:

  Event triggered when a clock error occurs in the DLP .
- TEMP_ALARM_XY:

  Event triggered when the temperature sensor measures a temperature that exceeds the threshold value. TEMP_SEL_MAN_XY must be specified first.
- ERR_RPT_FLAG_XY:

  Event triggered when DATA_INVALID is detected by the DLP .
- LVL_DET_OR_XY:

Event triggered when the signal levels exceed the LVL_DET_XY on channel X or Y. LVL_DET_EN_XY and LVL_DET_XY must be set first .

- MDS_BSY_XY:

  Event triggered while the MDS process is busy aligning the DAC .

- DATA_IQ_VALID_XY:

  Event is triggered when DATA_INVALID is detected by the DLP

- SPD_OVF_XY:

  Event triggered when the Signal Power Detector (SPD) average value is exceeding the threshold value .

- IQR_ERR_XY:

  Event triggered when the IQ signal is out of range .

The monitoring of these events can also be done using the interrupt process available in the DAC165xQ . Once the interrupt is detected, the host controller (e.g. an FPGA) can read back the events flags in registers INTR_FLAGS_0_XY and INTR_FLAGS_1_XY and determine the actions to be taken.

Ignore events option

Set bits IGN_RT_EN_XY, IGN_MDS_BSY_XY, and IGN_DATA_V_IQ_XY of the mute control register for the mute controller to ignore certain events.

Mute event categories

The MUTE state is entered when one of the mute events is asserted. Four categories of mute events can be distinguished: ALARM, DATA, INCIDENT, and DIRECT .

Table 19. Mute event categories

Mute event	ALARM[1]		DATA		INCIDENT		DIRECT	
	Enable	Disable	Enable	Disable	Enable	Disable	Enable	Disable
SPI_SW_MUTE_XY							default[2]	
RF_EN_XY							default	IGN_RF_EN_XY
CLK_MON_XY	ALARM_EN_XY[0][3]							
MON_DCLK_ERR_XY	ALARM_EN_XY [1][3]							
CA_ERR_XY	ALARM_EN_XY [2][3]							
TEMP_ALARM_XY	ALARM_EN_XY [3][3]							
ERR_RPT_FLAG	ALARM_EN_XY [4][3]		default		ERF_INCIDENT_EN_XY			
LVL_DET_OR_XY	ALARM_EN_XY [5][3]							
MDS_BSY_XY	ALARM_EN_XY [6][3]	IGN_MDS_BSY_XY	default	IGN_MDS_BSY_XY				
DATA_IQ_VALID	ALARM_EN_XY [7][3]	IGN_DATA_V_IQ_XY	default	IGN_DATA_V_IQ_XY				
SPD_OVF_XY	ALARM_EN_XY [8][3]				SPD_INCIDENT_EN_XY			
IQR_ERR_XY	ALARM_EN_XY [9][3]				IQR_INCIDENT_EN_XY			

[1] All ALARM mute events can be disabled using bit IGN_ALARM_XY. However, their detection can still be monitored using the INTERRUPT module.

[2] This bit is not auto-clear.

[3] The ALARM mute events must be cleared with bit ALARM_CLR_XY to move from the WAIT state to the DEMUTE state.

Priority between categories

The priority in which the auto-mute module evaluates its inputs is:

- Priority 1: DIRECT
- Priority 2: ALARM
- Priority 3: DATA
- Priority 4: INCIDENT

Mute actions

Four mute actions can be selected for each of the four previous mute event categories.

The digital data can also be reset to its default value (bits I_DC_LVL_XY and Q_DC_LVL_XY) to avoid disturbances in the FIR filters.

Register MUTE_CTRL_1_XY :

- Hard_mute + mute IQ:

  The digital gains of the DACs are set to zero (within 1 DAC clock period). The digital path is filled with the default I and Q levels.
- Hold_mute + mute IQ:

  The outputs of the DACs are kept to the current value (within 1 DAC clock period). The digital path is filled with the default I and Q levels.

  Remark: Bit HOLD_DATA_XY must be enabled for this action. If this bit is not set, the overall Hold_mute + mute IQ actions are not taken into account.
- Soft_mute + mute IQ:

  The digital gains of the DACs are swept down to zero at the MUTE_RATE_CTRL_0_XY value . The digital path is filled with the default I and Q levels.
- Soft_mute:

  The outputs of the DACs are swept down to zero at the MUTE_RATE_CTRL_0_XY value . The digital path is kept with the received values.

  Remark: As the DC offsets are applied after the digital gain, the outputs are still impacted by their values, even if a mute action event occurs.

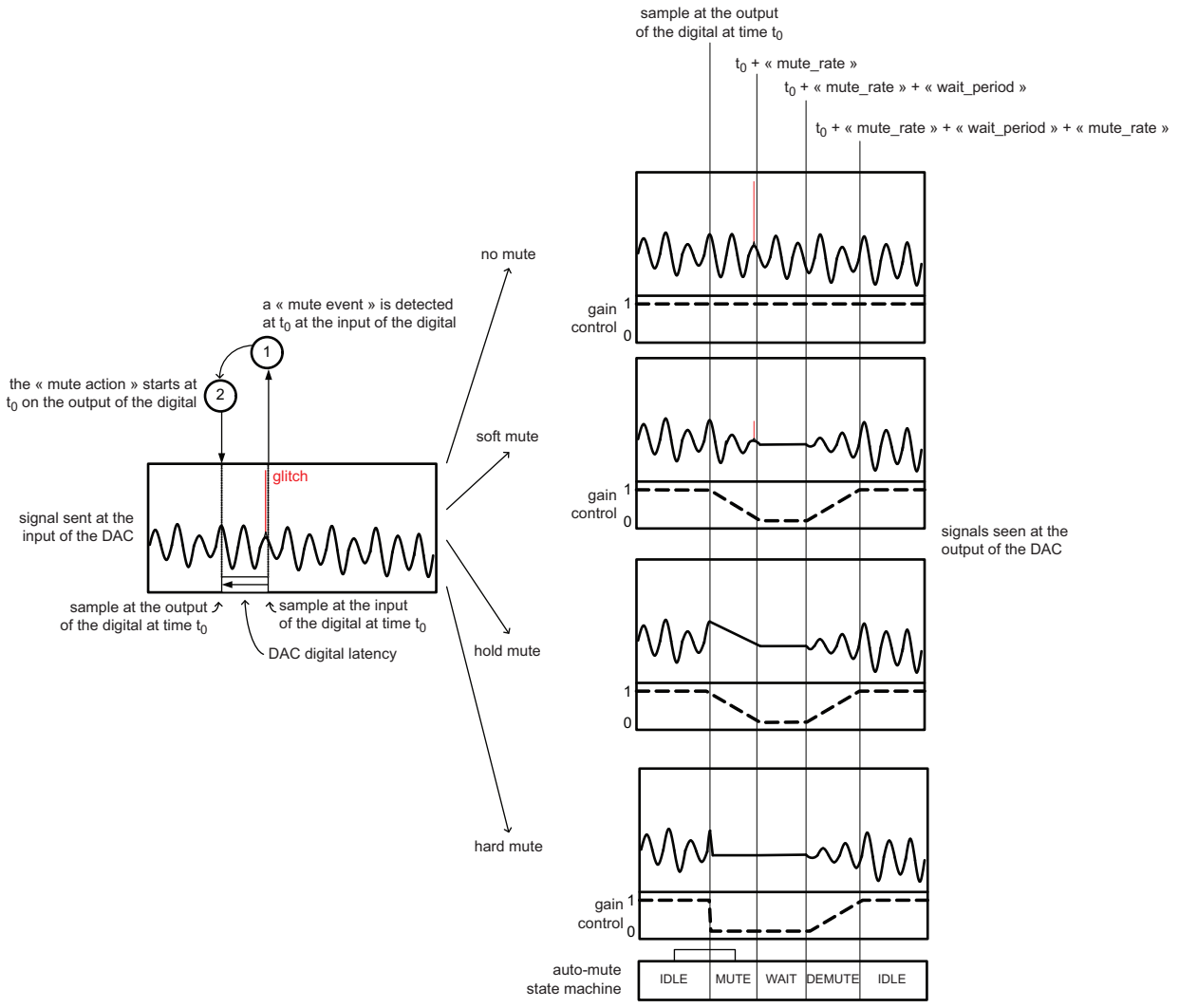


Fig 22. Mute actions representation

Mute rate

The time period used to decrease or increase the gains during a MUTE or DEMUTE state is called mute rate. Each mute action category has its own mute rate available through the registers ALARM_MRATE_XY, DATA_MRATE_XY, INCIDENT_MRATE_XY and DIRECT_MRATE_XY.

Table 20. Mute rate availability

Through ALARM_MRATE_XY, DATA_MRATE_XY, INCIDENT_MRATE_XY, and DIRECT_MRATE_XY.

DAC clock	750 MHz	1 GHz	1.5 GHz
Period ×8 (ns)	10.67	8.00	5.33
Value	Mute rate (ns)	Mute rate (ns)	Mute rate (ns)
0000	10.67	8.00	5.33
0001	21.34	16.00	10.66
0010	42.68	32.00	21.32
0011	85.36	64.00	42.64
0100	170.72	128.00	85.28
0101	341.44	256.00	170.56
0110	682.88	512.00	341.12
0111	1,365.76	1,024.00	682.24
1000	2,731.52	2,048.00	1,364.48
1001	3,642.47	2,731.00	1,819.53
1010	5,463.04	4 096.00	2,728.96
1011	7,283.61	5,461.00	3,638.39
1100	10,926.08	8,192.00	5,457.92
1101	14,557.88	10,915.00	7,272.12
1110	21,852.16	16,384.00	10,915.84
1111	43,704.32	32,768.00	21,831.68

Mute wait period

The wait period time can be calculated with Equation 14:

$$wait\ period = (MUTE\_WAIT\_PERIOD + 1) \times 8 \times DAC\_CLK\_PERIOD \quad (14)$$

At 1 Gsps, this gives a wait period between 8 ns and 527 μs.

DEMUTE triggering

When the mute action is either a DIRECT, an INCIDENT or a DATA mute action, the WAIT state is enabled as long as the wait period is not elapsed and the event is not released.

When the mute action is an ALARM mute action, the WAIT state is enabled as long as the alarm controller is not reset using bit MC_ALARM_CLR_XY .

11.2.3.11 Digital offset adjustment

When the DAC165xQ analog output is DC connected to the next stage, the digital offset correction (bits DAC_X_OFFSET[15:0] and DAC_Y_OFFSET[15:0]) can be used to adjust the common-mode level at the output of each DAC. Table 21 shows the variation range of the digital offset.

Table 21. Digital offset adjustment

DAC_X_OFFSET[15:0] DAC_Y_OFFSET[15:0] (two's complement)	Offset applied
1000 0000 0000 0000	−32768
1000 0000 0000 0001	−32767
...	...
1111 1111 1111 1111	−1
0000 0000 0000 0000	0
0000 0000 0000 0001	+1
...	...
0111 1111 1111 1110	+32766
0111 1111 1111 1111	+32767

11.2.4 Signal detectors

11.2.4.1 Level detector

A level detector feature is available at the end of the digital path. It can be enabled using bit LVL_DET_EN_XY . This feature specifies a signal output range limited (or clipped) to −128 × LVL_DET to +128 × LVL_DET around the half Full-Scale (FS) . If the signal value enters the upper or lower clipping area, it is clipped to +128 × LVL_DET or −128 × LVL_DET, respectively). Figure 23 shows this behavior.

Use this feature in combination with the auto-mute feature to avoid unexpected spectral spurs after the clipping of the signal .

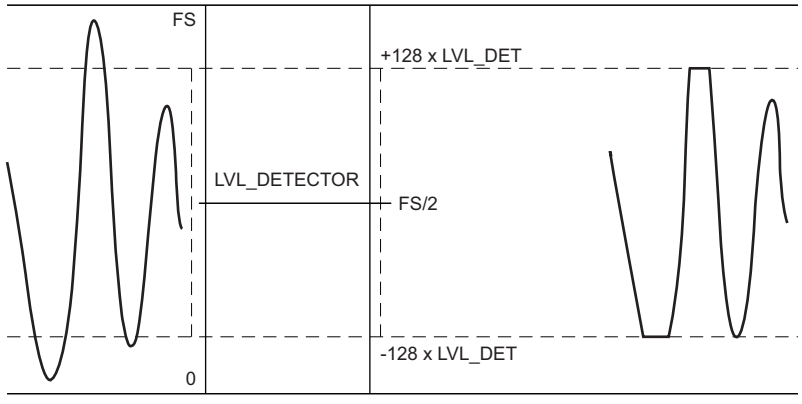


Fig 23. Level detector operation

Table 22. Level detector values

LVL_DET[7:0]	Peak excursion from full-scale / 2	Code output range (binary offset)	dBFS value 10log(peak excursion x 2 / 65536)
00h	0	32768	NaN
...		...	...
19h	3200	32568 to 35968	−10.1 dBFS
...		...	...
80h	16384	16384 to 49152	−3 dBFS
...		...	...
CBh	25984	6784 to 58752	-1 dBFS
...		...	...
FFh	32768	0 to 65536	0 dBFS

11.2.4.2 Signal Power Detector (SPD)

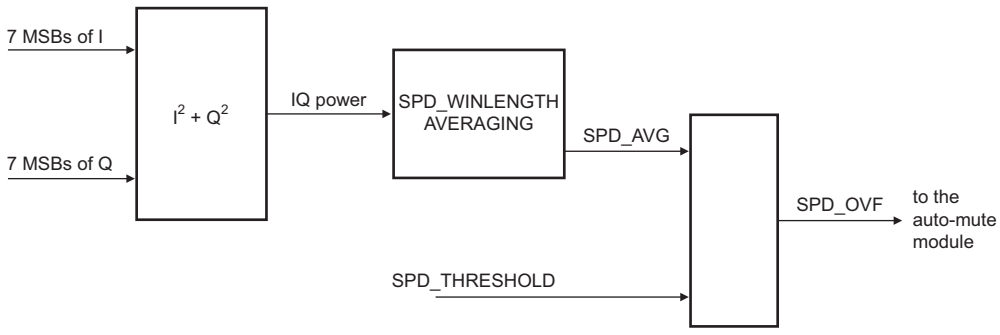


Fig 24. Signal power detector

The Signal Power Detector (SPD) takes the 7 MSBs of the I and Q signal to determine the IQ power of an IQ-pair. Averaging is done over the programmable number (2^6, 2^7 to 2^{21}) of IQ-pairs using the SPD_WIN_LENGTH register . If the SPD_AVG bit exceeds the 16-bits threshold value, the SPD overflow (SPD_OVF) flag becomes active and can invoke a mute action depending on the mute control settings.

The SPD can have a large response time because of the samples average based algorithm. This must be taken into account at system level.

11.2.4.3 IQ Range (IQR)

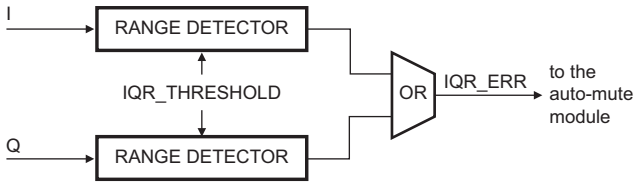


Fig 25. IQ range

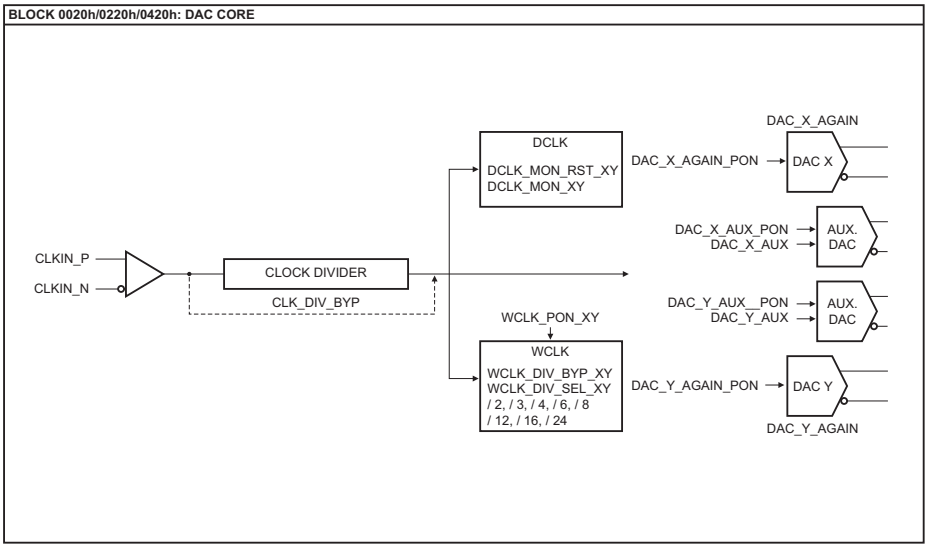
The IQ range detector checks if the I and Q signal values are within the range specified by register IQR_THRESHOLD compared to the center value (= 0 if the data are in 2 complement's representation or 32768 if the data are in binary offset representation):

–IQR_THRESHOLD < I – center value < +IQR_THRESHOLD

–IQR_THRESHOLD < Q – center value < +IQR_THRESHOLD

11.2.5 Analog core of the dual DAC

This section refers to the analog configuration required to set up the dual DAC core. The clock and output stages are described as well as the internal registers (Block 0020h; see Figure 26) used to configure the clock tree inside the chip.



Block 0020h = DAC A/B

Block 0220h = DAC C/D

Block 0420h = All DACs

Fig 26. DAC core overview

11.2.5.1 Clocks

The DAC165xQ requires one single differential clock (CLKIN_P, CLKIN_N) for the whole device (including the digital data path, the quad DAC core and the JESD204B interface).

During the reset phase (RESET_N asserted), the input clock must be stable and running, ensuring a proper reset of the complete device.

Clock input external configuration

The DAC165xQ incorporates one differential clock input, CLKIN_N/CLKIN_P, with embedded 100 Ω differential resistor. The clock input can be LVDS but it can also be interfaced with CML.

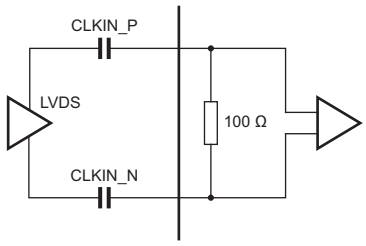


Fig 27. LVDS clock configuration

On-board Phase-Locked Loop (PLL)

The DAC165xQ has a single differential clock input to directly feed the digital and analog clock tree of the device. When using the embedded PLL, a reference clock has to be provided at this input. The mixed-signal PLL synthesizes the correct internal clocks with very low jitter. The predivider (N) and post-divider (M) can be programmed to divider ratio ranges from 1 to 16. The reference clock to the PLL should be 61.44 MHz for optimal PLL performance. The DAC clock frequency can be calculated with Equation 15:

$$f_{DAC} = \frac{FCW}{M \times N} \times f \quad (15)$$

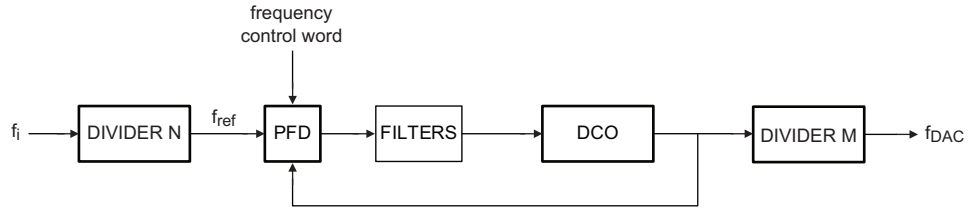


Fig 28. PLL block diagram

Figure 28 shows a conceptual view of the PLL. Digital control words that control the oscillator frequency determine the output frequency of the PLL.

Table 23. Examples

f_i (MHz)	N	f_{ref} (MHz)	FCW	DCO (MHz)	M	F_{DAC} (MHz)
122.88	2	61.44	72	4423.68	3	1474.56
122.88	2	61.44	80	4915.20	5	983.04

Clock frequency input range

The DAC165xQ can only operate in two modes:

- Direct clocking mode:

  The input clock frequency is limited to 1500 MHz
- Divided clocking mode:

  The input clock is internally divided by 2. The maximum input frequency is 3 GHz. This mode allows the programming of the group delay feature.

Clocks internal configuration

The following registers must be specified to configure the DAC165xQ in Direct clocking mode :

- <tbd>

The final clock is referred to as the "DAC clock". This is the clock that is going directly to the quad DAC core and is running at maximum speed. From this DAC clock two digital clocks are derived: DCLK and WCLK.

DCLK is the digital clock used for all logic related to the Digital Signal Processing (DSP) of the DAC. DCLK is automatically generated from the registers PON_DAC_CORE_CFG_XY_0, INTERPOLATION_XY and CDI_MOD. Registers DCLK_MON and DCLK_MON_RST can be used to monitor this automatic generation. This flag can also raise the interrupt feature .

WCLK is the digital clock used for all logic related to the Digital Lane Processing (DLP) of the input interface. This clock must be enabled by bit WCLK_PON_XY . The divider ratio WCLK_DIV_SEL_XY must be specified using the following equation:

$$\frac{WCLK}{DAC\ clock} = \frac{M}{(L \times INTERPOLATION\_XY)} \quad (16)$$

Where:

- M stands for the number of DACs used inside the DAC165xQ (M = 1 or M = 2)
- L stands for the number of serial input lanes used (L = 1, L = 2, or L = 4)
- INTERPOLATION_XY stands for the interpolation factor specified in register TX_CFG_XY .

Table 24 shows the results for nominal use cases (not exhaustive)

Table 24. WCLK_DIV selection

LMF configuration	Interpolation ratio	WCLK/DAC clock	WCLK_DIV_BYP	WCLK_DIV_SEL
421 / 422	2	1/4	0	010
	4	1/8	0	100
	8	1/16	0	110
222	2	1/2	0	000
	4	1/4	0	010
	8	1/8	0	100
124	2	1	1	xxx
	4	1/2	0	000
	8	1/4	0	010
211	2	1/2	0	000
	4	1/4	0	010
	8	1/8	0	100

Clock Domain Interface (CDI)

A CDI logic handles the error-free data transition from the WCLK clock domain to the DCLK domain. It consists of 12 buffers that absorb the phase variation between the two clocks. The reliability of the data transmission depends on the clock-frequency ratios and therefore on the interpolation mode. The CDI must be set in the same mode as the interpolation ratio to be properly configured. This mode is configured with register CDI_CTRL .

Table 25. Interpolation and CDI modes

Interpolation	CDI mode	Maximum input data rate (Msps)
~1	Mode 0 (^2)	750
×2	Mode 0 (^2)	750
×4	Mode 1 (^4)	375
×8	Mode 2 (^8)	187.5

Ideally, buffer number 11 is selected as the reference. If jitter of ±1 clock cycle is injected between the clocks occurs, the pointer can oscillate between buffers 10 and 0. If more jitter is injected, the range increases to buffers 9 and 1, etc.

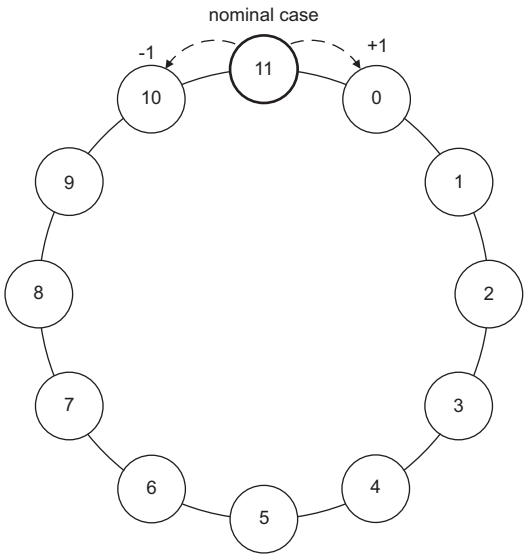


Fig 29. Concept view of the CDI monitoring

This buffer position can be monitored using register MON_DCLK .

The variation of the buffer location could also raise an interrupt (see interrupt section).

11.3 Analog quad DAC core

The DAC165xQ core consists of two DACs. Each of them can be independently set to Power-down mode or Sleep mode if using the DAC in single channel mode is preferred (DAC_X_AGAIN_PON).

11.3.1 Regulation

The DAC165xQ reference circuitry integrates an internal band gap reference voltage which delivers a 0.7 V reference on the GAPOUT pin. Decouple pin GAPOUT using a 100 nF capacitor.

The reference current is generated via an external resistor of 560 Ω (1 %) connected to VIRES.

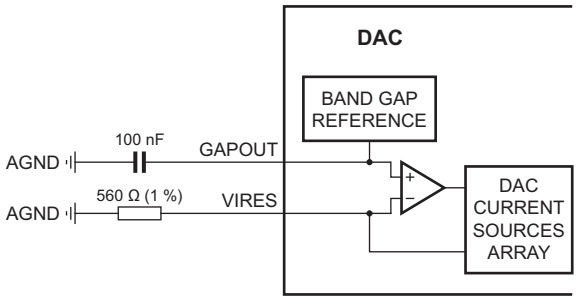


Fig 30. Internal reference configuration

Figure 30 shows the optimal configuration for temperature drift compensation because the band gap reference voltage can be matched to the voltage across the feedback resistor.

The DAC current can also be adjusted by applying an external reference voltage to the non-inverting input pin GAPOUT and disabling the internal band gap reference voltage (bit BGAP_PON_XY).

11.3.2 Full-scale current adjustment

The default full-scale current ($I_{O(fs)}$) is 20 mA. However, further adjustments, ranging from 8.1 mA to 34 mA, can be made to both DACs independently using the serial interface.

The settings applied to DAC_X_GAIN[9:0] define the full-scale current of DAC X:

$$I_{O(fs)}\ \mu A = 8100 + DAC\_X\_GAIN[9{:}0] \times 25{,}3 \quad (17)$$

The DAC_Y_GAIN[9:0] define the full-scale current of DAC Y:

$$I_{O(fs)}\ \mu A = 8100 + DAC\_Y\_GAIN[9{:}0] \times 25{,}3 \quad (18)$$

11.4 Analog output

11.4.1 DAC1658Q: High common-mode output voltage

The device has four output channels, each producing two complementary current outputs, which enable the reduction of even-order harmonics and noise. The pins are IOUTA_P/IOUTA_N, IOUTB_P/IOUTB_N, IOUTC_P/IOUTC_N and IOUTD_P/IOUTD_N. Connect these pins to ground (GND) using a load resistor RL to the 3.3 V analog power supply ($V_{DDA(3V3)}$).

Figure 31 shows the equivalent analog output circuit of one DAC. This circuit includes a parallel combination of NMOS current sources and associated switches for each segment.

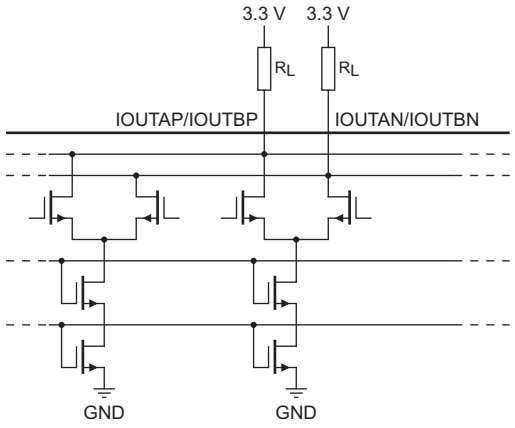


Fig 31. Equivalent analog output circuit

The cascode source configuration increases the output impedance of the source, which improves the dynamic performance of the DAC because there is less distortion.

Depending on the application, the various stages and the targeted performances, the device can be used for an output level of up to 2 V (p-p).

11.4.2 DAC1653Q: Low common-mode output voltage

The device has four output channels, each producing two complementary current outputs, which enable the reduction of even-order harmonics and noise. The pins are IOUTA_P/IOUTA_N and IOUTB_P/IOUTB_N, IOUTC_P/IOUTC_N and IOUTD_P/IOUTD_N. Connect these pins using a load resistor R_L to the analog ground (GND).

Figure 32 shows the equivalent analog output circuit of one DAC. This circuit includes a parallel combination of PMOS current sources and associated switches for each segment.

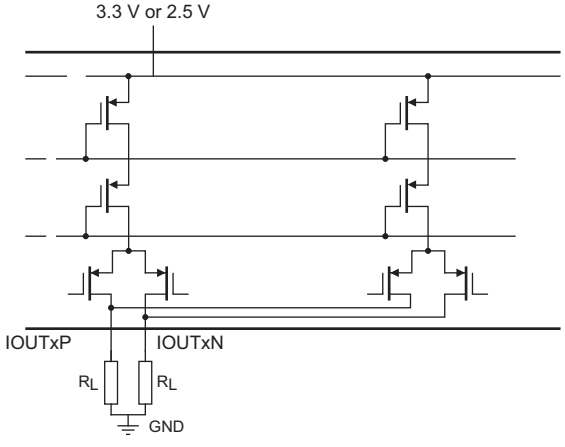


Fig 32. Equivalent analog output circuit

11.5 Temperature sensor

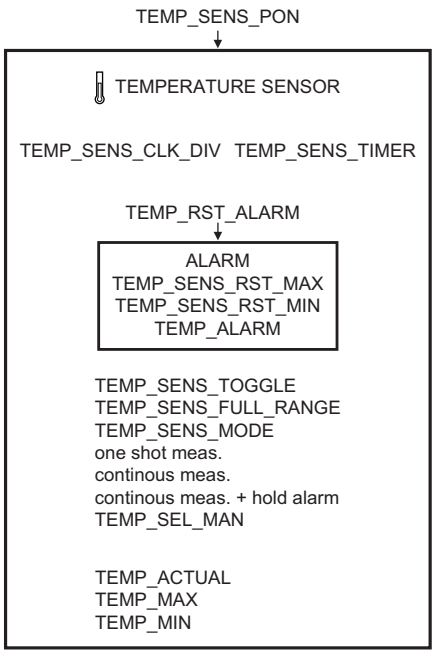


Fig 33. Temperature sensor

The DAC165xQ embeds a temperature sensor to monitor the temperature inside the chip. This module is based on a 6-bit resolution ADC clocked at DAC_CLK / (8 × TS_CLKDIV). The mode of measurements is configurable as a one shot measurement, continuous measurements or continuous measurements with alarm flag held in case of temperature exceeding a preset threshold. In continuous mode, the measurement is done every TS_TIMER cycles. The TEMPS_LVL specifies the threshold level that is compared with the measured value. If the measured value exceeds the threshold, the TEMP_ALARM flag is set and triggers a mute action . The maximum and minimum temperatures measured are stored in registers TEMP_MAXand TEMP_MIN . The current temperature is stored in register TEMP_ACTUAL . Once the TEMP_ALARM flag is set, it must be reset using the TEMP_SENS_RST_ALARM bit of the temperature sensor control register. The maximum and minimum temperature can also be reset using bits TEMP_SENS_RST_MAX and TEMP_SENS_RST_MIN of the temperature sensor control register .

The value stored in the maximum, current, and minimum registers represents the output value of the ADC. This value must be matched to the real temperature.

$$T\ (°C) = \alpha \times ADC\_value \tag{19}$$

Where:

- α = <tbd>

11.6 Multiple Devices Synchronization (MDS); JESD204B subclass I

The MDS feature enables multiple DAC channels to be sampled synchronously and phase coherently to within one DAC clock period. This feature is part of the JESD204B standard but the implementation adds some unique features that simplify the PCB design.

11.6.1 Non-deterministic latency of a system

In a system using multiple DAC devices, there are numerous sources of timing uncertainties. Figure 34 gives an overview of these uncertainties.

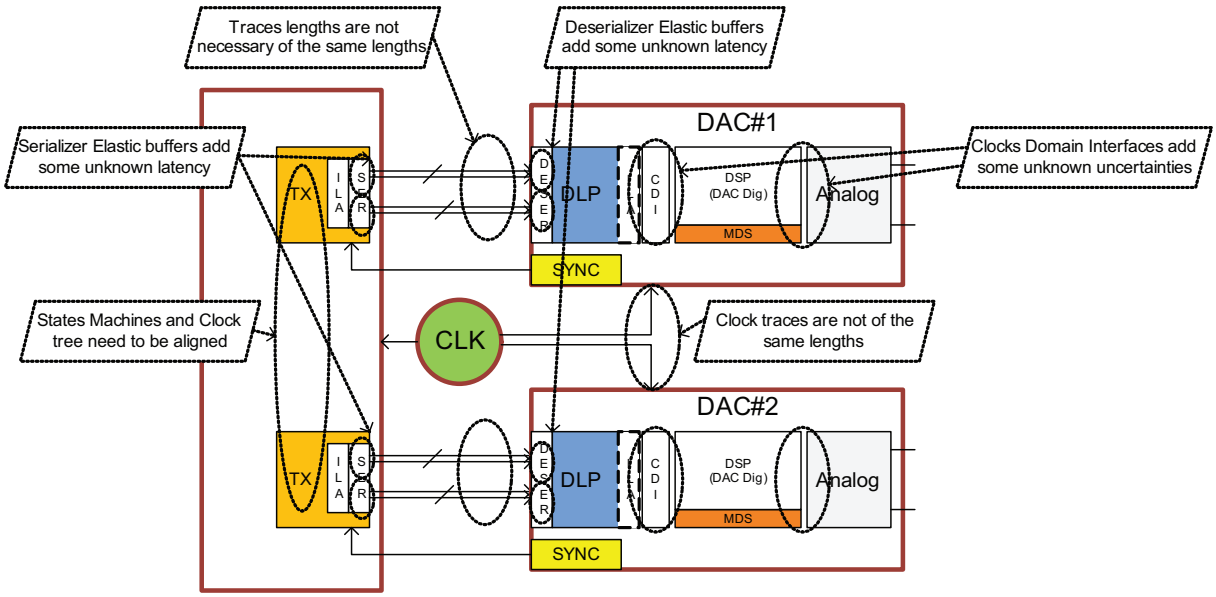


Fig 34. Timing uncertainties when using multiple DAC devices

The sources of uncertainties are shared between the Transmitter device (TX), the Receiver devices (RX), the PCB layout and the architectures of the JESD204B system clocks. A single device can detect timing drift and uncertainties, but not at system level. Therefore a synchronization process is required to enable the sytem to output the analog signals of all the RX devices in a coherent way. Moreover, the system becomes predictable if from one start-up to another one, the overall latency is deterministic.

The MDS feature of the DAC165xQ has been implemented in compliance with the JESD204B subclass 1 specification to fulfill these requirements.

11.6.2 JESD204B system clocks

There are various system 'clocks' that are used in the JESD204B specification. However, only one of them is seen at system level, the device clock, which is provided to the device. The other clocks are related to the JESD204B standard and are used to assemble/deassemble the data in octets and then in 10B words (see JESD204B standard). Figure 35 and Table 26 show the relationship between them.

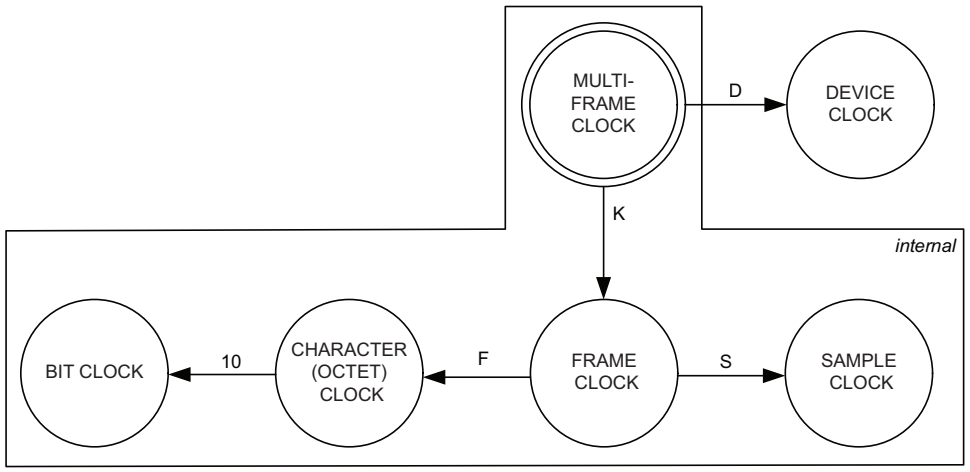


Fig 35. JESD204B system clocks

Table 26. Relationship between various clocks

Clock name	Ratio with respect to multi-frame clock	Comments regarding JESD204B specification
multi-frame clock	1	-
frame clock	× K	Ceil(17 / F) ≤ K ≤ min(32, floor(1024 / F))
character clock	× F × K	F = 1 to 256
bit clock	× 10 × F × K	8b/10b encoding
sample clock	× S × K	S = 1 to 32
device clock	× D	D is integer

From a system point of view, the TX and RX must share the same values for the internal clocks but not necessarily the same device clocks. Figure 36 and Figure 37 show the clocking scheme for an FPGA and a DAC working in an LMF-S = 421-1 configuration.

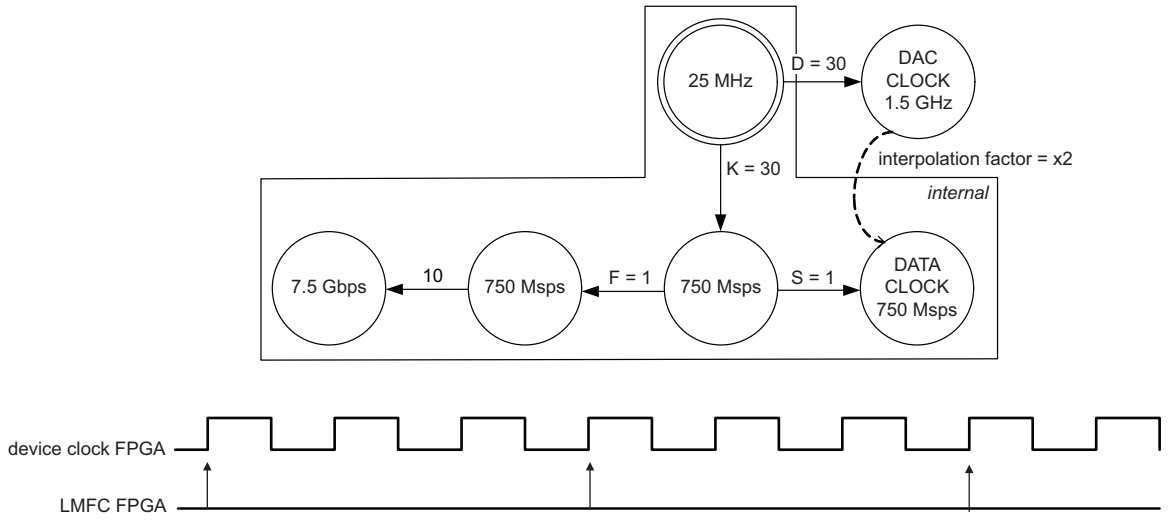


Fig 36. Clocking scheme FPGA

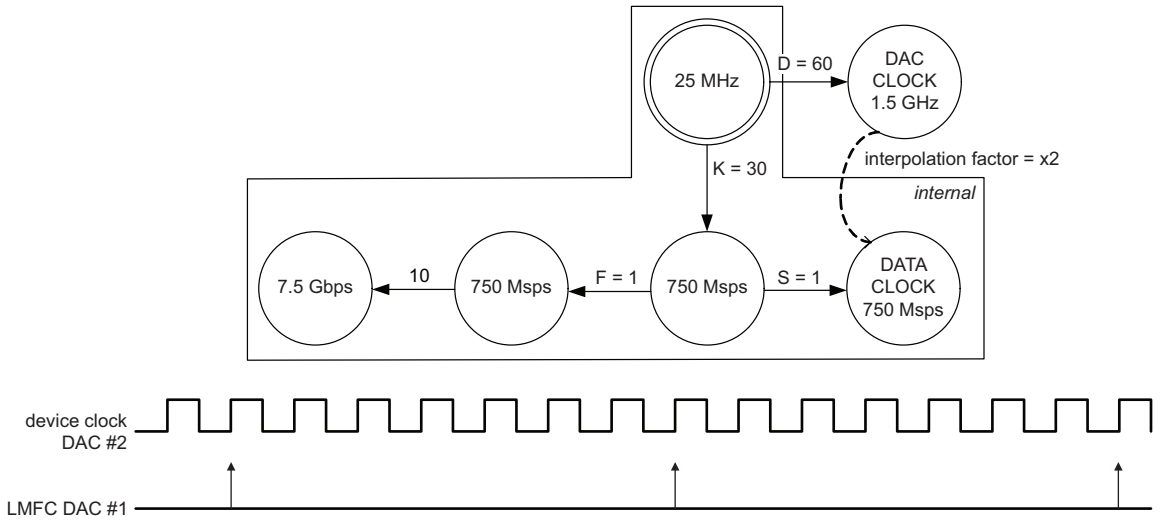


Fig 37. Clocking scheme DAC

As all clocks can be derived from the Multi-Frame Clock (MFC), this clock becomes the reference for a JESD204B system. Each device used in the system has its own local version of the MFC. These local version are called Local Multi-Frame Clock (LMFC). Due to the timing uncertainties the phase relationships between all the device LMFCs are unknown. The goal of MDS is to be able to realign all LMFCs in a fixed and accurate way.

11.6.3 SYSREF clock

To align all the LMFCs within the system, a new clock named SYSREF (SYStem REFerence) is used. This clock is linked to the multi-frame clock by a ratio R. It is a low frequency signal. However, the edges of the signal must be sharp enough as it is sampled by the device clock.

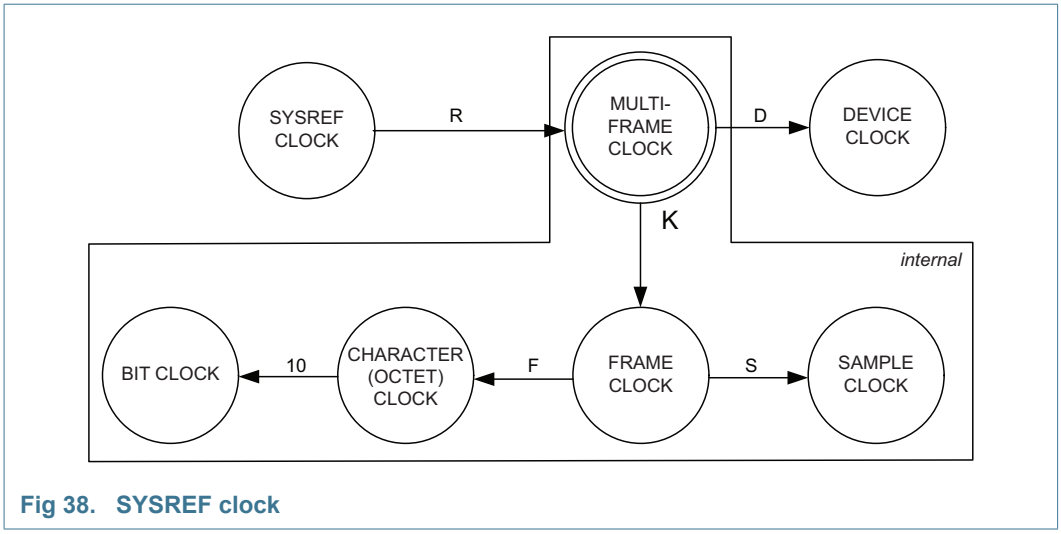


Fig 38. SYSREF clock

The SYSREF signals must be propagated to all the devices of the system. They are used to release the LMFC, so they are all aligned over the devices. The SYSREF signal is sampled by the device clocks. To ensure that all phases of the signals are aligned at the source, the SYSREF signals and the device clocks must be generated from the same clock IC.

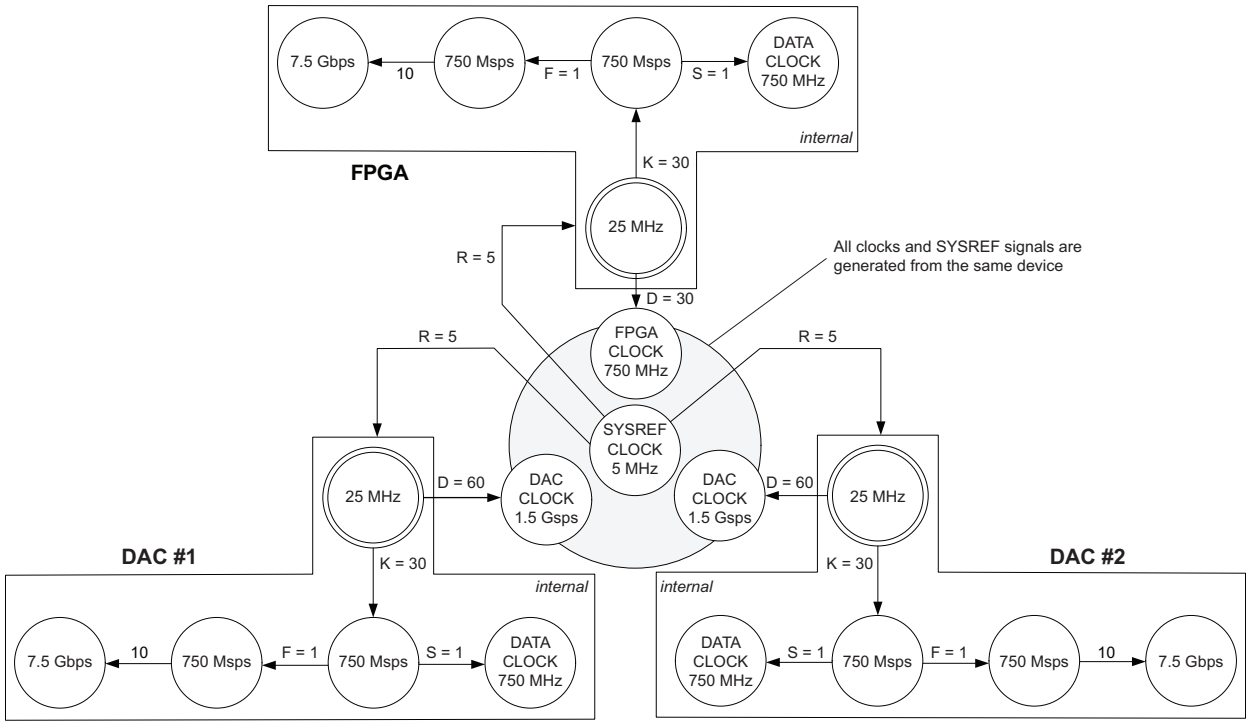


Fig 39. System

All the JESD204B devices sample the SYSREF signal with their own device clocks. The edge detection of the SYSREF signal is used as a system timing reference and the device phase-align their LMFCs to the closest edge of the SYSREF. To ensure an accurate alignment within all devices, the SYSREF signal must show the same phase at the input port of all the devices to synchronize. Therefore, the trace lengths of the SYSREF signals must be equal for all the DAC devices. As the SYSREF signal is sampled by the device clock, the minimum setup ($t_{su(min)}$) and hold ($t_{h(min)}$) time are specified with respect to the Device Clock timing (see Figure 40).

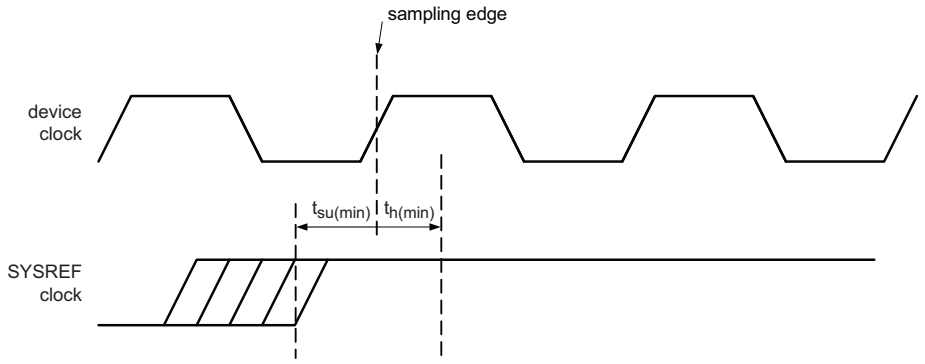


Fig 40. Timing constraints for the SYSREF signal

Figure 41 shows the LMFCs before and after alignment to the SYSREF clock.

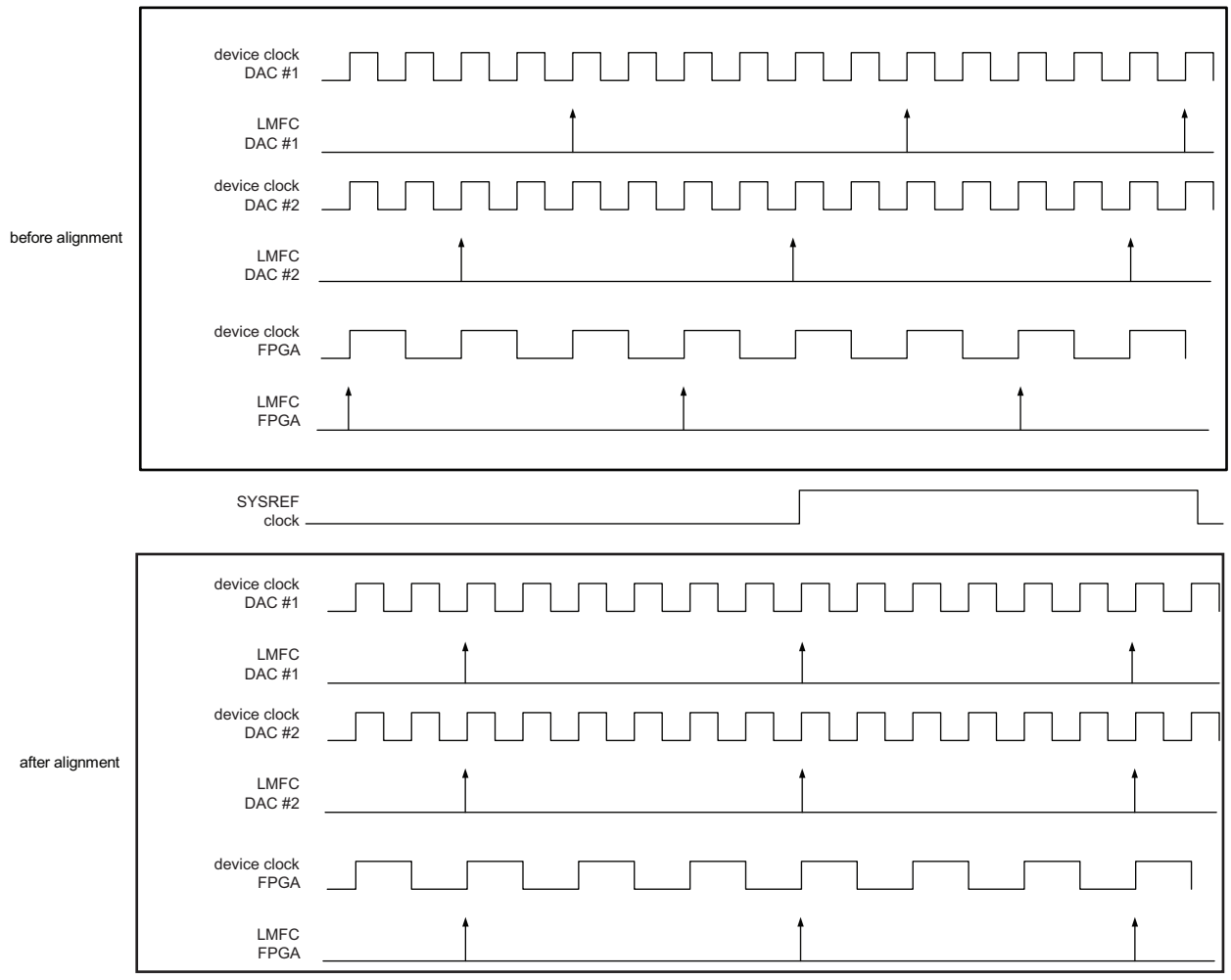


Fig 41. LMFCs before and after alignment to the SYSREF clock

11.6.4 MDS implementation

The DAC165xQ MDS implementation is based on two modules as described in Figure 42:

- **M1**:

  This module contains the SYSREF detector that is sampled at the DAC clock and the control loop used to create a $LMFC_{MDS}$ signal. The control loop is clocked with the digital clock. The digital clock equals DAC clock / 8.

  Remark: The DAC clock and the device clock can differ when using the clock divider. In this section DAC clock is referring to the final clock used to sample the DAC cores.

- **M2**:

  This module compares the phase of the $LMFC_{RCV}$ received from the JESD204B digital lane processing to the phase of the $LMFC_{MDS}$ and shifts the position of the buffer to align the data path to the $LMFC_{MDS}$.

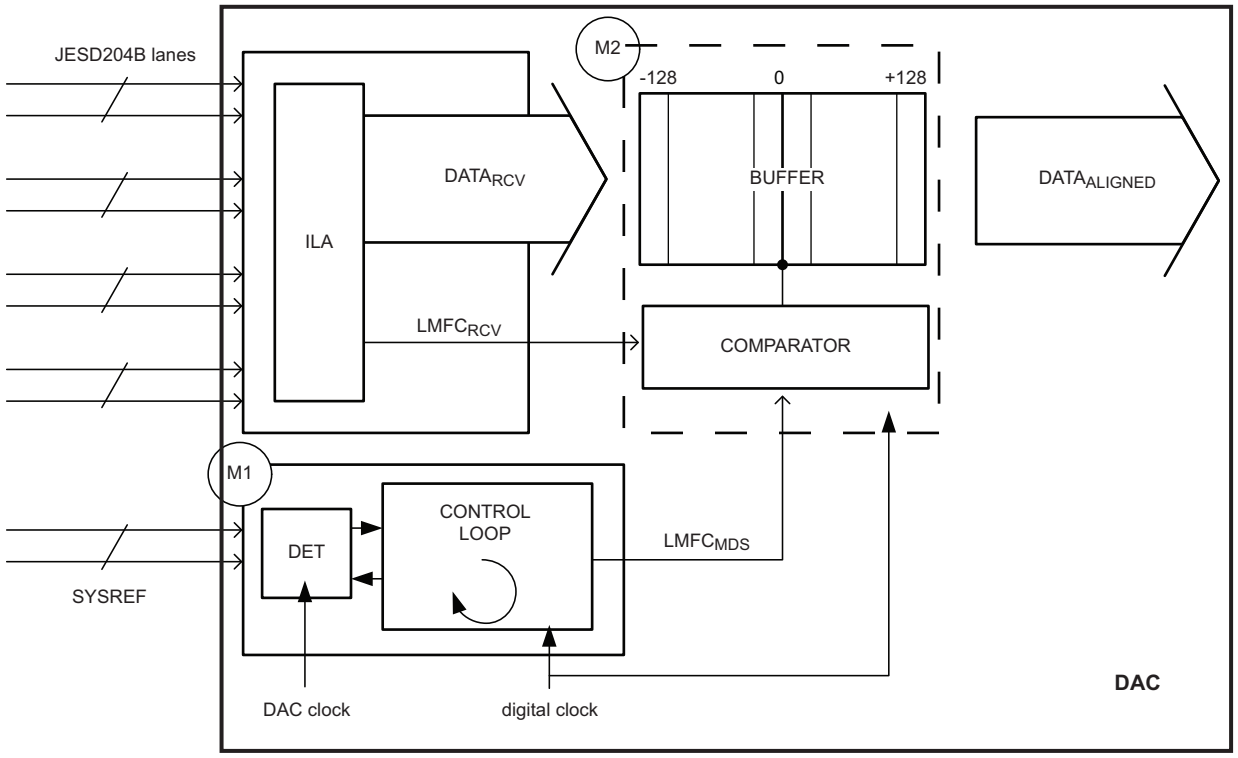


Fig 42. Modules of MDS implementation

11.6.4.1 Capturing the SYSREF signal

Module M1 ensures the capture of the SYSREF signal at DAC clock accuracy. This is done by an early-late detector and a control-loop. The control-loop must capture several SYSREF edges to deliver an accurate $LMFC_{MDS}$ signal to the M2 module. The Initialization of the control-loop is triggered by the edge detection of the SYSREF signal (see Figure 43). It stands for 30 digital clock cycles, after which the capture process starts. The capture is done during the capture window and is repeated at the end of every control

loop period until the signal is locked. The SYSREF edge must occur within the capture window. The capture process must be delayed to match this constraint. This is done by programming the capture delay register.

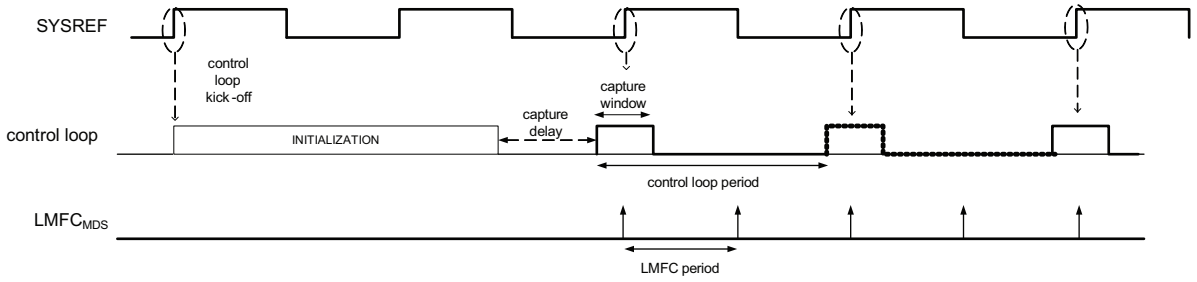


Fig 43. Capturing the SYSREF signal

Figure 44 shows an example on how to set up the M1 module.

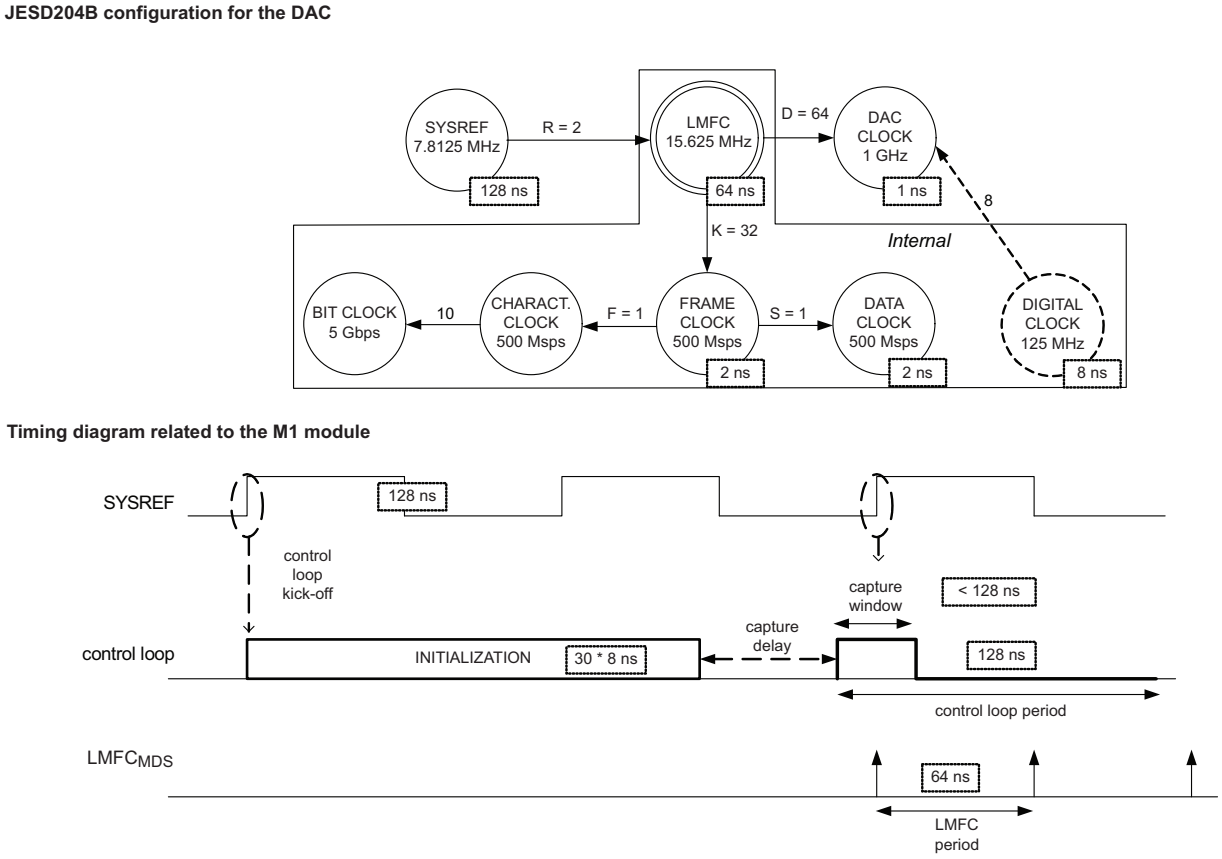


Fig 44. Example of how to set up the M1 module

The DAC165xQ requires the following parameters:

- **LMFC_PERIOD (register x0AA)**:
  Period of the LMFC in digital clock cycles (e.g. 8 × 8 ns)

- **CAPTURE_DELAY (register x0AC)**:

  Must be tuned using the following equation:

  $$initialization + capture\ delay = n \times SYSREF\ period$$

  Example:

  $$(30 \times 8\ ns) + (2 \times 8\ ns) = 2 \times 128\ ns$$

  The capture delay is expressed in digital clock period (for example 2 × 8 ns)

- **Capture window and control loop period**:

  These are specified using MDS_WIN_HIGH and MDS_WIN_LOW registers (respectively x0A9 and x0A8). They are expressed in digital clock cycles and must be set using the following equations:

  $$capture\ window = 2 \times (MDS\_WIN\_HIGH + 1)$$

  $$control\ loop\ period = capture\ window + MDS\_WIN\_LOW + 1$$

  Remark: The capture window must be smaller than the SYSREF period.

At the end of the capture process, the $LMFC_{MDS}$ signal is provided to the M2 module and the MDS_LOCK bit of the MDS status register is set to 1. If the M1 module cannot lock, the MDS_BSY flag is kept high and a mute action can be held .

11.6.4.2 Aligning the LMFCs and the data

Module M2 ensures the phase alignment of the $LMFC_{RCV}$ to the closest $LMFC_{MDS}$ edge. The $LMFC_{RCV}$ is issued from the digital lane processing by analyzing the ILA sequence using the multi-frames /A/ symbols present. The transmitter (TX) is expected to have its self-synchronization process to the global MFC_{SYSTEM}. It generates the ILA sequence based on the aligned $LMFC_{TX}$. The total latency of the link is compounded of a fixed value (due to PCB traces, devices internal fixed delays, etc.) and an undeterministic value (due to elastic buffers, clocks domains interface, etc.). By buffering the data and the $LMFC_{RCV}$ after the inter-lane alignment process, the M2 module is capable to adjust the position of the buffer delay to match the recovered $LMFC_{MDS}$.

Figure 45 shows the alignment process for two links. The two links have two different total latencies but due to the $LMFC_{TX}$ and $LMFC_{MDS}$ phase synchronization to the MFC_{SYSTEM}, the various devices are capable to align to the same MFC_{SYSTEM} edge in a fixed and deterministic way.

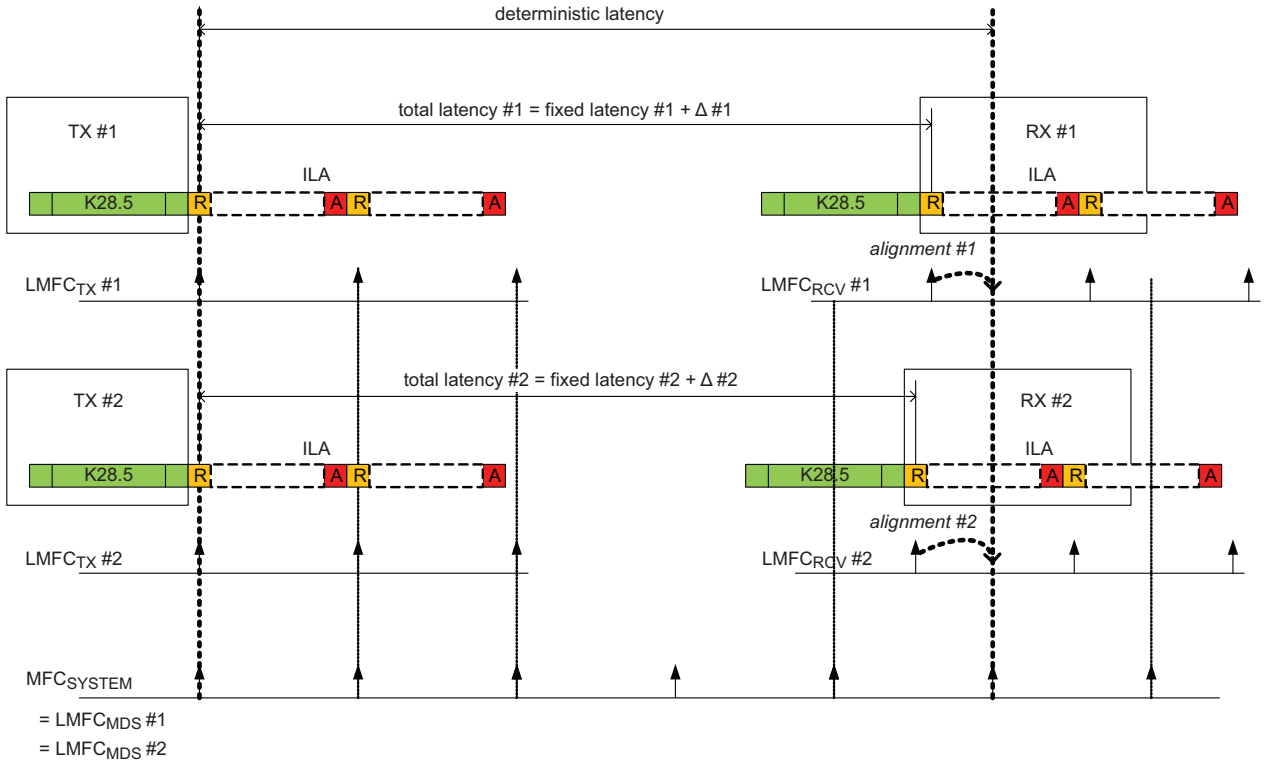


Fig 45. Multiple devices alignment process

Take special care when selecting the MFC_{SYSTEM} period. A longer period is better than a short one. In general, the MFC_{SYSTEM} period must be at least two times the maximum latency between devices to avoid a wrong edge selection as shown in Figure 46.

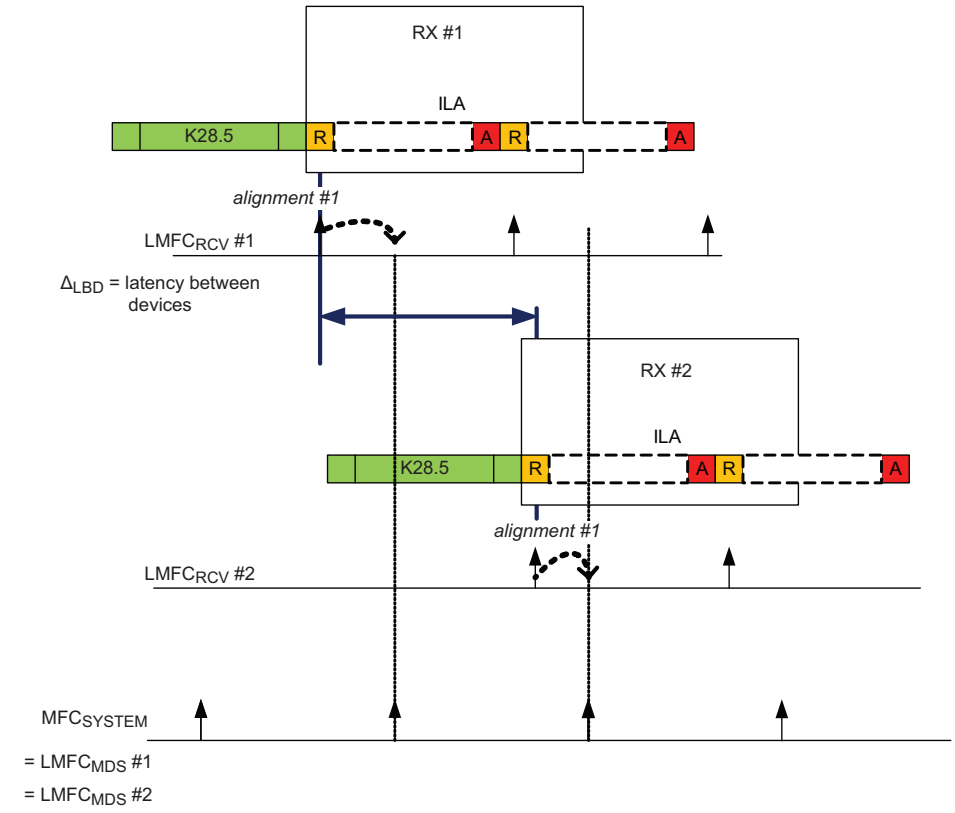
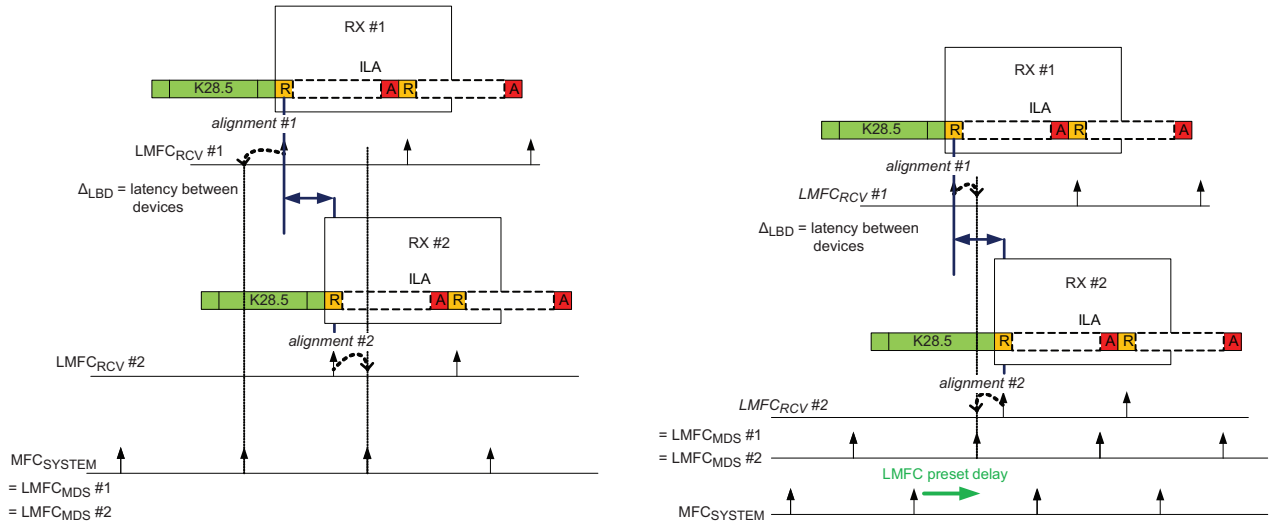


Fig 46. Wrong edge selection

In some cases, the latency between devices is small, but the edge is wrongly selected due to the closest edge criteria. To avoid this, a LMFC preset delay can be applied on all the $LMFC_{MDS}$ signals. It is important that all the DAC devices receive the same LMFC preset value. If not the latency is not exactly the same. This parameter is set with the LMFC_PRST register expressed in digital clock cycles. This value must be adjusted manually for each newly designed system.



a. Wrong edge selection

b. Correct edge selection with the LMFC preset delay

Fig 47. Edge selection

11.6.4.3 Monitoring the MDS process

The buffer adjustment performed using the M1 and M2 modules can be read back using the MDS_ADJ_DLY register . Bits 7 to 3 of this register represent the coarse delay expressed in digital clock cycles whereas bits 2 to 0 represent the fine adjustment in DAC clock cycles. The buffer adjustment has a default value of 80h.

11.6.4.4 Adding adjustment offset

The DAC165xQ allows adding an offset on top of the automatic adjustment. This is available via register MDS_OFFSET_DLY . The offset range is from −16 to 15 digital clock cycles. This offset value can be set at the start-up time as well as in at later period. This enables compensating a layout error or adding a specific phase to one DAC device.

Another adjustment delay can be set but only after a first automatic alignment using the manual adjustment delay register MDS_MAN_ADJ_DLY .

11.6.4.5 Selecting the SYSREF input port

The DAC165xQ incorporates two SYSREF differential ports: SYSREF_E_P/N (East side of the device) and SYSREF_W_P/N (West side of the device). One of these ports can be selected as the input for the SYSREF signal. Which port is selected is device dependent. One DAC165xQ uses the Eastern SYSREF while another DAC165xQ uses the Western SYSREF (see Figure 48).

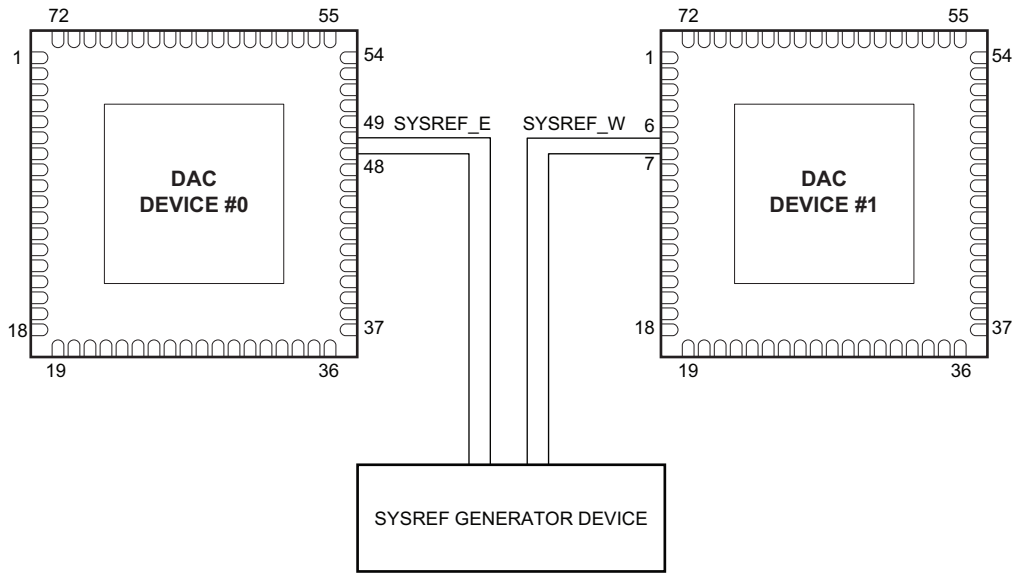


Fig 48. SYSREF differential ports

Register MDS_EAST_WEST is used to select between the East port or the West port. Each SYSREF input buffer has an optional internal differential resistor termination of about 100 Ω. This resistor can be enabled with registers MDS_SEL_EAST_RT and MDS_SEL_WEST_RT . The clock edge (rising/falling) on which the SYSREF signal is sampled can also be selected using registers MDS_SEL_FE_EAST and MDS_SEL_FE_WEST .

11.7 Interrupts

In some cases it may be useful if the host-controller is notified that a certain internal event has taken place by means of an interrupt . The DAC165xQ includes a simple interrupt (INTR) controller for this purpose.

The INTR-signal can be made available on one of the I/O pins. The polarity is programmable .

11.7.1 Events monitored

The DAC165xQ monitors various internal events and indicates their occurrence in the INTR_FLAGS_XY registers . The following event can be observed:

- INTR_DLP_XY:

  Digital Lane Processing (DLP) has its own interrupt controller. The result of this slave controller is provided to the main interrupt controller through the INTR_DLP_XY bit .
- MDS_BSY_XY and $\overline{\text{MDS\_BSY\_XY}}$:

  Refer to the activity of the MDS controller. During the synchronization phase, the MDS_BUSY signal is high, and come low once finished.
  - MDS_BSY_XY reflects the start of the activity of the MDS controller
  - $\overline{\text{MDS\_BSY\_XY}}$ reflects the end of the activity of the MDS controller
- TEMP_ALARM_XY:

Indicates that the temperature measured by the on-chip temperature sensor exceeds the threshold temperature .

- LVL_DET_OR_XY:

  Indicates that one of the level detectors is enabled.

- CA_ERR_XY:

  Indicates a DLP clock error.

- CLK_MON_XY:

  Indicates a CDI clock error.

- DCLK_ERR_MON_XY:

  Indicates a drift on the DCLK as specified by register INTR_DCLK_MON_RANGE_XY .

- ERR_RPT_FLAG_XY:

  Indicates the transmission of error reporting via the SYNCB interface.

- ALARM_STATE_XY:

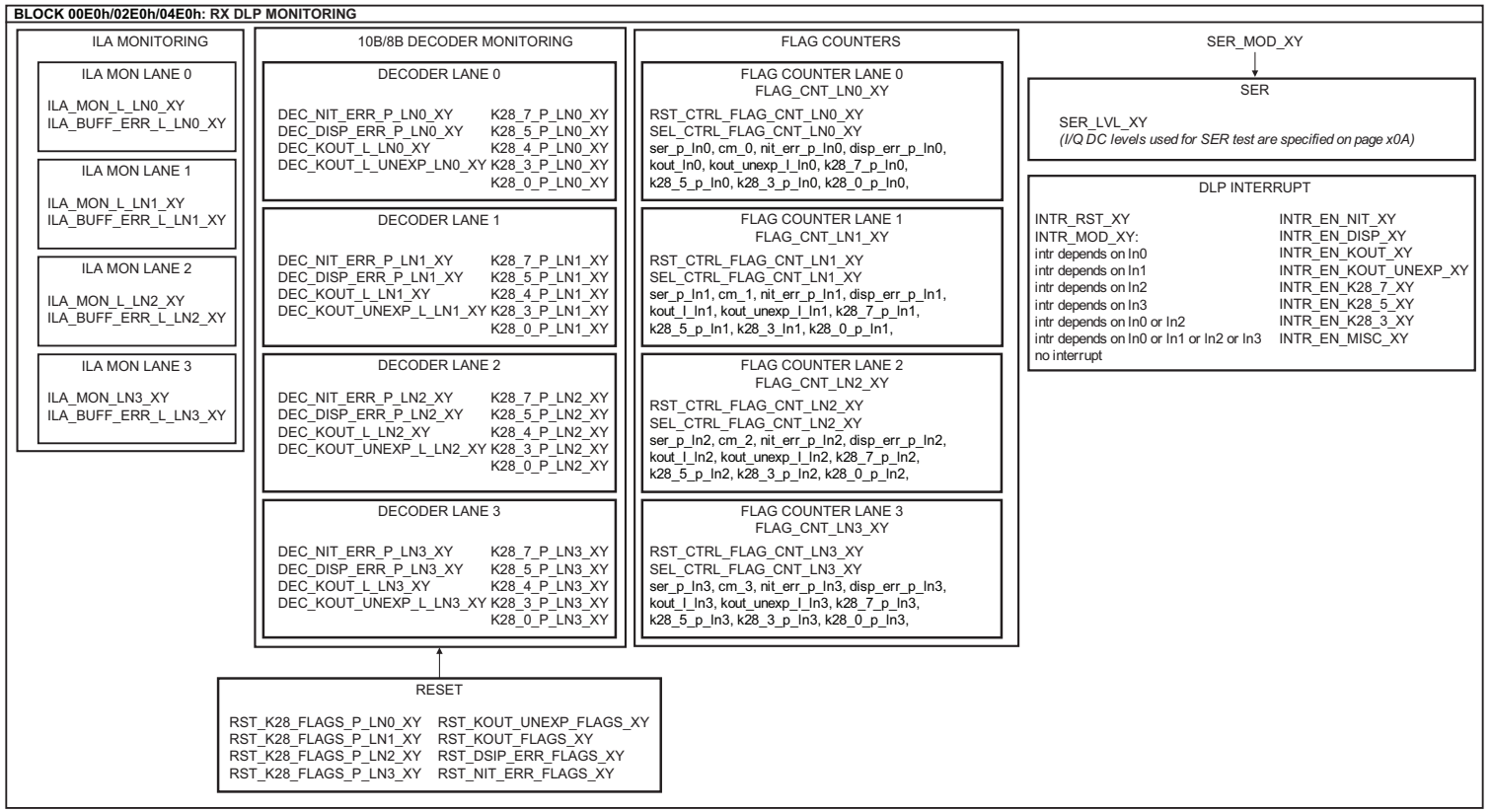
  Indicates when an auto-mute event occurs .

11.7.2 Enabling interrupts

An indication if an 0→1 transition of the corresponding monitor- or error indicator activates the INTR-signal can be given using the INTR_EN_XY registers . The INTR_FLAGS_XY registers indicate which of the selected events has invoked the interrupt. When bit INTR_RST_XY is set to 1 the flags and the INTR-signal are reinitialized.

11.7.3 Digital Lane Processing (DLP) interrupt controller

The DLP has its own interrupt controller that reports to the main interrupt controller. This DLP interrupt controller is managed from the SPI registers of block x00E0 (see Figure 49).



Block 00E0h = DAC A/B

Block 02E0h = DAC C/D

Block 04E0h = All DACs

Fig 49. Digital lane processing monitoring overview

As this interrupt controller is dedicated to the JESD204B serial interface the INTR_MOD_XY bits must be specified according to the LMF configuration used in the system.

Table 27. INTR_MOD settings

INTR_MOD_XY	Interrupt setting[1]	Nominal LMF use[2]
000	DLP interrupt depends on lane 0	124
001	DLP interrupt depends on lane 1	124
010	DLP interrupt depends on lane 2	124
011	DLP interrupt depends on lane 3	124
100	DLP interrupt depends on lane 0 or lane 2	222
101	DLP interrupt depends on lane 0 or lane 1 or lane 2 or lane 3	421 / 422
110	HOLD_FLAG_CNT_EN_XY[3]	-
111	no interrupt	-

[1] The lane numbering refers to the logical lanes

[2] Any mode can also be used for debug purposes.

[3] The "HOLD_FLAG_CNT_EN_XY" feature is explained in .

Register INTR_DLP_XY is reinitialized when the bit INTR_RST_XY control is set to logic 1 .

The DLP events that can be monitored with the interrupt controller are programmable via register INTR_EN_XY . Those events are related to the lanes specified by the INTR_MOD_XY bits in register INTR_SER_CTRL_XY . They can be enabled by the following bits:

- INTR_EN_NIT_XY: A Not-In-Table (NIT) error has occurred on one of the lanes
- INTR_EN_DISP_XY: A disparity error has occurred on one of the lanes
- INTR_EN_KOUT_XY: K control characters have been detetected on one of the lanes
- INTR_EN_KOUT_UNEXP_XY: An unexpected K control character has been detected on one of the lanes
- INTR_EN_K28_7_XY: A K28.7 symbol has been detected on one of the lanes
- INTR_EN_K28_5_XY: A K28.5 symbol has been detected on one of the lanes
- INTR_EN_K28_3_XY: A K28.3 symbol has been detected on one of the lanes
- INTR_EN_MISC_XY: An event related to the INTR_MISC_EN_XY register has occurred

  Register INTR_MISC_EN_XY refers to two kinds of events, mainly for debug purposes:

  - Lane x has reached the CS_INIT state
  - An error has occurred in the ILA alignment process on lane x

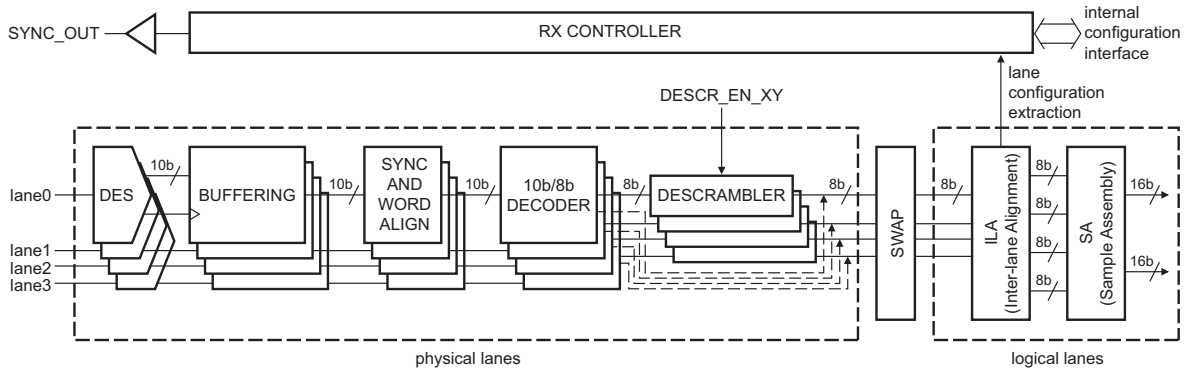
When register INTR_DLP_XY is invoked, the “FLAGS” registers must be read to determine which event has occurred:

- An INTR_EN_NIT_XY event is related to the DEC_NIT_ERR_P_LNx_XY bits of register DEC_FLAGS_XY
- An INTR_EN_DISP_XY event is related to the DEC_DISP_ERR_P_LNx_XY bits of register DEC_FLAGS_XY
- An INTR_EN_KOUT_XY event is related to the DEC_KOUT_L_LNx_XY bits of register KOUT_FLAG_XY
- An INTR_EN_KOUT_UNEXP_XY event is related to the DEC_KOUT_UNEXP_L_LNx_XY bits of register KOUT_UNEXP_FLAG_XY
- An INTR_EN_K28_7 event is related to the K28_7_LNx bits of register K28_FLAG
- An INTR_EN_K28_5 event is related to the K28_5_LNx bits of register K28_FLAG
- An INTR_EN_K28_3 event is related to the K28_3_LNx bits of register K28_FLAG
- An INTR_EN_MISC_XY event is related to the CS_STATE_LNx_XY bits of register CS_STATE_LN_XY and the ILA_BUFF_ERR_LNx_XY bits of register ILA_BUFF_ERR_XY register

All flag bits can be reset using register RST_FLAGS_MON_XY .

11.7.4 JESD204B physical and logical lanes

The DAC165xQ integrates a JESD204B serial interface with a high flexibility of configuration.



The descrambler can be enabled or disabled.

Fig 50. JESD204B receiver

Because of various implementations for JESD204B transmitter devices, a flexible configuration of the physical lanes is required. This configuration allows the lane polarity to invert individually and to arbitrary swap the lane order. Identifying the lane numbers can be confusing because of the lane swapping. Two terms, Physical and Logical, are used in this document to explicitly identify the lanes.

Physical lanes:

The DAC165xQ integrates four JESD204B serial receivers that are referenced via the pinning information (see Figure 2).

- DAC A/B physical lane 0 refers to the signal coming from pins VIN_AB_P0 and VIN_AB_N0
- DAC_A/B physical lane 1 refers to the signal coming from pins VIN_AB_P1 and VIN_AB_N1
- DAC A/B physical lane 2 refers to the signal coming from pins VIN_AB_P2 and VIN_AB_N2
- DAC A/B physical lane 3 refers to the signal coming from pins VIN_AB_P3 and VIN_AB_N3
- DAC C/D physical lane 0 refers to the signal coming from pins VIN_CD_P0 and VIN_CD_N0
- DAC C/D physical lane 1 refers to the signal coming from pins VIN_CD_P1 and VIN_CD_N1
- DAC C/D physical lane 2 refers to the signal coming from pins VIN_CD_P2 and VIN_CD_N2
- DAC C/D physical lane 3 refers to the signal coming from pins VIN_CD_P3 and VIN_CD_N3

Logical lanes:

The DAC165xQ incorporates a Swap lanes module (see Figure 7) that allows a remapping of the lane numbers to be compatible with the system implementation.

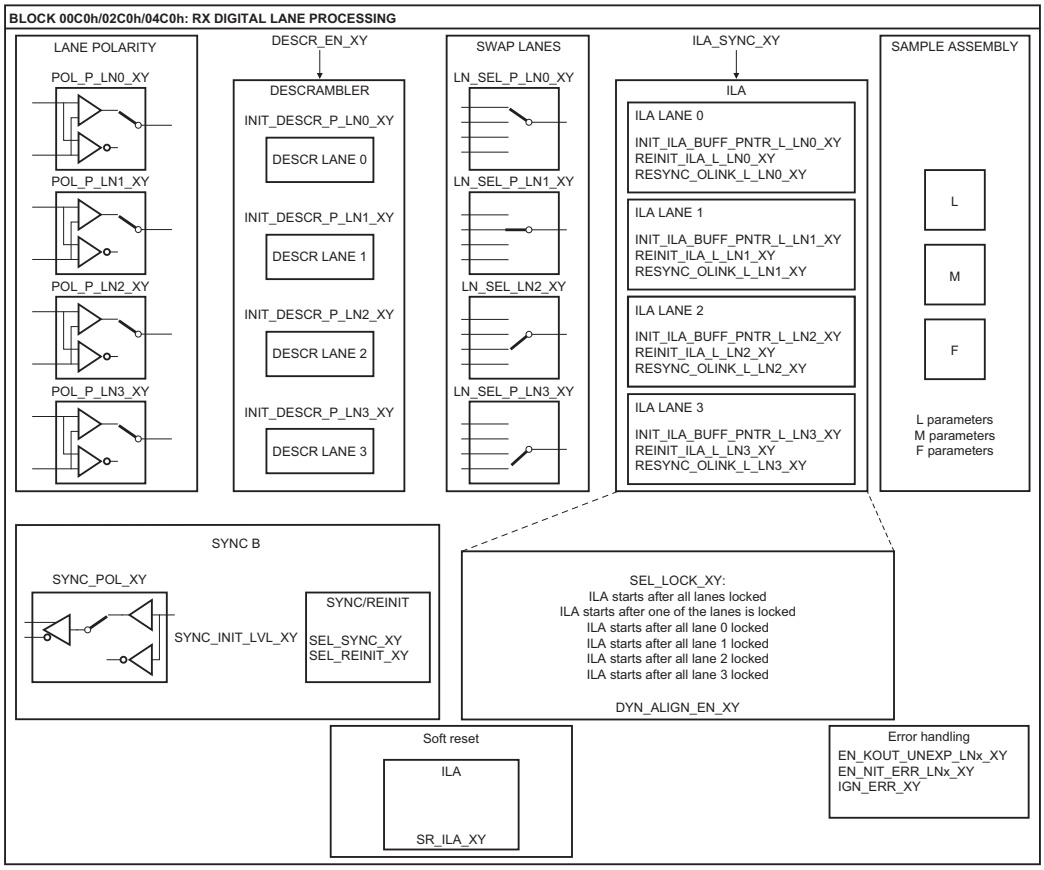
- DAC A/B logical lane 0 refers to the lane specified with the LN_SEL_P_LN0_XY bits in register LN_SEL_XY (00CDh)
- DAC A/B logical lane 1 refers to the lane specified with the LN_SEL_P_LN1_XY bits in register LN_SEL_XY (00CDh)
- DAC A/B logical lane 2 refers to the lane specified with the LN_SEL_P_LN2_XY bits in register LN_SEL_XY (00CDh)
- DAC A/B logical lane 3 refers to the lane specified with the LN_SEL_P_LN3_XY bits in register LN_SEL_XY (00CDh)
- DAC C/D logical lane 0 refers to the lane specified with the LN_SEL_P_LN0_XY bits in register LN_SEL_XY (02CDh)
- DAC C/D logical lane 1 refers to the lane specified with the LN_SEL_P_LN1_XY bits in register LN_SEL_XY (02CDh)
- DAC C/D logical lane 2 refers to the lane specified with the LN_SEL_P_LN2_XY bits in register LN_SEL_XY (02CDh)
- DAC C/D logical lane 3 refers to the lane specified with the LN_SEL_P_LN3_XY bits in register LN_SEL_XY (02CDh)

The following naming convention are used to distinguish between the physical lanes and the logical lanes in the SPI registers: “P_LNx” is used to identify the physical lanes. “L_LNx” is used to identify the logical lanes. “x” stands for the lane number in both cases.

11.7.5 RX Digital Lane Processing (DLP)

Digital lane processing is the module containing all JESD204B interface controls except the PHY deserializer.

Figure 51 shows the registers for the configuration of the digital lane processing.



Block 00C0h = DAC A/B

Block 02C0h = DAC C/D

Block 04C0h = All DACs

Fig 51. RX digital lane processing overview

11.7.5.1 Lane polarity

Each physical lane polarity can be individually inverted with the POL_P_LNx_XY bits of register P_LN_POL_XY . Using this feature transforms the 10 bits from ABCDEFGHIJ to ABCDEFGHIJ.

11.7.5.2 Lane clocking edge

Each physical lane can be sampled either by the rising edge or the falling edge of the internal clocking system. This is accomplished by asserting/deasserting the SEL_RF_F10_P_LNx_XY bits of register CA_CTRL_XY .

11.7.5.3 Scrambling

The descrambler is a 16-bit parallel self-synchronous descrambler based on the polynomial $1 + x^{14} + x^{15}$. From the JESD204B specification, the scrambling/descrambling process only occurs on the user data, not on the code group synchronization or the ILA sequence. After two received bytes, the descrambler is correctly set up to decode the data in the proper way. However, it the initial state of the descrambler bits is set incorrectly, the two first decoded bytes are decoded incorrectly. The JESD204B specification proposes an initial state for both scrambler and descrambler to avoid this.

Using registers INIT_DESCR_P_LNx_XY any kind of intitial state can be set in the DAC165xQ. The descrambling process starts when the ILA sequence has finished. This process can be turned off by deasserting bit DESCR_EN_XY in register ILA_CTRL_1_XY .

11.7.5.4 Lane swapping and selection

If the physical lanes do not match with the ordering of the transmitter lanes, they can be reordered using the lane swapping module. As the DAC165xQ allows various LMF configurations , it is important that the lane swapping respects the following reordering constraints linked to the L value (see Table 28).

Table 28. Logical lanes versus L values

L value		Logical lanes used for the Sample assembly module
Binary	**Decimal**	
DAC A/B		
100	4	logical lane 0
		logical lane 1
		logical lane 2
		logical lane 3
010	2	logical lane 0
		logical lane 2
001	1	logical lane 0
DAC C/D		
100	4	logical lane 0
		logical lane 1
		logical lane 2
		logical lane 3
010	2	logical lane 0
		logical lane 2
001	1	logical lane 0

The selection of the logical lanes can be is specified by the LN_SEL_L_LNx_XY bits of register LN_SEL_XY .

Table 29 shows the possible choices regarding the value of the L parameter.

Table 29. Lane mapping between logical and physical lanes regarding the L value

L	4	2	1
DAC A/B			
logical lane 0	physical lane 0 or physical lane 1 or physical lane 2 or physical lane 3	physical lane 0 or physical lane 1 or physical lane 2 or physical lane 3	physical lane 0 or physical lane 1 or physical lane 2 or physical lane 3
logical lane 1	physical lane 0 or physical lane 1 or physical lane 2 or physical lane 3	not used	not used
logical lane 2	physical lane 0 or physical lane 1 or physical lane 2 or physical lane 3	physical lane 0 or physical lane 1 or physical lane 2 or physical lane 3	not used
logical lane 3	physical lane 0 or physical lane 1 or physical lane 2 or physical lane 3	not used	not used

Table 29. Lane mapping between logical and physical lanes regarding the L value

L	4	2	1
DAC C/D			
logical lane 0	physical lane 0 or physical lane 1 or physical lane 2 or physical lane 3	physical lane 0 or physical lane 1 or physical lane 2 or physical lane 3	physical lane 0 or physical lane 1 or physical lane 2 or physical lane 3
logical lane 1	physical lane 0 or physical lane 1 or physical lane 2 or physical lane 3	not used	not used
logical lane 2	physical lane 0 or physical lane 1 or physical lane 2 or physical lane 3	physical lane 0 or physical lane 1 or physical lane 2 or physical lane 3	not used
logical lane 3	physical lane 0 or physical lane 1 or physical lane 2 or physical lane 3	not used	not used

11.7.5.5 Word locking and Code Group Synchronization (CGS)

When the bits are received from the RX physical layer, DLP has to identify the MSB and LSB boundaries of the 10-bit codes from the bitstream. This can be monitored using the LOCK_CNT_MON_LN01_XY and LOCK_CNT_MON_LN23_XY registers .

When all lanes are locked, the values of the registers are stable and the code group synchronization process can start. This process is described by the JESD204B specification and is represented by the state machine shown in Figure 52.

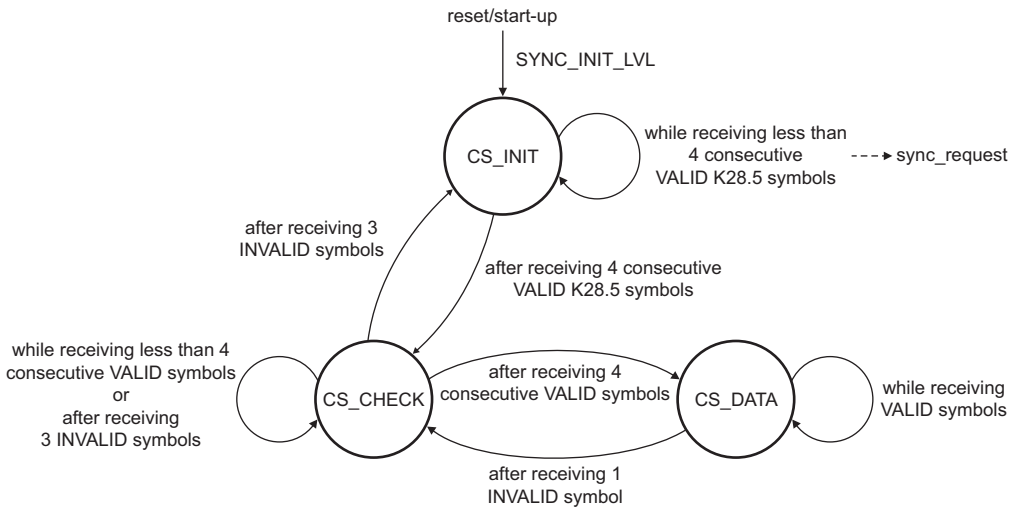


Fig 52. Code group synchronization

The CGS states of each lane can be monitored using the CSYNC_STATE_P_LNx_XY bits of register CSYNC_STATE_LNx_XY . The definition of each state can be found in Table 30.

Table 30. Code group synchronization state machine

CSYNC_STATE_LNn[1:0]	Name	Definition
00	CSYNC_INIT	looking for K28_5 (/K/) symbol
01	CSYNC_CHCK	four consecutive K28_5 (/K/) symbols have been received
10	CSYNC_DATA	code group synchronization achieved

11.7.5.6 SYNC configuration

The SYNC signal is the feedback signal that is sent to the transmitter device to ensure the JESD204B link synchronization. When all lanes are in CSYNC_INIT state a synchronization request is sent to the SYNC buffer that is linked to pins SYNC_OUTP and SYNC_OUTN (see Figure 2).

The polarity of this buffer is controlled by bit SYNC_POL_XY of register SYNCOUT_MOD_XY . By default the sync_request is active low. The sync_request signal can be specified by bits SEL_SYNC and SYNC_INIT_LVL of register SYNCOUT_MOD_XY register. Bit SYNC_INIT_LVL_XY of register SYNCOUT_MOD_XY only specifies the state of the sync_request signal after resetting the CGS state machine (at start-up time or after device reset only).

Table 31. Sync_request control

SEL_SYNC[2:0]	Description
000	sync_request active when state machine of one of the lanes is in CS_INIT mode
001	sync_request active when state machine of all lanes is in CS_INIT mode
010	sync_request active when state machine of lane 0 is in CS_INIT mode
011	sync_request active when state machine of lane 1 is in CS_INIT mode

Table 31. Sync_request control *...continued*

SEL_SYNC[2:0]	Description
100	sync_request active when state machine of lane 2 is in CS_INIT mode
101	sync_request active when state machine of lane 3 is in CS_INIT mode
110	sync_request fixed to 1
111	sync_request fixed to 0

11.7.5.7 Inter-lane alignment

This module handles the alignment of the logical lanes based on the ILA sequence described in the JESD204B specification. Inter-lane alignment starts when all lanes are locked and at reception of the first non-K28.5 (or /K/) symbol.

During the ILA sequence, the K28.3 (/A/ symbol) is used to align the data streams. During this sequence, the length (K) of the multi-frame is measured. This value is used by the lane monitoring and correction process. The value is also used for the MDS circuitry, where the SYSREF signal is expected to be a multiplication of the multi-frame length (K) in the JESD204B specification.

During the second multi-frame, the JESD204B configuration data of each physical lane is stored in register blocks x0120 and x0140 (see Figure 53). The DAC165xQ does not do anything with these configuration data. They are only made available for the host controller.

BLOCK nnn0h: JESD204 READ CONFIGURATION (DAC X/Y)

JESD204 CONFIGURATION

CONFIG 0	P_LN_DID	
CONFIG 1	P_LN_ADJ_CNT	P_LN_BID
CONFIG 2	P_LN_ADJ_DIR P_LN_ADJ_PH	P_LN_LID
CONFIG 3	P_LN_SCR	P_LN_L
CONFIG 4	P_LN_F	
CONFIG 5		P_LN_K
CONFIG 6	P_LN_M	
CONFIG 7	P_LN_CS	P_LN_N
CONFIG 8	P_LN_SBCLSS_VS	P_LN_N'
CONFIG 9	P_LN_JESD_VS	P_LN_S
CONFIG 10	P_LN_HD	P_LN_CF
CONFIG 11	P_LN_RES1	
CONFIG 12	P_LN_RES2	
CONFIG 13	P_LN_FCHK	

Fig 53. JESD204 read configuration for physical lanes overview

Table 32. Overview of generic parts of register addresses

	DAC A/B	DAC C/D
lane 0	nnn = 012	nnn = 032
lane 1	nnn = 013	nnn = 033
lane 2	nnn = 014	nnn = 034
lane 3	nnn = 015	nnn = 035

The inter-lane alignment synchronization is enabled by default, but it can be disabled using bit ILA_SYNC_XY of register ILA_CTRL_1_XY register . When ILA is disabled, the lane-alignment can be done manually using registers MAN_ALIGN_P_LN_1_0_XY . The manual mode must first be enabled using bit FORCE_ALIGN_XY of register FORCE_ALIGN_XY .

The ILA module uses a 16-bit buffer for each lane. The first /A/ symbol received over the lanes is used as reference. The /A/ symbols of the other lanes, which are received later, are compared to the first one to be all aligned. The initial location of the symbols is predefined by the INIT_ILA_BUFF_PNTR_L_LN01_XY and INIT_ILA_BUFF_PNTR_L_LN23_XY registers . The alignment can be monitored with the ILA_MON_L_LNn_XY bits of the ILA_MON_L_LN10 and ILA_MON_L_LN32 registers . If the lane difference is too great, a buffer out of range error occurs, which can be monitored with bits ILA_BUFF_ERR_L_LNx_XY of the ILA_BUFF_ERR_XY register . In this specific case, a reinitialization of the full link can be requested by setting the REINIT_ILA_L_LNx_XY bits of the REINIT_CTRL_XY register.

The JESD204B specification also mentions a dynamic realignment mode where a monitoring process is checking the /A/-symbol location. This can realign the data stream if two successive /A/ symbols are found at the same new position. By default this monitoring and correction process is disabled to avoid any moving latency over the link, but one can enable the feature by setting bit DYN_ALIGN_EN_XY of the FORCE_ALIGN_XY register .

11.7.5.8 Character replacement

Character replacement, as specified by the JESD204B specification, can occur at the end of the frame (K28.7 or /F/ symbol) or at the end of the multi-frame (K28.3 or /A/ symbol). By default this feature is enabled, but it can be disabled using bit FRAME_ALIGN_EN_XY of the FORCE _LOCK register .

Remark: The DAC165xQ can handle multi-frame length values (K) between $ceil(17/F)$ and 32 but with the restriction that the number of octets in a multi-frame must always be even. This implies that if F = 1, a value of K = 17 is not allowed. When F = 1 only even values > 17 are allowed. Working with F = 1 and K = 17 often implies that the character replacement process is not reliable.

11.7.5.9 Sample assembly

Sample assembly handles the assembly of the data based on the LMF parameters described by the LMF_CTRL register . The following configurations are supported:

- LMF = 421
- LMF = 422
- LMF = 222

- LMF = 124

Sample assembly is based on the logical lanes definition when updating the L value .

11.7.5.10 Resynchronization over links

The DAC165xQ recognizes a K28.5 (/K/) symbols sequence coming over its lanes. This identification allows resynchronization of the device if the RESYNC_OLINK_L_LNx_XY bits of register REINIT_CTRL_XY are set correctly .

11.7.5.11 Symbols detection monitoring and error handling

The DLP decodes the 10-bit words to 8-bit words. The decoding table is specified in the IEEE 802.3-2005 specification. During decoding, the disparity is calculated according to the disparity rules mentioned in the same specification. The JESD204B specification also defines the following definitions:

- VALID:

  The code group is found in the column of the 10b/8b decoding tables according to the current running disparity.
- DISPARITY ERROR:

  The received code group exists in the 10b/8b decoding table, but is not found in the correct column according to the current running disparity.
- NOT-IN-TABLE (NIT) ERROR:

  The received code group is not found in the 10b/8b decoding table of either disparity.
- INVALID:

  A code group that either shows a disparity error or that does not exist in the 10b/8b decoding table.

The Not-In-Table error (NIT) and Disparity error (DISP) can be monitored using bits DEC_NIT_ERR_P_LNx_XY and DEC_DISP_ERR_P_LNx_XY of the DEC_FLAGS_XY register . Both are considered Invalid, but the DAC165xQ has some flexibility in this definition. Using the NAD_ERR_CORR bit of the ERR_HNDLNG register either NIT errors only or NIT errors and disparity errors can be set as INVALID. Moreover, the specified invalid errors can also be totally ignored by setting the bit IGN_ERR_XY of the ERR_HNDLNG register to logic 1 . This specific mode is designed for debug purposes only, especially when sample error measurement needs to be executed.

The VALID/INVALID status of the decoded word can trigger the MUTE feature using bits DATA_V_IQ_CFG_XY of the MUTE_CTRL_1_XY register .

The following comma symbols are detected during data transmission irrespective of the running disparity:

/K/ = K28.5

/F/ = K28.7

/A/ = K28.3

/R/ = K28.0

/Q/ = K28.4

Their single detection is monitored in registers KOUT_FLAG_XY and K28_FLAG_XY (.

During the data transmission phase, only K28.3 (/A/) and K28.7 (/F/) symbols are expected. Sometimes (e.g. wrong bit transmission), a code group is interpreted as a K character that is not K28.3 or K28.7. If this occurs a KOUT_UNEXP flag is asserted that can be read using bits DEC_KOUT_UNEXP_L_LNx_XY of the KOUT_UNEXP_FLAG_XY (.

All the previous flags can be reset using the RST_FLAGS_MON_XY register . Detection of them can also assert the DLP interrupt .

11.7.6 Monitoring and test modes

The DAC165xQ embeds various monitoring and test modes that are useful during the prototyping phase of a system.

Remark: The test capability linked to observing specific characters, errors or state machine statuses is not reviewed in this section. It is up to the reader to define specific modes based on the DAC165xQ capability.

11.7.6.1 Flag counters

Due to the high data rate of the JESD204B serial interface, it is hard to monitor events that occur on the lanes in real time. Four multi-purpose counters have been added to the design to help this monitoring. Each counter is 16 bits wide and is linked to one lane. It increments its value each time a specific event occurs. These flags counters can be read using the FLAG_CNT_LNx_XY registers and reset using the RST_CTRL_FLAG_CNT_LNx_XY bits of the CTRL_FLAG_CNT_LNxx registers The flag counters can also be reset automatically when DLP is reset by setting the AUTO_RST_FLAG_CNTS_XY bit of register RST_BUFF_ERR_FLAGS to logic 1.

The specification of the event that increments the counter is done by setting the SEL_CTRL_FLAGS_CNT_LNxx_XY bits of the CTRL_FLAG_CNT_LNxx_XY registers to one of the sources described in Table 33.

Table 33. Counter source
Default settings are shown highlighted.

SEL_CFC_LNn[2:0]	Source
000	not-in-table error
001	disparity error
010	K symbol not found
011	unexpected K symbol found
100	K28_7 (/F/) symbol found
101	**K28_5 (/K/) symbol found**
110	K28_3 (/A/) symbol found
111	K28_0 (/R/) symbol found

When the counter is reaching its maximum value (0xFFFF), this value is held until the next counter reset. Bit HOLD_FLAG_CNT_EN_XY of the RST_BUFF_ERR_FLAGS_XY register gives two options for when a counter reaches the maximum value.

Table 34. HOLD_FLAG_CNT_EN_XY options
Default settings are shown highlighted.

HOLD_FLAG_CNT_EN_XY	Option
0	**All counters are independent. Each counter continues its own counting.**
1	All counters are linked. When one counter reached the maximum value and stops, all other counters stop as well.

When the counters are stopped, an interrupt can be activated .

This feature makes it possible to, for instance, analyze the occurrence of character replacement or NIT errors.

11.7.6.2 Sample Error Rate (SER)

A sample error rate feature is implemented in the DAC165xQ to analyze the quality of the transmission. Due to the 8b10b encoding, the analysis is done at sample level only and not at bit level. The transmitter sends a constant data over the link and the DAC165xQ compared this received value to the value specified in the SER_LVL_XY_LSB and SER_LVL_XY_MSB registers . Enable the scrambling on both transmitter and receiver side to add more random effect on the data. The SER_LVL_XY_MSB and SER_LVL_XY_LSB are specifying a 16-bit value at the lane level, it means the device can be considered as operating in one of two modes:

- F = 2 mode:

  The lane is receiving 16-bit data specified by SER_LVL_XY_MSB and SER_LVL_XY_LSB.
- F = 1 mode:

  The lane is receiving alternately 8-bit data specified by SER_LVL_XY_MSB and SER_LVL_XY_LSB.

The SER mode requires that the DAC is already synchronized (using CGS and ILA sequence). The kick-off of the measurement is done by setting the SER_MOD_XY bit of register SER_INTR_CTRL_XY . In this mode, the flags counters are used to count the number of 16-bit samples that do not match the SER_LVL_XY value. This mode enables the establishing of the sample error rate of each lane.

11.7.6.3 JTSPAT test

The Jitter Tolerance Scrambled PATtern (JTSPAT) is an 1180-bit pattern intended for receiving jitter tolerance testing for scrambled systems. The JTSPAT test pattern consists of two copies of JSPAT and an additional 18 characters intended to cause extreme late and early phases in the CDR PLL followed by a sequence, which can cause an error (i.e. an isolated bit following a long run). This pattern was developed to stress the receiver within the boundary conditions established by scrambling.

Table 35. Jitter tolerance scrambled pattern symbols sequence[1]

D1.4 0111010010	D16.2 0110110101	D24.7 0011001110	D30.4 1000011101	D9.6 1001010110	D10.5 0101011010
D16.2 1001000101	D7.7 1110001110	D24.0 0011001011	D13.3 1011000011	D23.4 0001011101	D13.2 1011000101
D13.7 1011001000	D1.4 0111010010	D7.6 1110000110	D0.2 1001110101	D21.5 1010101010	D22.1 0110101001
D23.4 0001011101	D20.0 0010110100	D27.1 1101101001	D30.7 1000011110	D17.7 1000110001	D4.3 1101010011
D6.6 0110010110	D23.5 0001011010	D7.3 1110001100	D19.3 1100101100	D27.5 110101010	D19.3 1100100011
D5.3 1010010011	D22.1 0110101001	D5.0 1010010100	D15.5 0101111010	D24.7 0011001110	D16.3 1001001100
D1.2 0111010101	D23.5 0001011010	D29.2 1011100101	D31.1 0101001001	D10.4 0101011101	D4.2 0010100101
D5.5 1010011010	D10.2 0101010101	D21.5 1010101010	D10.2 0101010101	D21.5 1010101010	D20.7 0010110111
D11.7 1101001000	D20.7 0010110111	D18.7 0100110001	D29.0 1011100100	D16.6 0110110110	D25.3 1001100011
D1.0 1000101011	D18.1 0100111001	D30.5 1000011010	D5.2 1010010101	D21.6 1010100110	D1.4 0111010010
D16.2 0110110101	D24.7 0011001110	D30.4 1000011101	D9.6 1001010110	D10.5 0101011010	D16.2 1001000101
D7.7 1110001110	D24.0 0011001011	D13.3 1011000011	D23.4 001011101	D13.2 1011000101	D13.7 1011001000
D1.4 0111010010	D7.6 1110000110	D0.2 1001110101	D21.5 1010101010	D22.1 0110101001	D23.4 0001011101
D20.0 0010110100	D27.1 1101101001	D30.7 1000011110	D17.7 1000110001	D4.3 1101010011	D6.6 0110010110
D23.5 0001011010	D7.3 1110001100	D19.3 1100101100	D27.5 1101101010	D19.3 1100100011	D5.3 1010010011
D22.1 0110101001	D5.0 1010010100	D15.5 0101111010	D24.7 0011001110	D16.3 1001001100	D1.2 0111010101
D23.5 0001011010	D27.3 1101100011	D3.0 1100010100	D3.7 1100011110	D14.7 0111001000	D28.3 0011101100
D30.3 0111100011	D30.3 1000011100	D7.7 1110001110	D7.7 0001110001	D20.7 0010110111	D11.7 1101001000
D20.7 0010110111	D8.7 0100110001	D29.0 1011100100	D16.6 0110110110	D25.3 1001100011	D1.0 1000101011
D18.1 0100111001	D30.5 1000011010	D5.2 1010010101	D21.6 1010100110		

[1] This table must be read, starting from the top, left-to-right first and then line-by-line to follow the sequence.

The DAC165xQ embeds a JTSPAT checker. The control registers are located in the JESD204 receiver monitoring registers block .

11.7.6.4 DLP strobe

The data coming out of the ILA module can be sampled by setting the DLP_STROBE_XY bit of the MISC_CTRL register . On each lane two octets are stored, which can be read out through registers P_LNxx_SMPL_MSB and P_LNxx_SMPL_LSB . The selection of the lane to read out the data is done by registers P_LN10_SEL and P_LN32_SEL .

11.7.7 IO-mux

The DAC165xQ uses two general purpose pins, IO0 and IO3. IO0 is always an output. IO1 can be configured as an input or as an output by setting the IO_EN bit of the EHS_CTRL register .

When acting as an output, the two IO pins are multiplexed to internal signals that can be useful for debug purposes. Table 36 shows the main configuration when using bits IO_SEL_x of the IO_MUX_CTRL_x register. The definitions of the three registers depend of the "Indicator" and the "Range" values used to specify the Signal that is sent through pins IO0 and IO1 (see tables below).

Table 36. Definition of IO_SEL registers

Register name	b7	b6	b5	b4	b3	b2	b1	b0
IO_SEL_4	IO3 indicator[1:0]		IO2 indicator[1:0]		IO1 indicator[1:0]		IO0 indicator[1:0]	
IO_SEL_3	IO3 range[7:0]							
IO_SEL_2	IO2 range[7:0]							
IO_SEL_1	IO1 range[7:0]							
IO_SEL_0	IO0 range[7:0]							

Table 37. Output signals for combination of indicators and ranges

Indicator[1:0]	Range[7:0]	Output signal
00	xxxx xxx0	IO0: WCLK IO1: DCLK
00	xxxx 0011	synchronization
10	1111 0000	end of ILA
10	1111 0001	$\overline{\text{end of ILA}}$
11	1100 0000	$\overline{\text{interrupt}}$
11	1100 0001	interrupt
11	1111 even	IO0: fixed to logic 1 IO1: fixed to logic 0
11	1111 odd	IO0: fixed to logic 0 IO1: fixed to logic 1

11.7.8 DLP latency

The variable delay (latency uncertainty) is the result of uncertainties and variation in design implementations along the path between the transmit logic device and the DAC165xQ. The Inter-Lane Alignment (ILA) module present in Digital Layer Processing (DLP) realigns the input streams to the last data received.

Table 38. Digital layer processing latency

Symbol	Parameter	Conditions	Test[1]	Min	Typ	Max	Unit
t_d	delay time	digital layer processing delay	D	11	-	26	cycles[2]

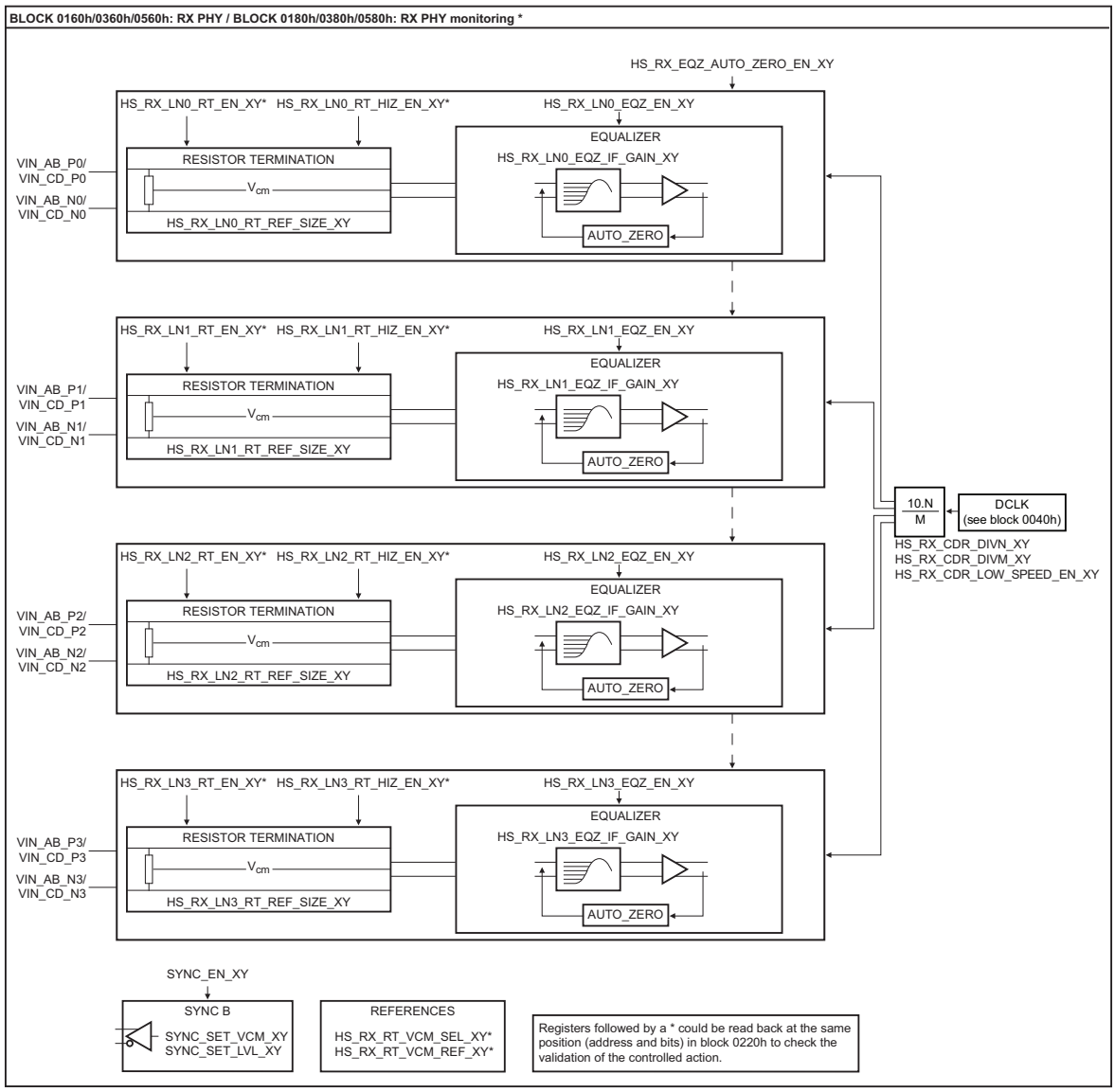
[1] D = garantueed by design.

[2] WCLK clock cycle.

11.8 JESD204B PHY receiver

Each JESD204B lane owns its own physical deserializer (RX PHY) that provides the 10-bit data stream to the DLP module. The SPI registers of block x0160 control the various features of the RX PHY, like the equalizer, the common-mode voltage and the resistor termination. The registers of block 0180h monitor the status of these controls.

Remark: Most of the main controls (power on/off, PLL clock dividers,etc.) are automatically set while specyfing the LMF mode and/or by the MAIN_CTRL register .



Blocks 0160h/0180h = DAC A/B

Blocks 0360h/0380h = DAC C/D

Blocks 0560h/0580h = All DACs

Fig 54. RX PHY control overview

11.8.1 Lane input

Each lane is Current Mode Logic (CML) compliant.

The common-mode voltage and the termination resistor can be programmed using register HS_RX_RT_VCM_XY and registers HS_RX_LNx_RT_REF_SIZE_XY (0x12 to 0x16). When not used, the lane input buffer can be set to a high impedance mode (register HS_RX_RT_CTRL_XY;).

AC-coupling is always required (see Figure 55).

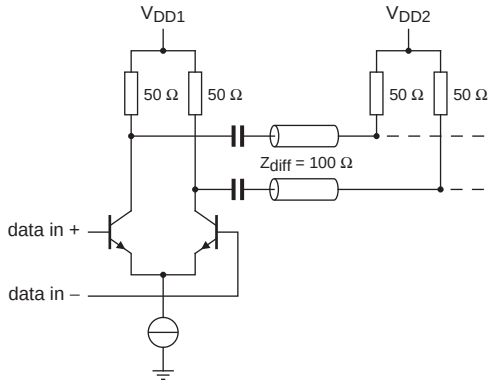


Fig 55. AC-coupling

11.8.2 Equalizer

The DAC165xQ embeds an internal equalizer (bits HS_RX_LNx_EQZ_EN_XY in register HS_RX_EQZ_CTRL_XY) in each high-speed serial lane. This improves the interference robustness between signals by amplifying the high-frequency jumps in the data conserving the energy of the low-frequencies ones. The equalizer can be programmed depending on the quality of the channel used (PCB traces/layout, connectors, etc.).

The auto-zero feature (bit HS_RX_EQZ_AUTO_ZERO_EN_XY in register HS_RX_EQZ_CTRL_XY) is enabled by default for the deserializer to adapt itself to the common-mode of the received signal. This feature can be set manually. It uses an external algorithm that controls the DAC165xQ via the SPI bus.

Set two gains to control the high-frequency and low-frequency jumps of the data (bits HS_RX_LNx_EQ_IF_GAIN_XY[2:0] of register HS_RX_LNx_EQZ_GAIN_XY).

11.8.3 Deserializer

The deserializer performs the incoming data clock recovery and also the serial-to-parallel conversion. One global PLL provides the same reference clock to the four lanes. The PLL configuration is automatically done when specifying the LMF parameters (see Table 10).

When using the DAC165xQ with a low serial input data rate (lower than 1.5 Gbps), it is recommended to enable the low speed mode of the Clock Data Recovery (CDR) unit by setting the HS_RX_CDR_LS_EN_XY bit of register HS_RX_CDR_DIVx_XY .

11.8.4 PHY test mode

A special test mode is available for measurement purposes only. The recovered clock of each CDR unit can be transmitted to the SYNC buffer after a frequency division by 20. This is done by setting bit SYNC_TST_DATA_EN_XY of register SYNC_SEL_CTRL to logic 1 . Bit SYNC_TST_DATA_SEL_XY is used to specify which CDR clock is used.

11.9 Output interfacing configuration

11.9.1 DAC1658Q: High common-mode output voltage

11.9.1.1 Basic output configuration

Using a differentially coupled transformer output provides optimum distortion performance. In addition, it helps to match the impedance and provides electrical isolation.

The DAC1658Q can generate a differential output of 1 V (p-p). In this configuration, connect the center tap of the transformer to a 25 Ω resistor, which is connected to the 3.3 V analog power supply. This adjusts the DC common-mode to around 3.05 V (see Figure 56).

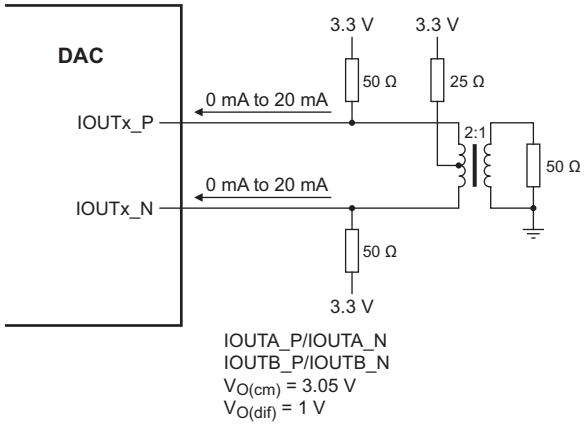
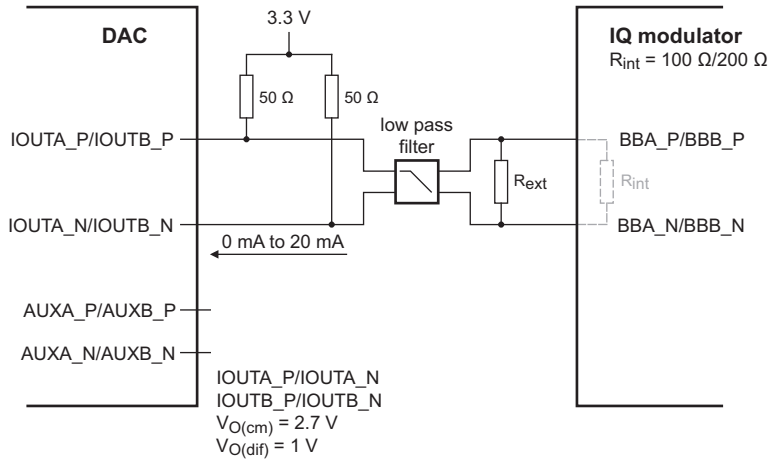


Fig 56. 1 V (p-p) differential output with transformer

11.9.1.2 Low input impedance IQ-modulator interface

The DAC1658Q can be easily connected to low input impedance IQ-modulators. The image of the local oscillator can be canceled using the digital offset control in the device.

Figure 57 shows an example of a connection between the DAC1658Q and a low input impedance modulator.



(1) If R_{int} = 100 Ω, then R_{ext} = not connected

(2) If R_{int} = 200 Ω , then R_{ext} = 200 Ω

Fig 57. DAC1658Q with low input impedance IQ-modulator interface

11.9.1.3 IQ-modulator - DC interface

When the system operation requires to keep the DC component of the spectrum, the DAC1658Q can use a DC interface to connect an IQ-modulator. In this case, the image of the local oscillator can be canceled using the digital offset control in the device.

Figure 58 shows an example of a connection to an IQ modulator with a 1.7 V common input level.

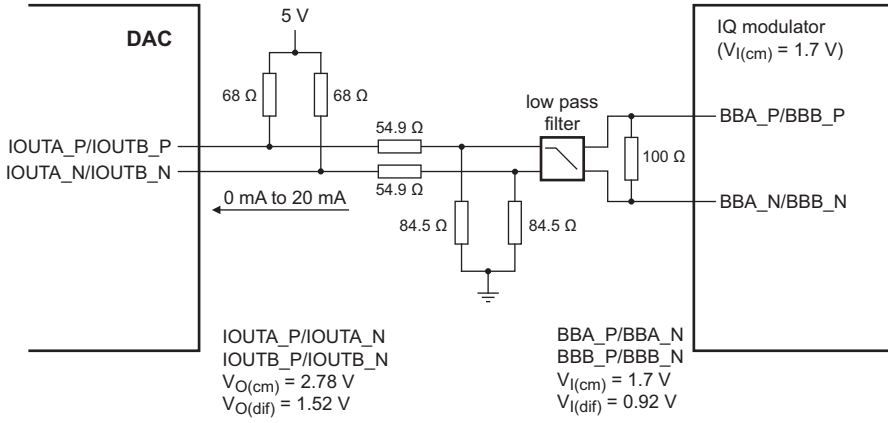


Fig 58. IQ-modulator: DC interface with a 1.7 V common input level

Figure 59 shows an example of a connection to an IQ-modulator with a 3.3 V common input level.

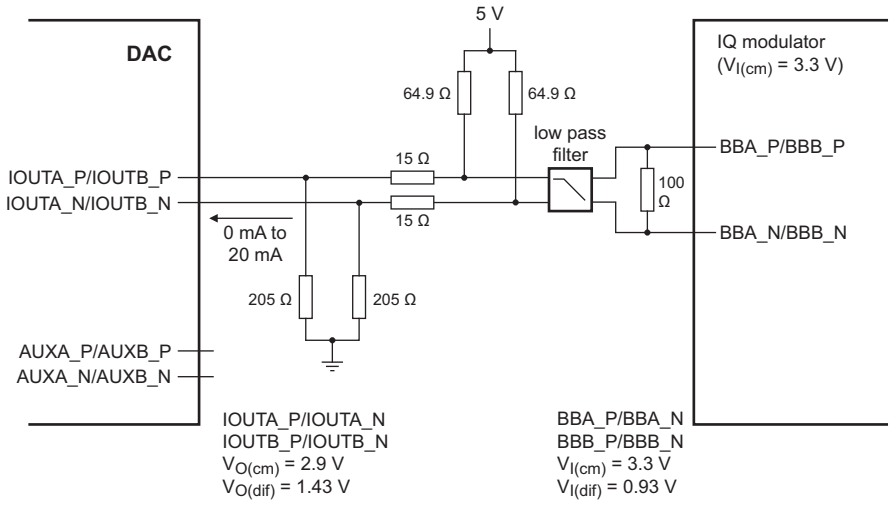


Fig 59. IQ-modulator: DC interface with a 3.3 V common input level

11.9.2 DAC1653Q: Low common-mode output voltage

11.9.2.1 Basic output configuration

Using a differentially coupled transformer output provides optimum distortion performance. In addition, it helps to match the impedance and provides electrical isolation.

The DAC1653Q can generate a differential output of 1 V (p-p). In this configuration, connect the center tap of the transformer to a 25 Ω resistor, which is connected to the GND. This adjusts the DC common-mode to around 0.25 V (see Figure 56).

11.9.2.2 Low input impedance IQ-modulator interface

The DAC1653Q can be easily connected to low input impedance IQ-modulators. The image of the local oscillator can be canceled using the digital offset control in the device.

Figure 57 shows an example of a connection between the DAC1653Q and a low input impedance modulator.

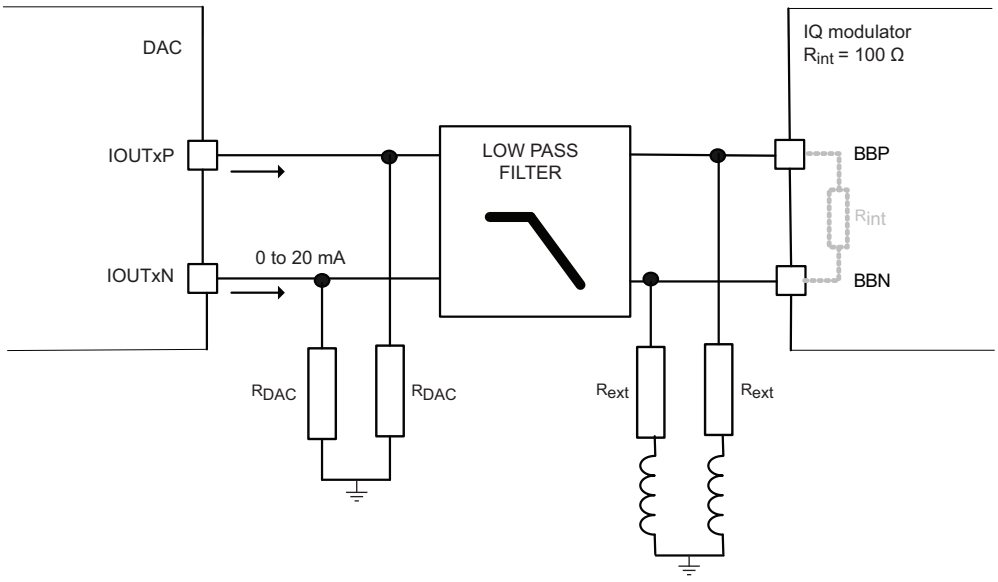


Fig 60. Low input impedance IQ-modulator interface

11.9.2.3 High input impedance IQ-modulator interface

The DAC1653Q can be easily connected to high input impedance IQ-modulators. The image of the local oscillator can be canceled using the digital offset control in the device.

Figure 61 shows an example of a connection between the DAC1653Q and a high input impedance modulator.

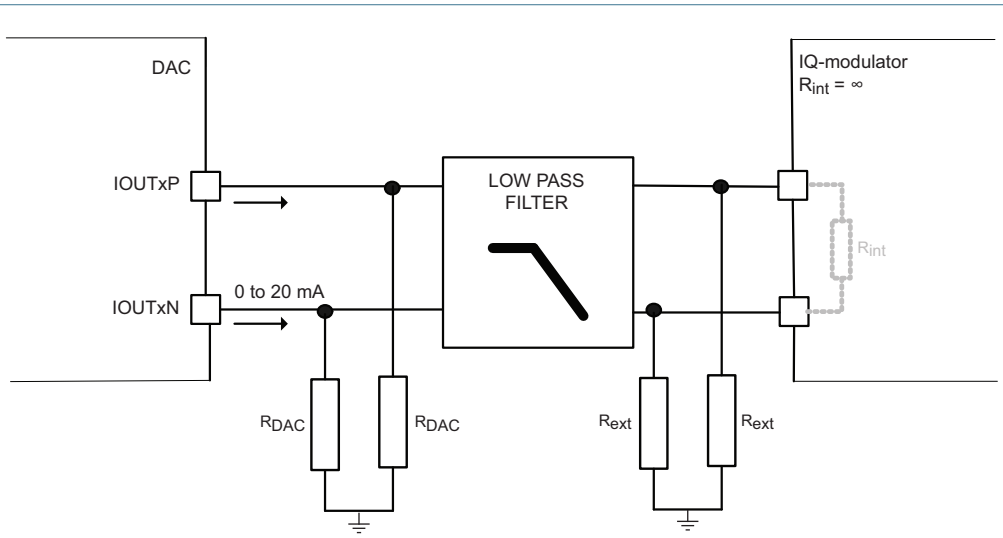


Fig 61. High input impedance IQ-modulator interface

11.10 Design recommendations

11.10.1 Power and grounding

Use a separate power supply regulator for the generation of the 1.2 V analog power (pins 43, 48. 51. 56) and the 1.2 V digital power (pins 7, 10, 33, 36) to ensure optimal performance.

High-speed input lanes are powered by a 1.2 V power supply that can require a dedicated power supply. Pins 15, 16, 19, 22, 25, 28 can be connected to either the global 1.2 V power supply or to a dedicated one.

Also, include individual LC decoupling for the following six sets of power pins:

- $V_{DDA(1V2)}$
  LDO low noise:
  - DAC AB (pins 65, 68, 69, 72)
  - DAC CD (pins 55, 58, 59, 62)
  - BIASING (pins 50, 53)
  - CLOCK (pin 2)
- $V_{DDA(3V3)}$
  LDO low noise:
  - Output AB (pins 1, 64)
  - Output CD (pins 54, 63)
- $V_{DDA(3V3)}$
  LDO low noise:
  - PLL (pin 5)
- $V_{DDD(1V2)}$
  Switch supply:
  - DIGITAL (pins 8, 15, 40, 47)
  - SYNC output (pin 39)
  - JESD204B input (pin 16, 23, 32)
  - IO/SPI (pin 41)

Use at least two capacitors for each power pin decoupling. Locate these capacitors as close as possible to the DAC1658Q power pins.

Use a separate LDO for the generation of the 1.2 V analog power ($V_{DDA(1V2)}$) and the 1.2 V digital power ($V_{DDD(1V2)}$) to ensure the best performance.

The die pad is used for both the power dissipation and electrical grounding. Insert several vias (typically 7 × 7 to connect the internal ground plane to the top layer die area.

12. Package outline

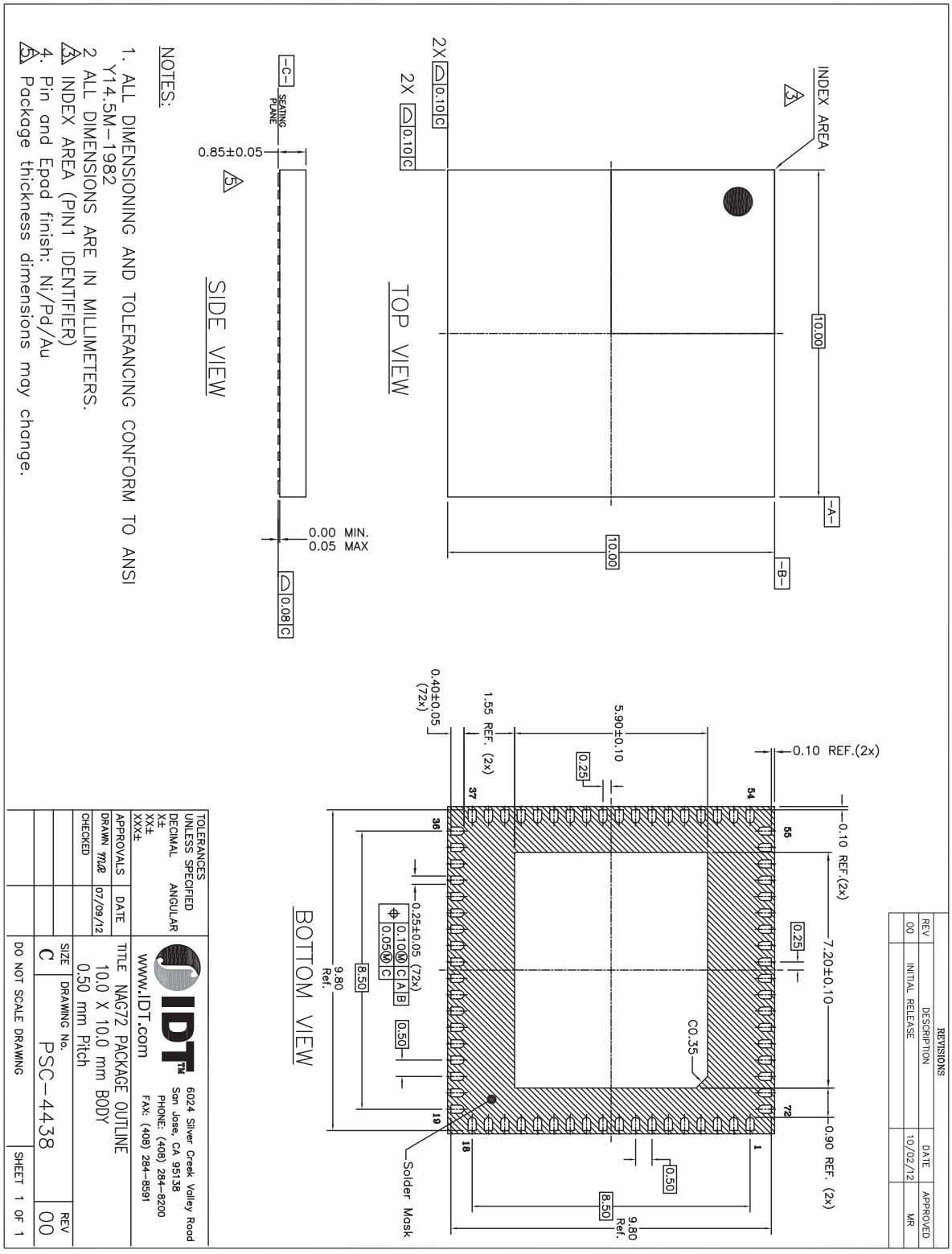


Fig 62. Package outline (QFN72)

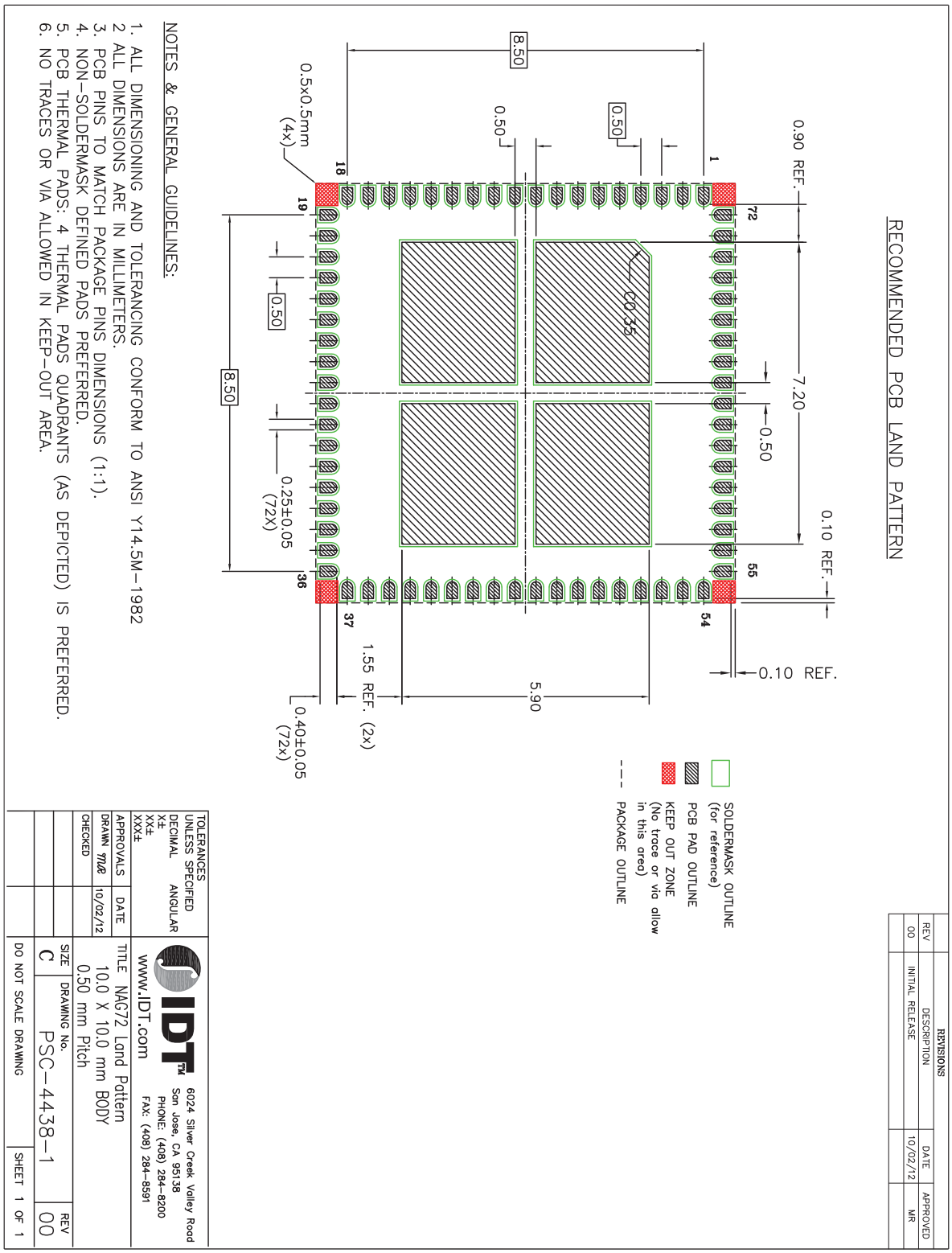


Fig 63. PCB land pattern

13. Abbreviations

Table 39. Abbreviations

Acronym	Description
B	BandWidth
BWA	Broadband Wireless Access
CDI	Clock Domain Interface
CDMA	Code Division Multiple Access
CML	Current Mode Logic
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital-to-Analog Converter
DSP	Digital Signal Processing
EDGE	Enhanced Data rates for GSM Evolution
FIR	Finite Impulse Response
GSM	Global System for Mobile communications
IF	Intermediate Frequency
IMD3	Third Order InterModulation
LMDS	Local Multipoint Distribution Service
LO	Local Oscillator
LVDS	Low-Voltage Differential Signaling
NCO	Numerically Controlled Oscillator
NMOS	Negative Metal-Oxide Semiconductor
PLL	Phase-Locked Loop
SFDR	Spurious-Free Dynamic Range
SPI	Serial Peripheral Interface
WCDMA	Wide band Code Division Multiple Access
WLL	Wireless Local Loop

14. Glossary

14.1 Static parameters

INL — The deviation of the transfer function from a best fit straight line (linear regression computation).

DNL — The difference between the ideal and the measured output value between successive DAC codes.

14.2 Dynamic parameters

Spurious-Free Dynamic Range (SFDR) — The ratio between the RMS value of the reconstructed output sine wave and the RMS value of the largest spurious observed (harmonic and non-harmonic, excluding DC component) in the frequency domain.

InterModulation Distortion (IMD) — From a dual-tone digital input sine wave (these two frequencies being close together), the intermodulation distortion products IMD2 and IMD3 (second order and third order components) are defined below.

IMD2 — The ratio between the RMS value of either tone and the RMS value of the worst second order intermodulation product.

IMD3 — The ratio between the RMS value of either tone and the RMS value of the worst third order intermodulation product.

Total Harmonic Distortion (THD) — The ratio between the RMS value of the harmonics of the output frequency and the RMS value of the output sine wave. Usually, the calculation of THD is done on the first 5 harmonics.

Signal-to-Noise Ratio (SNR) — The ratio between the RMS value of the reconstructed output sine wave and the RMS value of the noise excluding the harmonics and the DC component.

Restricted BandWidth Spurious-Free Dynamic Range ($SFDR_{RBW}$) — the ratio between the RMS value of the reconstructed output sine wave and the RMS value of the noise, including the harmonics, in a given bandwidth centered around f_{offset}.

15. Revision history

Table 40. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
DAC1653Q/ DAC1658Q 1.03	13th, May 2013	Advance data sheet	-	-

16. Tables

continued >>

17. Contents

continued >>

Disclaimer