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1M x 16 SRAM MODULE

SYS161000FKX - 70/85/10/12
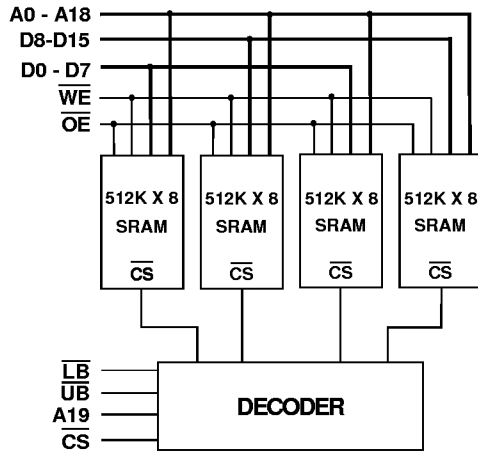
Issue 1.4 : January 1999

Description

The SYS161000FKX is a plastic 16Mbit Static RAM Module in a 44 pin DIP package. The module utilises four 512Kx8 SRAMs housed in TSOPII packages, surface mounted onto an FR4 epoxy substrate. The RAMs are organised as two banks of 512Kx16 each. The upper address line is used to select one of the two banks, and using $\overline{LB}$ and $\overline{UB}$ as two extra chip select functions for Lower Byte and Upper Byte control, respectively.

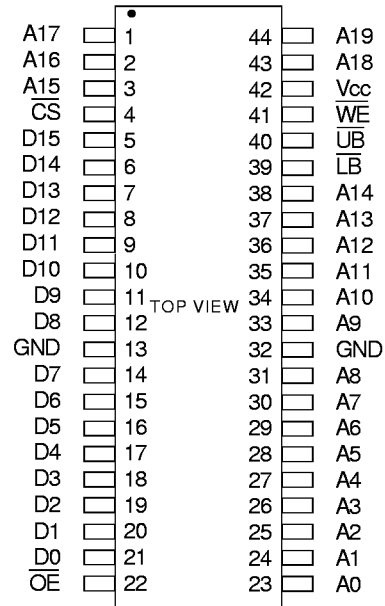The module is completely asynchronous, static design requiring no clocks or refreshing.

Features

- Access Times of 70/85/100/120 ns.
- 44 pin DIL Package.
- 5 Volt Supply ± 10%
- Power Dissipation:
  Operating   1.20   W (Max.)
  Standby -L Version (CMOS)   2.64 mW (Max.)
- Completely Static Operation.
- Low Voltage V_{CC} Data Retention.
- On-board Supply Decoupling Capacitors.
- Provides upgrade from JEDEC Standard 64Kx16 40 pin modules..

Block Diagram

A0 - A18
D8-D15
D0 - D7
$\overline{WE}$
$\overline{OE}$

| 512K X 8 SRAM $\overline{CS}$ | 512K X 8 SRAM $\overline{CS}$ | 512K X 8 SRAM $\overline{CS}$ | 512K X 8 SRAM $\overline{CS}$ |

$\overline{LB}$
$\overline{UB}$
A19
$\overline{CS}$
DECODER

Pin Functions

Address Inputs	A0 - A19
Data Input/Output	D0 - D15
Chip Select	$\overline{CS}$
Write Enable	$\overline{WE}$
Lower Byte Enable	$\overline{LB}$
Upper Byte Enable	$\overline{UB}$
Output Enable	$\overline{OE}$
Power (+5V)	V_{cc}
Ground	GND

Pin Definition

A17	1		44	A19
A16	2		43	A18
A15	3		42	Vcc
$\overline{CS}$	4		41	$\overline{WE}$
D15	5		40	$\overline{UB}$
D14	6		39	$\overline{LB}$
D13	7		38	A14
D12	8		37	A13
D11	9		36	A12
D10	10		35	A11
D9	11	TOP VIEW	34	A10
D8	12		33	A9
GND	13		32	GND
D7	14		31	A8
D6	15		30	A7
D5	16		29	A6
D4	17		28	A5
D3	18		27	A4
D2	19		26	A3
D1	20		25	A2
D0	21		24	A1
$\overline{OE}$	22		23	A0

Package Details

Plastic 44 Pin Dual-In-Line (DIP)

DC OPERATING CONDITIONS

Absolute Maximum Ratings [1]

Parameter	Symbol	Min	Typ	Max	Unit
Voltage on any pin relative to V_{SS}	V_T [2]	-0.3	-	7.0	V
Power Dissipation	P_T	-	-	2.0	W
Storage Temperature	T_{STG}	-55	-	125	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) V_T can be -3.0V pulse of less than 30ns.

Recommended Operating Conditions

Parameter		Symbol	Min	Typ	Max	Unit
Supply Voltage		V_{CC}	4.5	5.0	5.5	V
Input High Voltage		V_{IH}	2.2	-	V_{CC}+0.3	V
Input Low Voltage		V_{IL}	-0.3	-	0.8	V
Operating Temperature	(Commercial)	T_A	0	-	70	°C
	(Industrial)	T_{AI}	-40	-	85	°C

DC Electrical Characteristics (V_{CC}=5V±10%) TA 0 to 70 °C

Parameter		Symbol	Test Condition	Min	Typ	max	Unit
I/P Leakage Current	Address,$\overline{OE}$,$\overline{WE}$	I_{LI}	$0V \leq V_{IN} \leq V_{CC}$	-4	-	4	µA
Output Leakage Current		I_{LO}	$\overline{CS} = V_{IH}$, $V_{I/O}$ = GND to V_{CC}	-2	-	2	µA
Operating Supply Current	16-bit mode	I_{CC1}	Min. Cycle, $\overline{CS} = V_{IL}$, $V_{IL} \leq V_{IN} \leq V_{IH}$	-	-	215	mA
Standby Supply Current	TTL levels	I_{SB1}	$\overline{CS} = V_{IH}$	-	-	20	mA
	CMOS levels	I_{SB2}	$\overline{CS} \geq V_{CC}$-0.2V, $0.2 \leq V_{IN} \leq V_{CC}$-0.2V	-	-	8	mA
	-L Version (CMOS)	I_{SB3}	$\overline{CS} \geq V_{CC}$-0.2V, $0.2 \leq V_{IN} \leq V_{CC}$-0.2V	-	-	480	mA
Output Voltage		V_{OL}	$I_{OL} = 8.0mA$	-	-	0.4	V
		V_{OH}	$I_{OH} = -4.0mA$	2.4	-	-	V

Typical values are at V_{CC}=5.0V, T_A=25°C and specified loading.

Capacitance (V_{CC}=5V±10%, T_A=25°C) Note: Capacitance calculated, not measured.

Parameter	Symbol	Test Condition	max	Unit
Input Capacitance (Address,$\overline{OE}$,$\overline{WE}$)	C_{IN1}	$V_{IN} = 0V$	48	pF
I/P Capacitance (other)	C_{IN2}	$V_{IN} = 0V$	12	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	24	pF

AC Test Conditions   Output Load

* Input pulse levels: 0V to 3.0V
* Input rise and fall times: 5ns
* Input and Output timing reference levels: 1.5V
* Output load: see diagram
* V_{CC}=5V±10%

I/O Pin   645Ω
                1.76V
        100pF
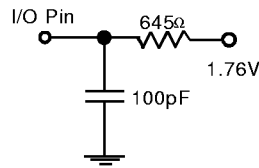
Operation Truth Table

$\overline{CS}$	$\overline{UB}$	$\overline{LB}$	$\overline{OE}$	$\overline{WE}$	DATA PINS	SUPPLY CURRENT	MODE
H	X	X	X	X	High Impedance	I_{SB1} , I_{SB2} , I_{SB3} , I_{SB4}	Standby
L	H	H	X	X	High Impedance	I_{SB1} , I_{SB2} , I_{SB3} , I_{SB4}	Standby
L	L	L	L	L	D_{0-15} IN	I_{CC1} / 2	Write
L	L	L	L	H	D_{0-15} OUT	I_{CC1} / 2	Read
L	L	L	H	L	D_{0-15} IN	I_{CC1} / 2	Write
L	L	L	H	H	High-Impedance	I_{CC1}	High-Z
L	H	L	L	L	D_{0-7} IN	I_{CC1} / 2	Write LB
L	H	L	L	H	D_{0-7} OUT	I_{CC1} / 2	Read LB
L	H	L	H	L	D_{0-7} IN	I_{CC1} / 2	Write LB
L	H	L	H	H	High-Impedance	I_{CC1} / 2	High-Z
L	L	H	L	L	D_{8-15} IN	I_{CC1} / 2	Write UB
L	L	H	L	H	D_{8-15} OUT	I_{CC1} / 2	Read UB
L	L	H	H	L	D_{8-15} IN	I_{CC1} / 2	Write UB
L	L	H	H	H	High-Impedance	I_{CC1} / 2	High-Z

Notes : H = V_{IH} : L =V_{IL} : X = V_{IH} or V_{IL}

Low V_{CC} Data Retention Characteristics - L & P Version's Only.

Parameter	Symbol	Test Condition	min	typ[1]	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$-0.2V	2.0	-	-	V
Data Retention Current -L Version	I_{CCDR1} [2]	V_{CC}=3.0V, $V_{IN} \geq 0$, $\overline{CS} \geq V_{CC}$-0.2V	-		280	mA
CS High to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	5	-	-	ms

Notes   (1) Typical figures are measured at 25°C.
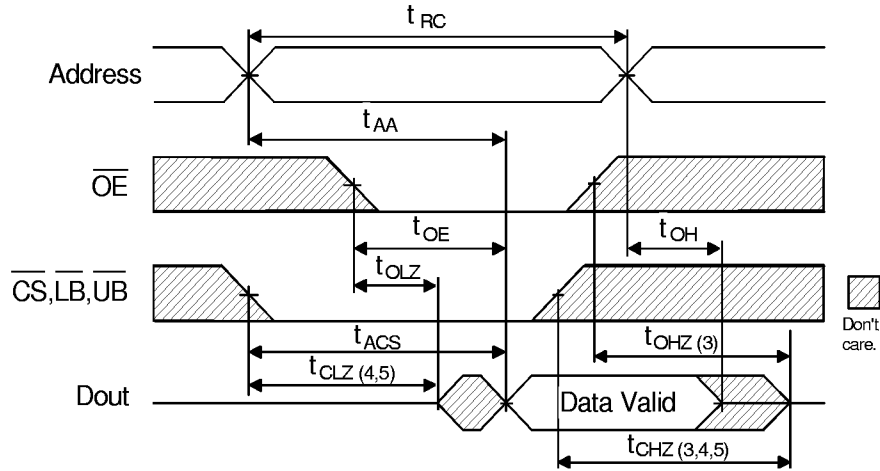   (2) This parameter is guaranteed not tested.

AC OPERATING CONDITIONS

Read Cycle

Parameter	Symbol	-70 min	-70 max	-85 min	-85 max	-10 min	-10 max	-12 min	-12 max	Unit
Read Cycle Time	t_{RC}	70	-	85	-	100	-	120	-	ns
Address Access Time	t_{AA}	-	70	-	85	-	100	-	120	ns
$\overline{CS}$, $\overline{LB}$, $\overline{UB}$ Access Time	t_{ACS}	-	70	-	85	-	100	-	120	ns
Output Enable to Output Valid	t_{OE}	-	35	-	45	-	50	-	55	ns
Output Hold from Address Change	t_{OH}	10	-	10	-	10	-	10	-	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	-	10	-	10	-	10	-	ns
Output Enable to Output in Low Z	t_{OLZ}	5	-	5	-	5	-	5	-	ns
Chip Deselection to O/P in High Z	t_{CHZ}	0	30	0	35	0	40	0	45	ns
Output Disable to Output in High Z	t_{OHZ}	0	25	0	30	0	35	0	40	ns

Write Cycle

Parameter	Symbol	-70 min	-70 max	-85 min	-85 max	-10 min	-10 max	-12 min	-12 max	Unit
Write Cycle Time	t_{WC}	70	-	85	-	100	-	120	-	ns
$\overline{CS}$, $\overline{LB}$, $\overline{UB}$ to End of Write	t_{CW}	60	-	75	-	80	-	90	-	ns
Address Valid to End of Write	t_{AW}	60	-	75	-	80	-	90	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	50	-	55	-	70	-	80	-	ns
Write Recovery Time	t_{WR}	5	-	5	-	5	-	5	-	ns
Write to Output in High Z	t_{WHZ}	0	30	0	30	0	35	0	40	ns
Data to Write Time Overlap	t_{DW}	30	-	35	-	40	-	45	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	0	-	ns
Output active from end of write	t_{OW}	5	-	5	-	5	-	5	-	ns

Read Cycle Timing Waveform [1,2]

Address t_{RC}

$\overline{OE}$ t_{AA}

t_{OE} t_{OH}

$\overline{CS}, \overline{LB}, \overline{UB}$ t_{OLZ}

Don't care.

t_{ACS} $t_{OHZ(3)}$

$t_{CLZ(4,5)}$

Dout   Data Valid

$t_{CHZ(3,4,5)}$

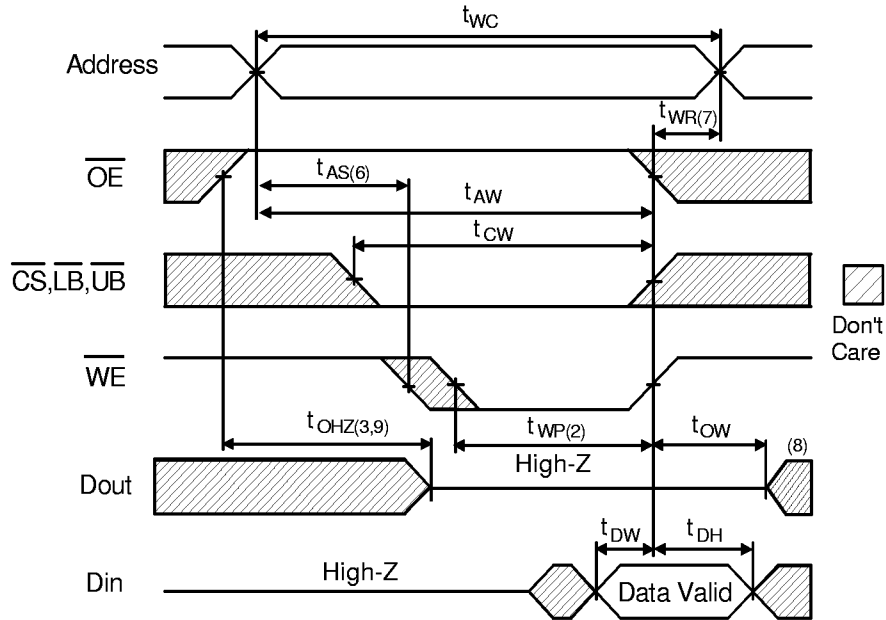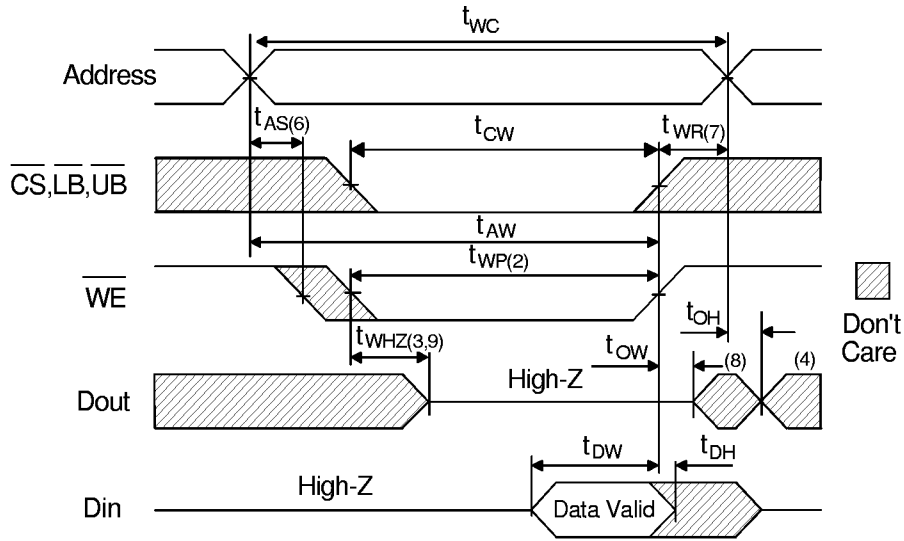### AC Read Characteristics Notes

(1) $\overline{WE}$ is High for Read Cycle.

(2) All read cycle timing is referenced from the last valid address to the first transition address.

(3) t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels.

(4) At any given temperature and voltage condition, t_{CHZ} (max) is less than t_{CLZ} (min) both for a given module and from module to module.

(5) These parameters are sampled and not 100% tested.

Write Cycle No.1 Timing Waveform [1,4]

Address t_{WC}

$t_{WR(7)}$

$\overline{OE}$ $t_{AS(6)}$ t_{AW}

t_{CW}

$\overline{CS}, \overline{LB}, \overline{UB}$

Don't Care

$\overline{WE}$

$t_{OHZ(3,9)}$ $t_{WP(2)}$ t_{OW} (8)

High-Z

Dout

t_{DW} t_{DH}

Din   High-Z   Data Valid

## Write Cycle No.2 Timing Waveform [1,5]

AC Write Characteristics Notes

(1) All write cycle timing is referenced from the last valid address to the first transition address.

(2) All writes occur during the overlap of $\overline{CS}/\overline{LB}/\overline{UB}$ and $\overline{WE}$ low.

(3) If $\overline{OE}$, $\overline{CS}/\overline{LB}/\overline{UB}$, and $\overline{WE}$ are in the Read mode during this period, the I/O pins are low impedance state. Inputs of opposite phase to the output must not be applied because bus contention can occur.

(4) Dout is the Read data of the new address.

(5) $\overline{OE}$ is continuously low.

(6) Address is valid prior to or coincident with $\overline{CS}/\overline{LB}/\overline{UB}$ and $\overline{WE}$ low, too avoid inadvertant writes.

(7) $\overline{CS}/\overline{LB}/\overline{UB}$ or $\overline{WE}$ must be high during address transitions.

(8) When $\overline{CS}/\overline{LB}/\overline{UB}$ is low : I/O pins are in the output state. Input signals of opposite phase leading to the output should not be applied.

(9) Defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.
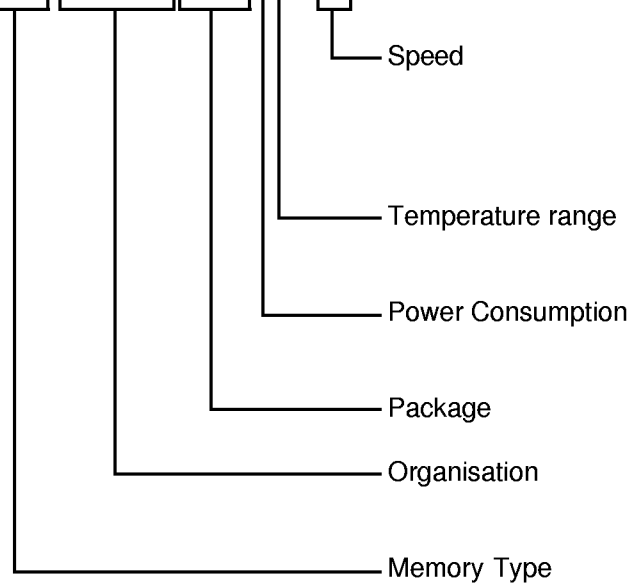
Data Retention Waveform
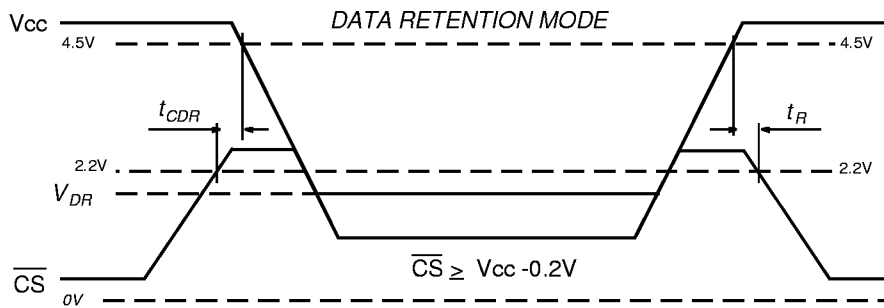
Package Information   Dimensions in mm

Plastic 44 Pin 0.6" Dual-In-Line (DIP)
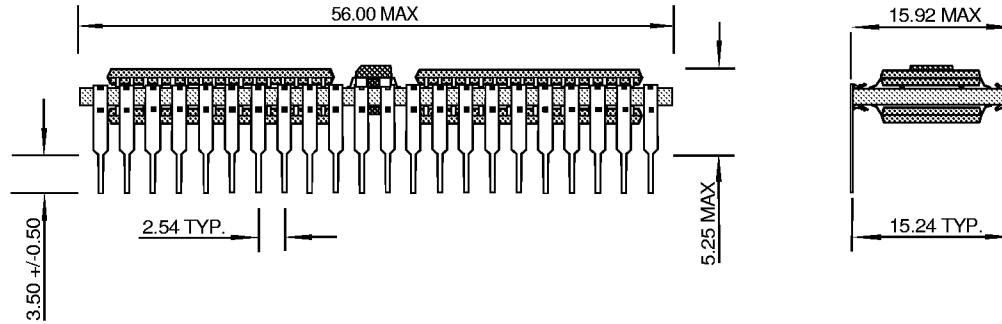
Ordering Information

SYS161000FKXLI - 70

— Speed   70 = 70 ns
                           85 = 85 ns
                           10 = 100 ns
                           12 = 120 ns

— Temperature range   Blank = Commercial Temp.
                              I = Industrial Temp.

— Power Consumption   Blank = Standard Part
                              L = Low Power Part

— Package   FKX = Plastic 44 Pin DIP

— Organisation   161000 = 1M x 16

— Memory Type   SYS = Static RAM

Note :
 Although this data is believed to be accurate the information contained herein is not intended to and does not create
any warranty of merchantibility or fitness for a particular purpose.
 Our products are subject to a constant process of development. Data may be changed at any time without notice.
 Products are not authorised for use as critical components in life support devices without the express written approval
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