Integrated Device Technology, Inc.

128KB/256KB/512KB SECONDARY CACHE MODULES FOR THE INTEL® i486™ CPU/82420TX PCI SET

PRELIMINARY
IDT7MP6133
IDT7MP6134
IDT7MP6135
IDT7MP6151
IDT7MP6152
IDT7MP6153

FEATURES

- 128KB/256KB/512KB secondary cache module family
- Ideal for use with Intel i486 CPU-based systems that use the Intel 82420TX PCIset core logic
- Operates with external i486 processor speeds of 33MHz
- Supports 128MB of cacheable memory
- Low cost low profile cardedge module with 112 leads
- Uses Burndy Computerbus™ connector, part number CELP2X56SC3Z48
- Presence detect pins map directly into 82424TX CDC
- Single 5V (±5%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity

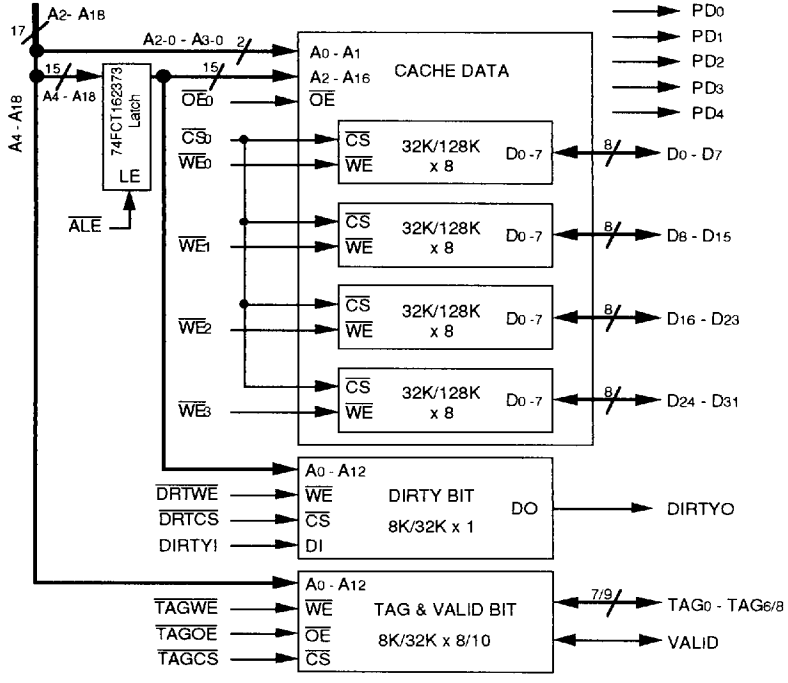
DESCRIPTION

The IDT7MP6133/34/35 and IDT7MP6151/52/53 are members of a family of low-cost secondary caches that are ideal for use with Intel i486 CPU-based systems using the Intel 82420TX PCIset core logic. The IDT7MP6133/34/35 and IDT7MP6151/52/53 use IDT's asynchronous SRAMs and one IDT74FCT162373 balanced drive Double-Density™ latch in plastic surface mount packages mounted on a multilayer epoxy laminate (FR-4) board. High speeds are achieved using IDT's high-performance, high-reliability CMOS technology.

The low-profile cardedge package configuration allows 112 signal leads to be placed on a package 3.15" long. Depending on which cache configuration is used, the module is a maximum of 0.365" thick and a maximum of 1.2" tall.

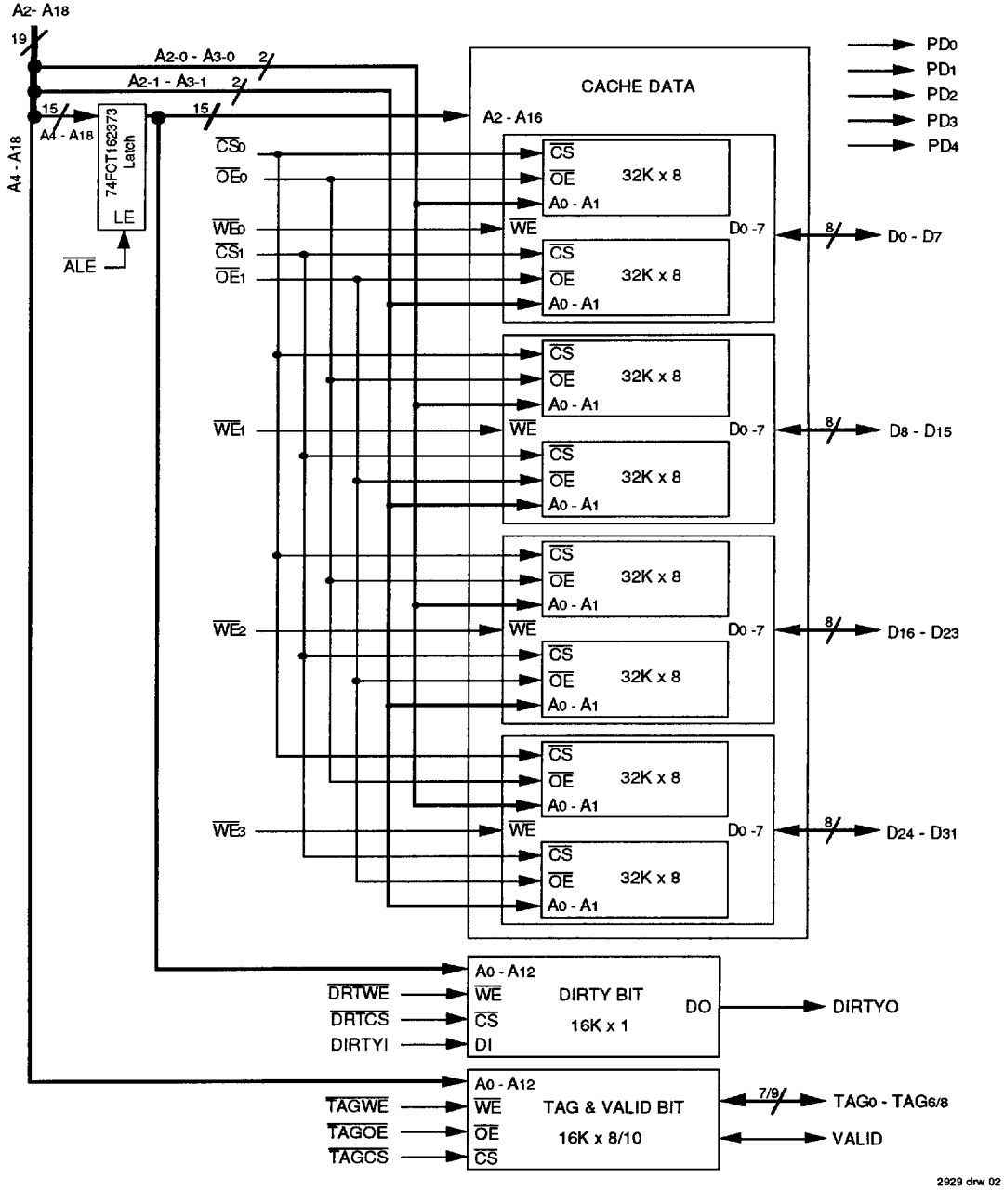
The IDT7MP6133/34/35 and IDT7MP6151/52/53 operate from single 5V power supply. Multiple GND pins and on-board decoupling capacitors ensure maximum protection from noise.

FUNCTIONAL BLOCK DIAGRAM
IDT7MP6133/51 AND IDT7MP6135/53 – 128KB/512KB VERSIONS



2929 drw 01

FUNCTIONAL BLOCK DIAGRAM
IDT7MP6134/52 – 256KB VERSIONS



PIN CONFIGURATION

GND	57	1	GND
D0	58	2	D1
D2	59	3	D3
D4	60	4	D5
D6	61	5	D7
VCC	62	6	VCC
(2) N.C.	63	7	N.C.(2)
D8	64	8	D9
D10	65	9	D11
D12	66	10	D13
GND	67	11	GND
D14	68	12	D15
D16	69	13	D17
D18	70	14	D19
D20	71	15	D21
VCC	72	16	VCC
D22	73	17	D23
(2) N.C	74	18	N.C.(2)
D24	75	19	D25
D26	76	20	D27
GND	77	21	GND
D28	78	22	D29
D30	79	23	D31
A2-0	80	24	A2-1(1)
A3-0	81	25	A3-1(1)
VCC	82	26	VCC
A4	83	27	A5
A6	84	28	A7
A8	85	29	A9
A10	86	30	A11
A12	87	31	A13
A14	88	32	A15
A16	89	33	A17
A18	90	34	N.C.
GND	91	35	GND
DIRTYI	92	36	DIRTYO
TAG0	93	37	TAG1
TAG2	94	38	TAG3
TAG4	95	39	TAG5
GND	96	40	GND
TAG6	97	41	TAG7(3)
VALID	98	42	TAG8(3)
$\overline{TAGCS}$	99	43	$\overline{ALE}$
$\overline{TAGWE}$	100	44	$\overline{WE0}$
VCC	101	45	VCC
GND	102	46	GND
$\overline{TAGOE}$	103	47	$\overline{WE1}$
$\overline{DIRTYWE}$	104	48	$\overline{WE2}$
$\overline{DIRTYCS}$	105	49	$\overline{WE3}$
VCC	106	50	VCC
$\overline{OE0}$	107	51	$\overline{OE1}$(1)
$\overline{CS0}$	108	52	$\overline{CS1}$(1)
PD0	109	53	PD1
PD2	110	54	PD3
PD4	111	55	N C.
GND	112	56	GND

LOW PROFILE CARDEDGE MODULE
TOP VIEW

NOTES: 2929 drw 03
1 These pins are N.C. (no connect) on the IDT7MP6133, IDT7MP6135, IDT7MP6151 and IDT7MP6153 modules
2. Please consult the factory regarding the IDT7MP6164 and IDT7MP6165 module versions that support parity
3 These pins are N C (no connect) on the IDT7MP6133, IDT7MP6134 and IDT7MP6135 modules

PIN NAMES

A4 – A18	Address Inputs
A2-0 – A3-0	Lower Order Bank 0 Address Inputs
A2-1 – A3-1	Lower Order Bank 1 Address Inputs
D0 – D31	Cache Data Inputs/Outputs
$\overline{CS0}$	Bank 0 Chip Select Input
$\overline{CS1}$	Bank 1 Chip Select Input (256KB only)
$\overline{WE0}$ – $\overline{WE3}$	Byte Write Enable Inputs
$\overline{OE0}$	Bank 0 Output Enable Input
$\overline{OE1}$	Bank 1 Output Enable Input (256KB only)
$\overline{ALE}$	Address Latch Enable Input
TAG0 – TAG8	Tag Data Inputs/Outputs
VALID	Valid Bit Input/Output
$\overline{TAGWE}$	Tag and Valid Bit Write Enable Input
$\overline{TAGOE}$	Tag and Valid Bit Output Enable Input
$\overline{TAGCS}$	Tag and Valid Bit Chip Select Input
DIRTYI	Dirty Bit Input
DIRTYO	Dirty Bit Output
$\overline{DRTCS}$	Dirty Bit Chip Select Input
$\overline{DRTWE}$	Dirty Bit Write Enable Input
PD0 – PD4	Presence Detect Pins
N C	No Connect
GND	Ground
VCC	Power Supply

2929 tbl 01

PRESENCE DETECT TABLE(1)

PD4	PD3	PD2	PD1	PD0	Size	Max(2)	Module
N C	N C.	N C.	N C.	N C.	—	—	no cache present
Vcc	Vcc	N C	N C	N C	64KB	8MB	—
Vcc	Vcc	N C	N C	Vcc	128KB	16MB	IDT7MP6133
Vcc	Vcc	N C	Vcc	N C	256KB	32MB	IDT7MP6134
Vcc	Vcc	N C	Vcc	Vcc	512KB	64MB	IDT7MP6135
Vcc	N C	Vcc	N C	N C	64KB	32MB	—
Vcc	N.C.	Vcc	N C	Vcc	128KB	64MB	IDT7MP6151
Vcc	N C	Vcc	Vcc	N C	256KB	128MB	IDT7MP6152
Vcc	N C	Vcc	Vcc	Vcc	512KB	128MB(3)	IDT7MP6153

NOTES: 2929 tbl 02
1 Pins PD4 - PD0 map directly to the 82424TX CDC Secondary Cache Control Register bits
PD4 – CP (cache present)
PD3, PD2 – TAW (tag address width)
PD1 PD0 – SCS (secondary cache size)
2 Maximum cacheable address space based on a 7-or 9-bit tag field
3 The maximum cacheable address space allowed by the core logic is 128MB

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V

2929 tbl 03

CAPACITANCE(1, 2)

(T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Condition	Module(3)	Unit
C_{IN1}	Input Capacitance ($\overline{ALE}$, DIRTYI, Dirty Control)	V_{IN} = 0V	12	pF
C_{IN2}	Input Capacitance ($\overline{WE}$)	V_{IN} = 0V	12/22/12	pF
C_{IN3}	Input Capacitance (A_4 - A_{18}, Tag Control)	V_{IN} = 0V	12(4)	pF
C_{IN4}	Input Capacitance($\overline{CS}$, $\overline{OE}$, A_2 - A_3)	V_{IN} = 0V	50	pF
$C_{I/O1}$	Data I/O Capacitance	V_{OUT} = 0V	14/25/14	pF
$C_{I/O2}$	Tag I/O Capacitance	V_{OUT} = 0V	12	pF
C_O	Output Capacitance	V_{OUT} = 0V	12	pF

2929 tbl 04

NOTES:
1. These parameters are guaranteed by design but not tested
2. These parameters are maximum values.
3. The module specifications are for either 128K/256KB/512KB versions respectively or all versions if the specification is a single number
4. For the IDT7MP6151/52/53 modules, the specification is 22pF

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

2929 tbl 05

NOTE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(1)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.75	5.0	5 25	V
GND	Supply Voltage	0	0	0 0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

2929 tbl 06

NOTE:
1 V_{IL} = –3 0V for pulse width less than 5ns.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, T_A = 0°C to 70°C)

Symbol	Parameter	Test Condition	Module Min.	Module Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max, V_{IN} = GND to V_{CC}	—	20	µA
$\|I_{LI}\|$	Input Leakage Current ($\overline{CS}$, $\overline{OE}$. A_2 - A_3)	V_{CC} = Max, V_{IN} = GND to V_{CC}	—	40	µA
$\|I_{LO}\|$	Output Leakage Current	V_{OUT} = 0V to V_{CC}, V_{CC} = Max., $\overline{CS} \geq V_{IH}$	—	20	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min	—	0 4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V
I_{CC}	Operating Power Supply Current	V_{CC} = Max , $\overline{CS} \leq V_{IL}$, f = f_{MAX}, Outputs Open	—	995(1) 1140(2)	mA
I_{SB}	Standby Supply Current	V_{CC} = Max , $\overline{CS} \geq V_{IH}$, f = f_{MAX}, Outputs Open	—	405(1) 445(2)	mA
I_{SB1}	Full Standby Supply Current	V_{CC} = Max , $\overline{CS} \geq V_{CC}$ – 0 2V, f =0, $V_{IN} > V_{CC}$ – 0.2V or < 0.2V	—	185(1) 205(2)	mA

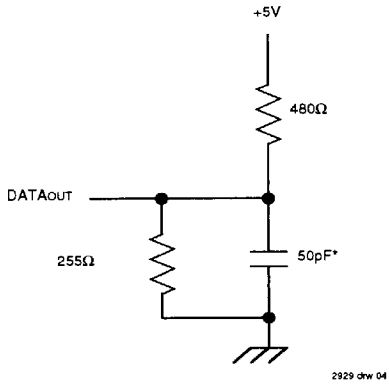
2929 tbl 07

NOTES:
1 This specification is for the IDT7MP6133/34/35 modules
2. This specification is for the IDT7MP6151/52/53 modules.

AC TEST CONDITIONS

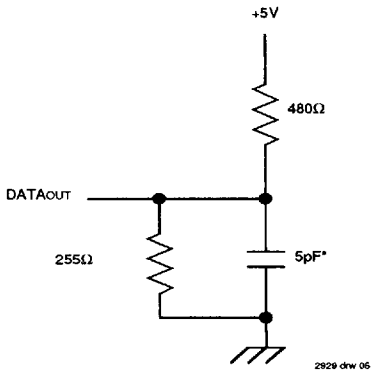
Input Pulse Levels	GND to 3 0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1 5V
Output Reference Levels	1 5V
Output Load	See Figures 1 and 2

2929 tbl 08



*including scope and jig capacitances

Figure 1. Output Load



*including scope and jig capacitances

Figure 2. Output Load (for tOHZ, tCHZ, tOLZ and tCLZ)

AC ELECTRICAL CHARACTERISTICS

(VCC = 5.0V ± 5%, TA = 0°C to 70°C)

		7MP6133/34/35S33M and IDT7MP6151/52/53S33M						
		Data		Tag		Dirty		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle								
tRC	Read Cycle Time	30	—	30	—	30	—	ns
tAA A2 - A3	Address Access Time	—	18	—	—	—	—	ns
tAA A4 - A16[3]	Address Access Time	—	30	—	12[2]	—	28	ns
tACS	Chip Select Access Time	—	18	—	12	—	30	ns
tOE	Output Enable to Output Valid	—	15	—	10	—	—	ns
tCHZ[1]	Chip Deselect to Output in High-Z	—	15	—	10	—	15	ns
tOHZ[1]	Output Disable to Output in High-Z	—	15	—	10	—	—	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
Write Cycle								
tWC	Write Cycle Time	30	—	30	—	30	—	ns
tWP	Write Pulse Width	13	—	13	—	13	—	ns
tDS	Data Setup to Write Time	11	—	13	—	13	—	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	ns
tCW	Chip Select to End-of-Write	20	—	20	—	20	—	ns
tAW A4 - A16	Address Valid to End-of-Write	23	—	20	—	23	—	ns
tAS A2 - A3	Address Set-up Time	2	—	—	—	—	—	ns
tAS A4 - A16	Address Set-up Time	10	—	2	—	10	—	ns

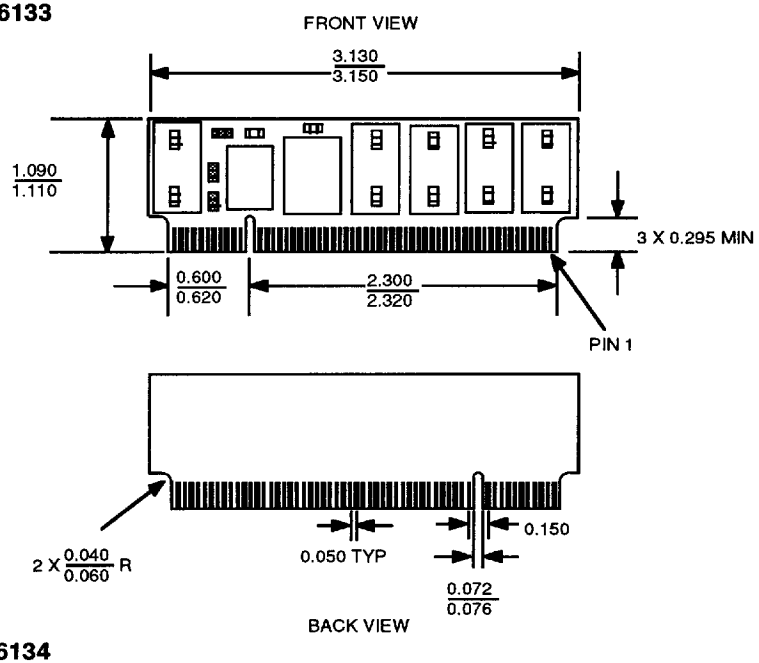
NOTES:

2929 tbl 09

1 This parameter is guaranteed by design, but not tested
2. Module supports i486DX2 CPU For support for i486SX/DX support, please consult the factory
3 This parameter is for the condition when $\overline{ALE}$ is high

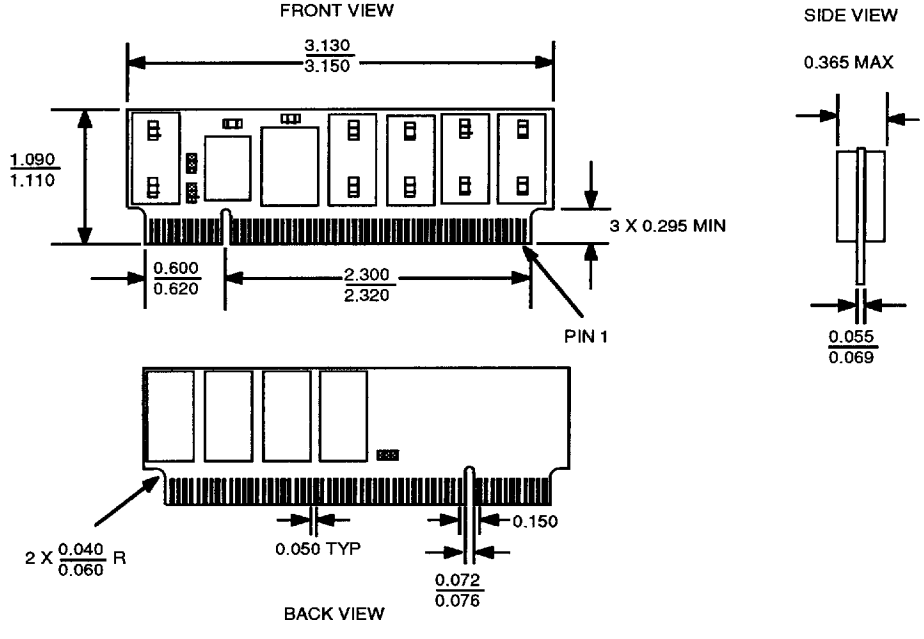
PACKAGE DIMENSIONS

IDT7MP6133



2929 drw 06

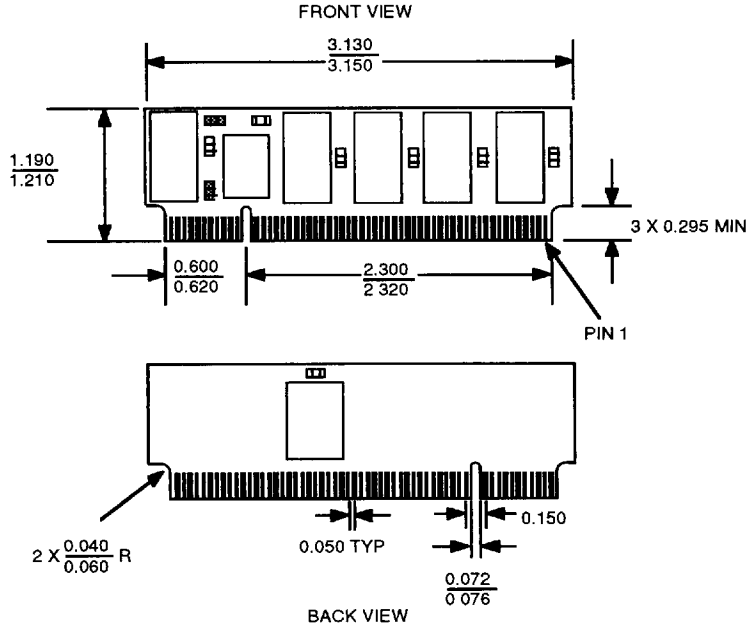
IDT7MP6134



2929 drw 07

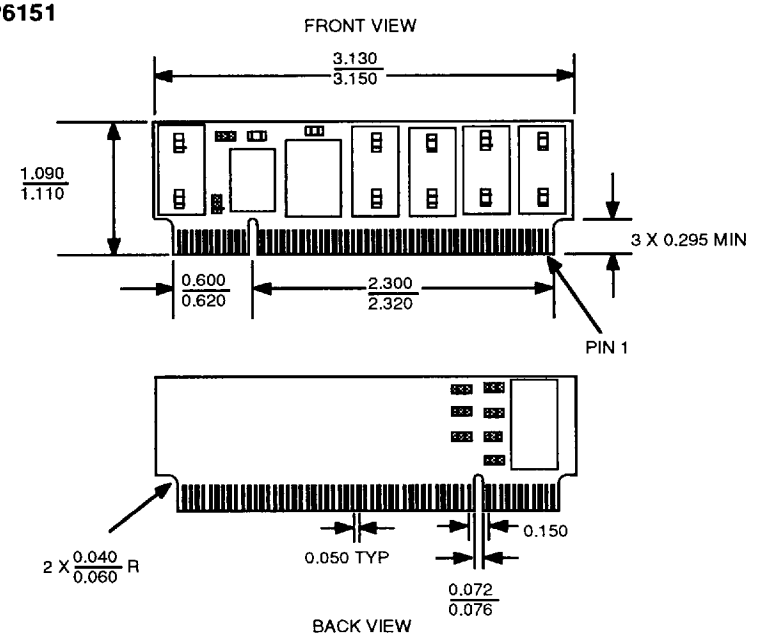
PACKAGE DIMENSIONS

IDT7MP6135



2929 drw 08

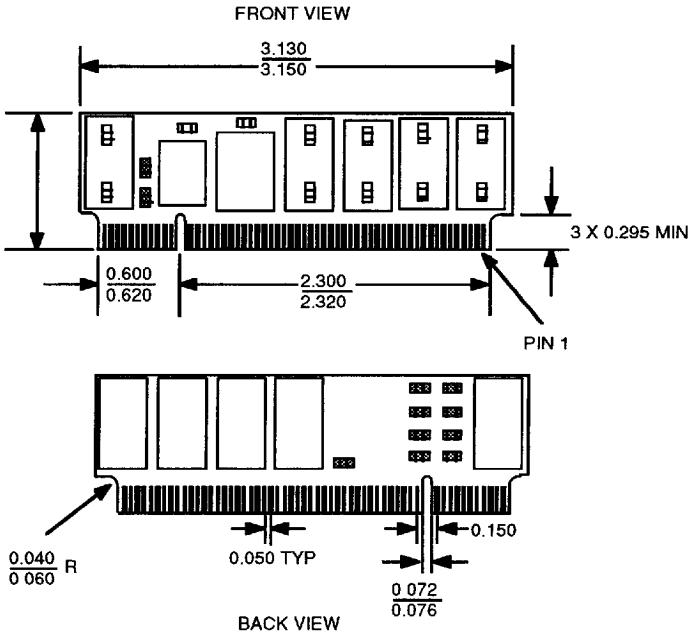
IDT7MP6151



2929 drw 09

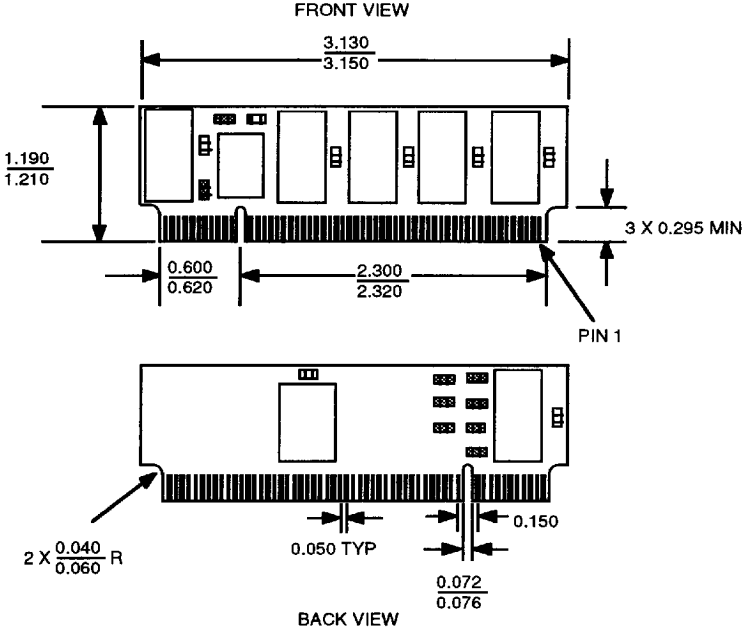
PACKAGE DIMENSIONS

IDT7MP6152



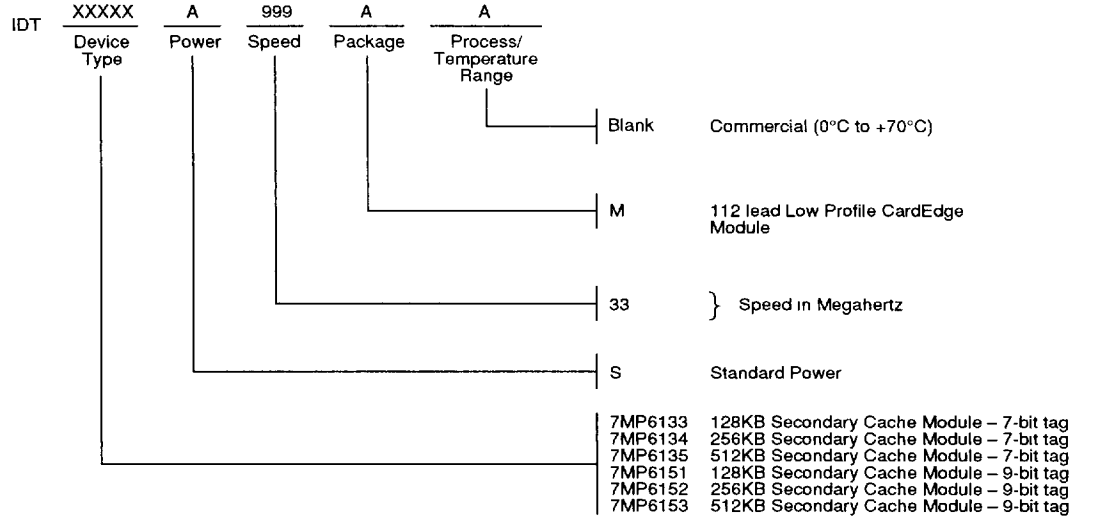
2929 drw 10

IDT7MP6153



2929 drw 11

ORDERING INFORMATION



2929 drw 12