TRIPLE 3-INPUT NOR GATE

The HEF4025B provides the positive triple 3-input NOR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.
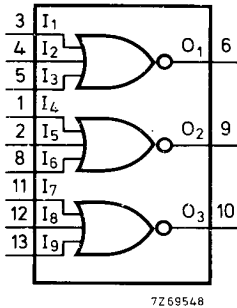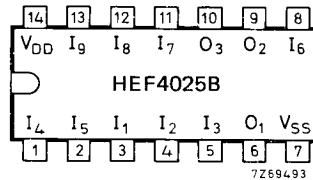

Fig. 1 Functional diagram.

Fig. 2 Pinning diagram.

HEF4025BP : 14-lead DIL; plastic (SOT-27).
HEF4025BD : 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4025BT : 14-lead mini-pack; plastic
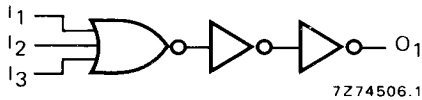(SO-14; SOT-108A).

Fig. 3 Logic diagram (one gate).

FAMILY DATA ⎫
⎬ see Family Specifications
I_{DD} **LIMITS category GATES** ⎭

A.C. CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = 25\ ^oC$; $C_L = 50$ pF; input transition times $\leqslant 20$ ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
$I_n \longrightarrow O_n$	5		70	135	ns	43 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	25	55	ns	14 ns + (0,23 ns/pF) C_L
	15		20	40	ns	12 ns + (0,16 ns/pF) C_L
	5		60	120	ns	33 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	25	50	ns	14 ns + (0,23 ns/pF) C_L
	15		15	35	ns	7 ns + (0,16 ns/pF) C_L
Output transition times						
HIGH to LOW	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$900\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	10	$4000\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	f_o = output freq. (MHz)
	15	$10\ 900\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	C_L = load capacitance (pF)

where
f_i = input freq. (MHz)
f_o = output freq. (MHz)
C_L = load capacitance (pF)
$\Sigma(f_oC_L)$ = sum of outputs
V_{DD} = supply voltage (V)