XRD87L94

CMOS, 1 MSPS, 12-Bit
Analog-to-Digital Converter
with Parallel Logic Interface Port

EXAR ...the analog plus company™

March 1996-3

FEATURES

- 12-Bit ADC with DNL = ±1 LSB, INL = ±2.5 LSB
- SNR > 60 dB
- Sampling Frequency ≤ 1 MHz
- Single 3.3 V Supply
- Rail-to-Rail Input Range
- V_{REF} Range: 1.5 V to V_{DD}
- CMOS Low Power: 30 mW (typ)
- 1/4, 1/2 and 3/4 Scale Reference Resistor Taps
- Three-State Outputs
- Binary and Two's Complement Digital Output Mode
- Latch-Up Proof
- ESD: 2000 V Minimum Protection

APPLICATIONS

- Scanners
- Digital Cameras
- Instrumentation
- Medical Imaging
- Digital Oscilloscopes
- Spectrum Analysis

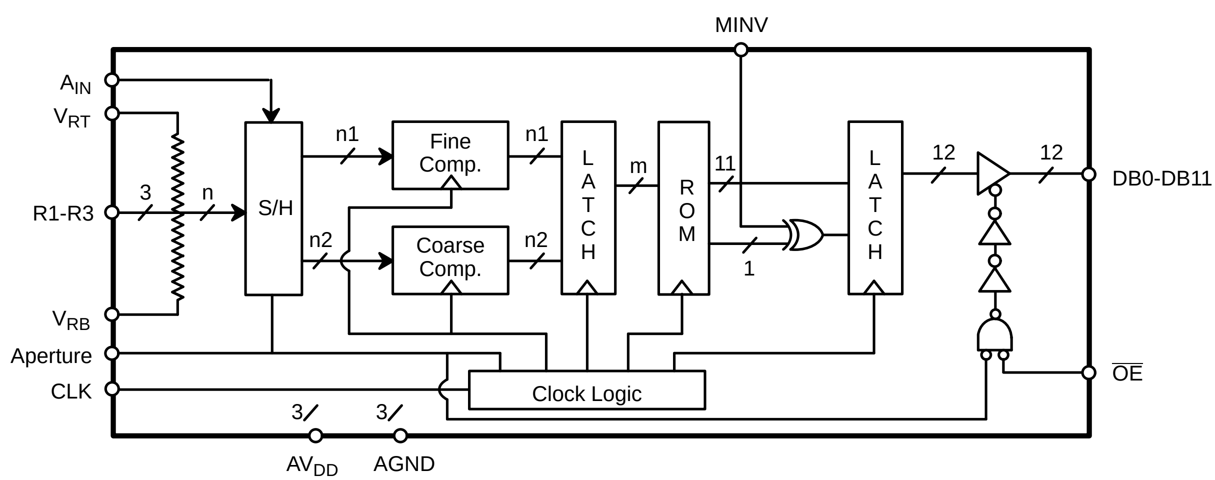
GENERAL DESCRIPTION

The XRD87L94 is a 1 MSPS 12-bit subranging Analog-to-Digital Converter with DNL = ±1 LSB and INL = ±2.5 LSB. The XRD87L94 contains an internal track and hold and an analog input bandwidth of 10 MHz.

The XRD87L94 operates with a single 3.3 V supply while consuming 30 mW of power (typical). Separate pins for reference ladder terminals and power supplies allow flexibility for various A_{IN}, V_{REF}, and power supply ranges.

Data is presented at the parallel output port every clock cycle after a 2.5 cycle pipeline delay from sample edge. The digital output port is also equipped with a 3-state function. MINV enables binary and 2's complement data formatting. Through pins R1-R3, transfer function adjustment can be accommodated.

SIMPLIFIED BLOCK DIAGRAM



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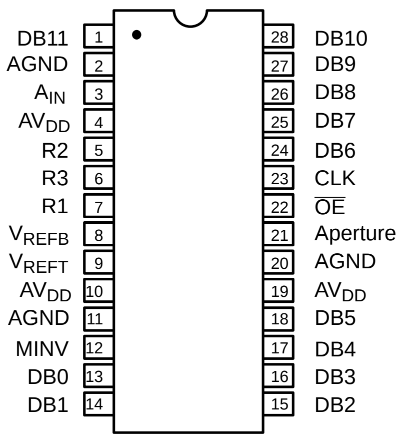
ORDERING INFORMATION

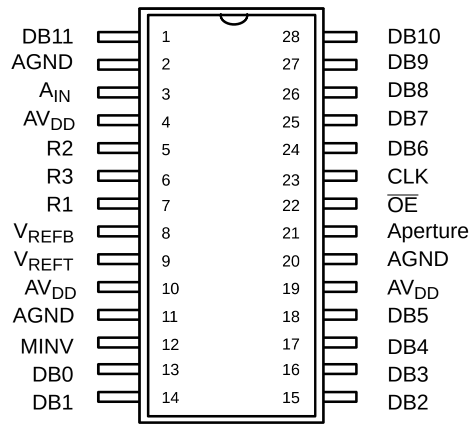
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
PDIP	–40 to +85°C	XRD87L94AIP	±1	±2.5
SOIC (EIAJ)	–40 to +85°C	XRD87L94AIK	±1	±2.5
SOIC (Jedec)	–40 to +85°C	XRD87L94AID	±1	±2.5

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



28 Pin PDIP (0.600”)



28 Pin SOP (EIAJ, 8.4mm)
28 Pin SOIC (Jedec, 0.300”)

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DB11	Data Output Bit 11 (MSB)
2	AGND	Analog Ground
3	A_{IN}	Analog Input
4	AV_{DD}	Analog Positive Supply
5	R2	Ref. Resistor Ladder Tap (1/2 V_{REF})
6	R3	Ref. Resistor Ladder Tap (3/4 V_{REF})
7	R1	Ref. Resistor Ladder Tap (1/4 V_{REF})
8	V_{REFB}	Negative Reference
9	V_{REFT}	Positive Reference
10	AV_{DD}	Analog Positive Supply
11	AGND	Analog Ground
12	MINV	Invert MSB (Active High)
13	DB0	Data Output Bit 0 (LSB)
14	DB1	Data Output Bit 1

PIN NO.	NAME	DESCRIPTION
15	DB2	Data Output Bit 2
16	DB3	Data Output Bit 3
17	DB4	Data Output Bit 4
18	DB5	Data Output Bit 5
19	AV_{DD}	Digital Positive Supply
20	AGND	Digital Negative Supply
21	Aperture	Delayed Clock, indicates sample point
22	$\overline{OE}$	Output Enable (Active Low)
23	CLK	Clock
24	DB6	Data Output Bit 6
25	DB7	Data Output Bit 7
26	DB8	Data Output Bit 8
27	DB9	Data Output Bit 9
28	DB10	Data Output Bit 10

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: $AV_{DD} = DV_{DD}$ = 3.3 V, FS = 1 MHz (50% Duty Cycle), $V_{REF(+)}$ = 3.0 V, $V_{REF(-)}$ = AGND, TA = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution			12		Bits	
Sampling Rate	FS			1	MHz	
ACCURACY[1]						
Differential Non-Linearity	DNL			±1	LSB	
Integral Non-Linearity	INL			±2.5	LSB	Best Fit Line (Max INL – Min INL)/2
Zero Scale Error	EZS		+10		LSB	
Full Scale Error	EFS		–10		LSB	
REFERENCE VOLTAGES						
Positive Ref. Voltage	$V_{REF(+)}$	1.5		AV_{DD}	V	Functional
Negative Ref. Voltage	$V_{REF(-)}$	AGND			V	
Differential Ref. Voltage[3]	V_{REF}	1.5		AV_{DD}	V	
Ladder Resistance	R_L		550		Ω	
ANALOG INPUT						
Input Bandwidth (–3 dB)[4]	BW		3		MHz	
Input Voltage Range	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	V p-p	
Input Capacitance Sample[5]	C_{IN}		50		pF	
Input Capacitance Convert[5]			8		pF	
Aperture Delay from Clock	t_{AP}		55		ns	
Aperture Delay from Aperture Signal	t_{AP}		0		ns	Aperture pin load 5 pF. Measured at 50% point.
DIGITAL INPUTS						
Logical “1” Voltage	V_{IH}	2.5			V	
Logical “0” Voltage	V_{IL}			0.5	V	
Leakage Currents[6]	I_{IN}					V_{IN}=DGND to DV_{DD}
CLK, $\overline{OE}$, MINV			10		µA	
Input Capacitance			5		pF	
Clock Timing						
Clock Period	t_S	0.4	1		µs	Functional
Rise & Fall Time[7]	t_R, t_F		15		ns	Functional
“High” Time	t_{PWH}		500		ns	Functional
“Low” Time	t_{PWL}		500		ns	Functional
Duty Cycle			50		%	
DIGITAL OUTPUTS						C_{OUT}=15 pF
Logical “1” Voltage	V_{OH}	V_{DD}-0.5			V	I_{LOAD} = 1 mA
Logical “0” Voltage	V_{OL}			0.5	V	I_{LOAD} = 1 mA
3-state Leakage	I_{OZ}		1		µA	V_{OUT}=DGND to DV_{DD}
Data Enable Delay	t_{DEN}		60		ns	
Data 3-state Delay	t_{DHZ}		60		ns	
Data Valid Delay	t_{DV}		115		ns	$\overline{OE}$ = 0
Data Invalid Delay	t_{DI}		115		ns	$\overline{OE}$ = 0

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Parameter	Symbol	25°C Min	Typ	Max	Units	Test Conditions/Comments
POWER SUPPLIES[8] **(Tmin to Tmax)**						
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}		3.3		V	
Current (AV_{DD} + DV_{DD})	I_{DD}			12	mA	
AC PARAMETERS						
Signal Noise Ratio (N+D)	SNR		60		dB	F_{IN} = 100 kHz

NOTES

1 Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/4096) is the DNL error. The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage. Accuracy is a function of the sampling rate (FS).
2 Guaranteed. Not tested.
3 Specified values guarantee functionality. Refer to other parameters for accuracy.
4 –3 dB bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.
5 Switched capacitor analog input requires driver with low output resistance.
6 All inputs have diodes to DV_{DD} and DGND. Input(s) $\overline{OE}$ and MINV have internal pull down(s). Input DC currents will not exceed specified limits for any input voltage between DGND and DV_{DD}.
7 Condition to meet aperture delay specifications (t_{AP}, t_{AJ}). Actual rise/fall time can be less stringent with no loss of accuracy.
8 AGND & DGND pins are connected through the silicon substrate.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND . . . . 5.5 V

$V_{REF(+)}$ & $V_{REF(–)}$ . . . . . . V_{DD} +0.5 to GND –0.5 V

V_{IN} . . . . V_{DD} +0.5 to GND –0.5 V

All Inputs . . . . V_{DD} +0.5 to GND –0.5 V

All Outputs . . . . V_{DD} +0.5 to GND –0.5 V

Storage Temperature . . . . –65 to +150°C

Lead Temperature
(Soldering 10 seconds) . . . . +300°C

Package Power Dissipation Rating @ 75°C
PDIP, SOIC 1050mW
Derates above 75°C . . . . 14mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
3 V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

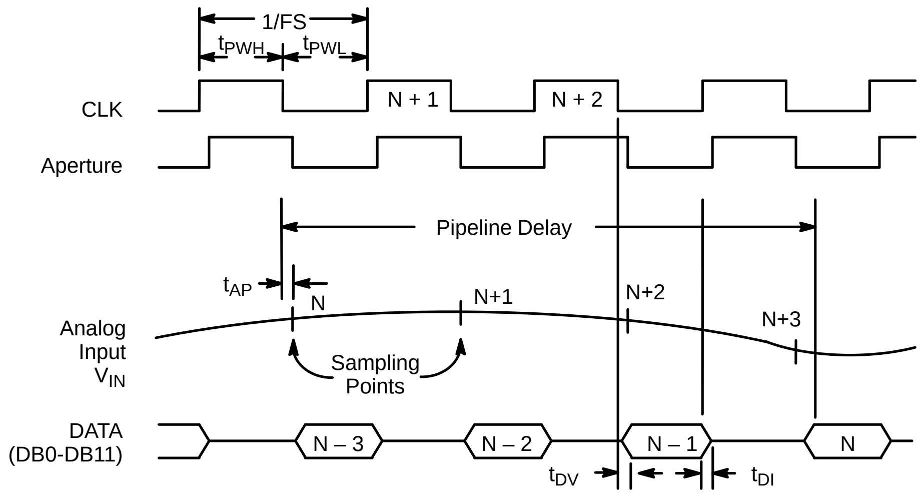


Figure 1. Timing Diagram with $\overline{OE}$ = 0
$t_{DV} = t_{AP} + t_{DEN}$
$t_{DI} = t_{AP} + t_{DHz}$

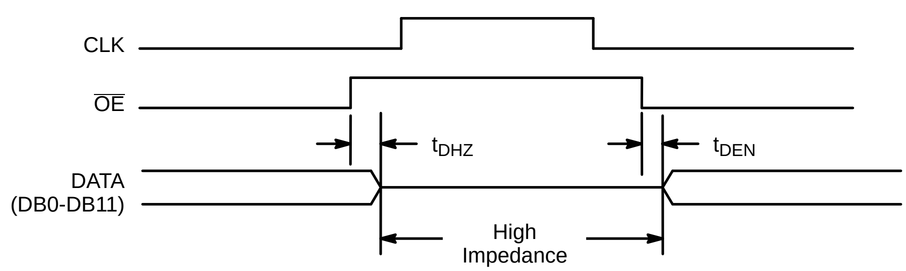


Figure 2. 3-State Timing Diagram

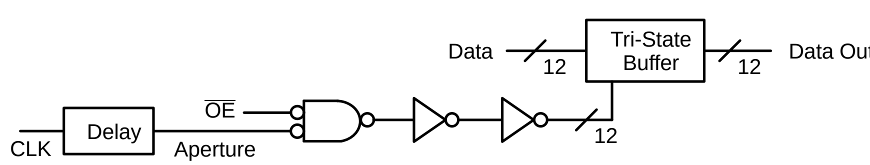


Figure 3. Block Diagram of the XRD87L94 Output

OVERVIEW OF THE XRD87L94 PINS & OPERATION NOTES

$\overline{OE}$: Output Enable (Input)

This signal controls the 3-state drivers on the digital outputs DB0 - DB11 as shown in *Figure 2.* During normal operation, $\overline{OE}$ should be held low so that all outputs are enabled (NOTE: an internal resistor will pull $\overline{OE}$ to this level if it is not connected). When $\overline{OE}$ is driven high, DB0 - DB11 goes into high impedance mode. This control operates asynchronously to the clock and only controls the output drivers. The internal output register will get updated if the clock is running while the outputs are in 3-state mode. The aperture and $\overline{OE}$ signals are internally combined to enable the output data. If aperture is high, the output data bits are tri-stated, independent of $\overline{OE}$. *Figure 3.* shows the circuit used to tri-state the output. This will reduce the errors introduced by digital output coupling during the A_{IN} sample time.

APERTURE: Aperture Delay Sync (Output)

This signal is high when the internal sample/hold function is sampling V_{IN}, and goes low when it is in the hold mode (when the ADC is comparing the stored input value to the reference ladder). The value of V_{IN} at the high to low transition of APERTURE is the value that will be digitized. A system can monitor this signal and adjust the CLK to accurately synchronize the sampling point to an external event. The aperture and $\overline{OE}$ signals are internally combined to enable the output data. If aperture is high, the output data bits are tri-stated, independent of $\overline{OE}$. This will reduce the errors introduced by digital output coupling during the A_{IN} sample time.

MINV: Digital Output Format (Input)

This signal controls the format of the digital output data bits DB0 – DB11. Normally it is held low so the data is in straight binary format (all 0's when $V_{IN} = V_{RB}$; all 1's when $V_{IN} = V_{RT}$). If MINV is pulled high then the MSB (DB11) will be inverted.

MINV is meant to be a static digital signal. If it is to change during operation, it should only change when the CLK is low. Changing MINV on the wrong phase of the CLK will not hurt anything, but the effects on the digital outputs will not be seen until the output latch of the output register is enabled. MINV has an internal pull down device.

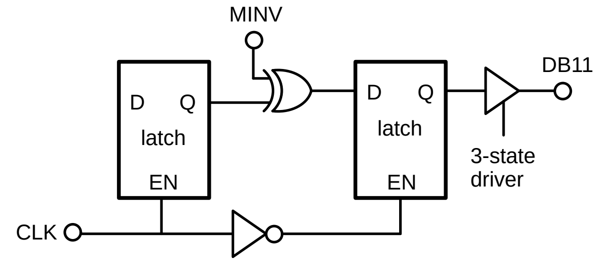


Figure 4. MINV Simplified Logic Circuit

V_{IN} Analog Input

This part has a switched capacitor type input circuit. This means that the input impedance changes with the phase of the input clock. V_{IN} is sampled at the high to low clock transition. The diagram *Figure 5.* shows an equivalent input circuit.

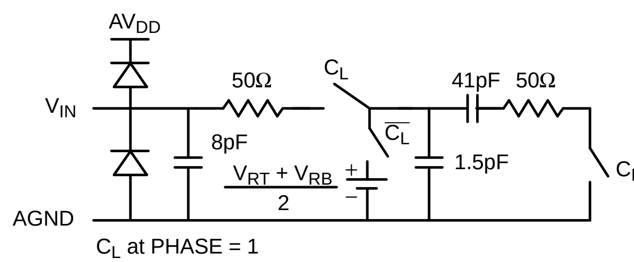


Figure 5. Equivalent Input Circuit

R1, R2, R3: Reference Ladder Taps

These taps connect to every 1/4 point along the reference ladder; R1 is 1/4th up from V_{RB}, R3 is 3/4ths up from V_{RB} (or 1/4th down from V_{RT}). Normally these pins should have 0.1 microfarad capacitors to V_{SS}; this helps reduce the INL errors by stabilizing the reference ladder voltages.

These taps can also be used to alter the transfer curve of the ADC. A 4-segment, piecewise linear, custom transfer curve can be designed by connecting voltage sources to these pins.

This may be desirable to make the probability of codes for a certain range of V_{IN} be enhanced or minimized.

Sometimes this is referred to as probability density function shaping, or histogram shaping.

The internal interconnect resistance from each of the t_{AP} pins to the ladder is less than 3Ω.

1.6V maximum per tap is recommended for applications above 85°C. Up to 3.2V is allowed for applications under 85°C.

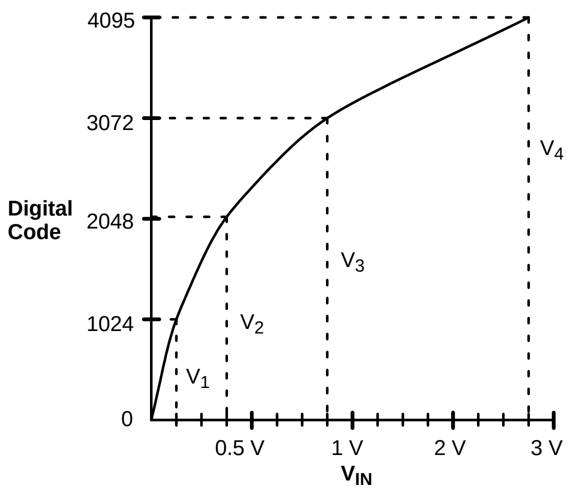
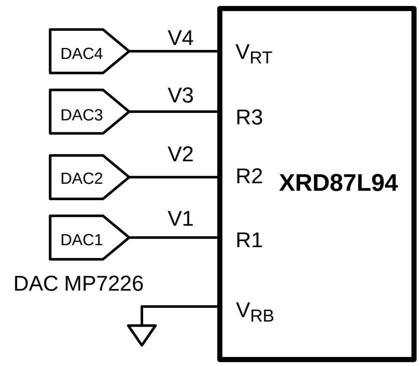


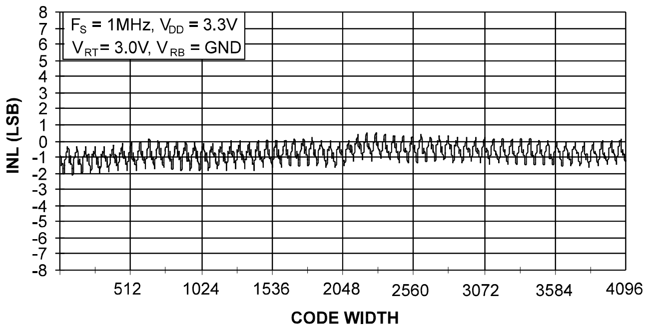
Figure 6. A Piecewise Linear Transfer Function



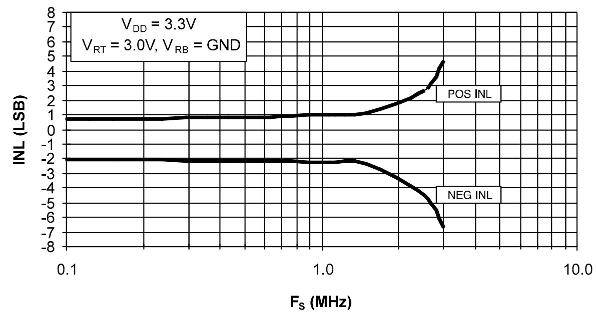
Only the Ladder detail shown.

Figure 7. A/D with Programmed Ladder Control for Creating a Piecewise Linear Transfer Function

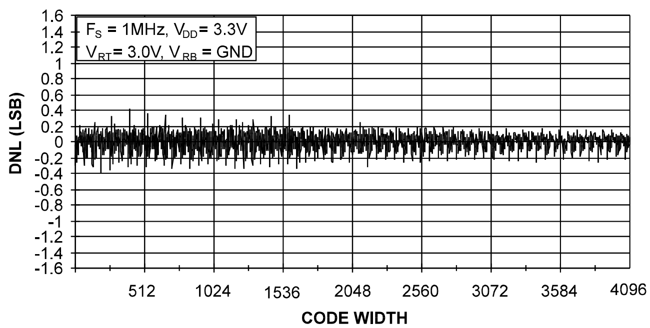
PERFORMANCE CHARACTERISTICS



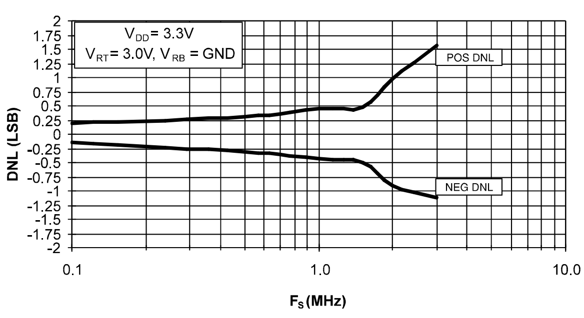
Graph 1. INL



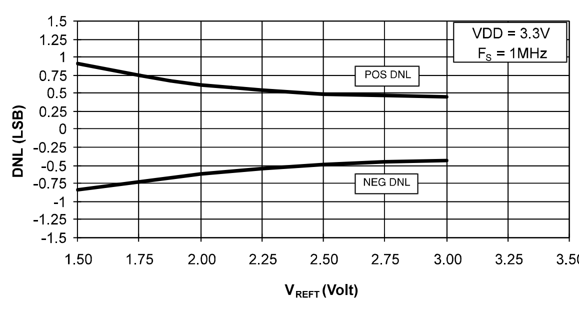
Graph 2. INL vs. Sampling Frequency



Graph 3. DNL



Graph 4. DNL vs. Sampling Frequency



Graph 5. DNL vs. Reference Voltage

Graph 1. I_{DD} vs. Sampling Frequency

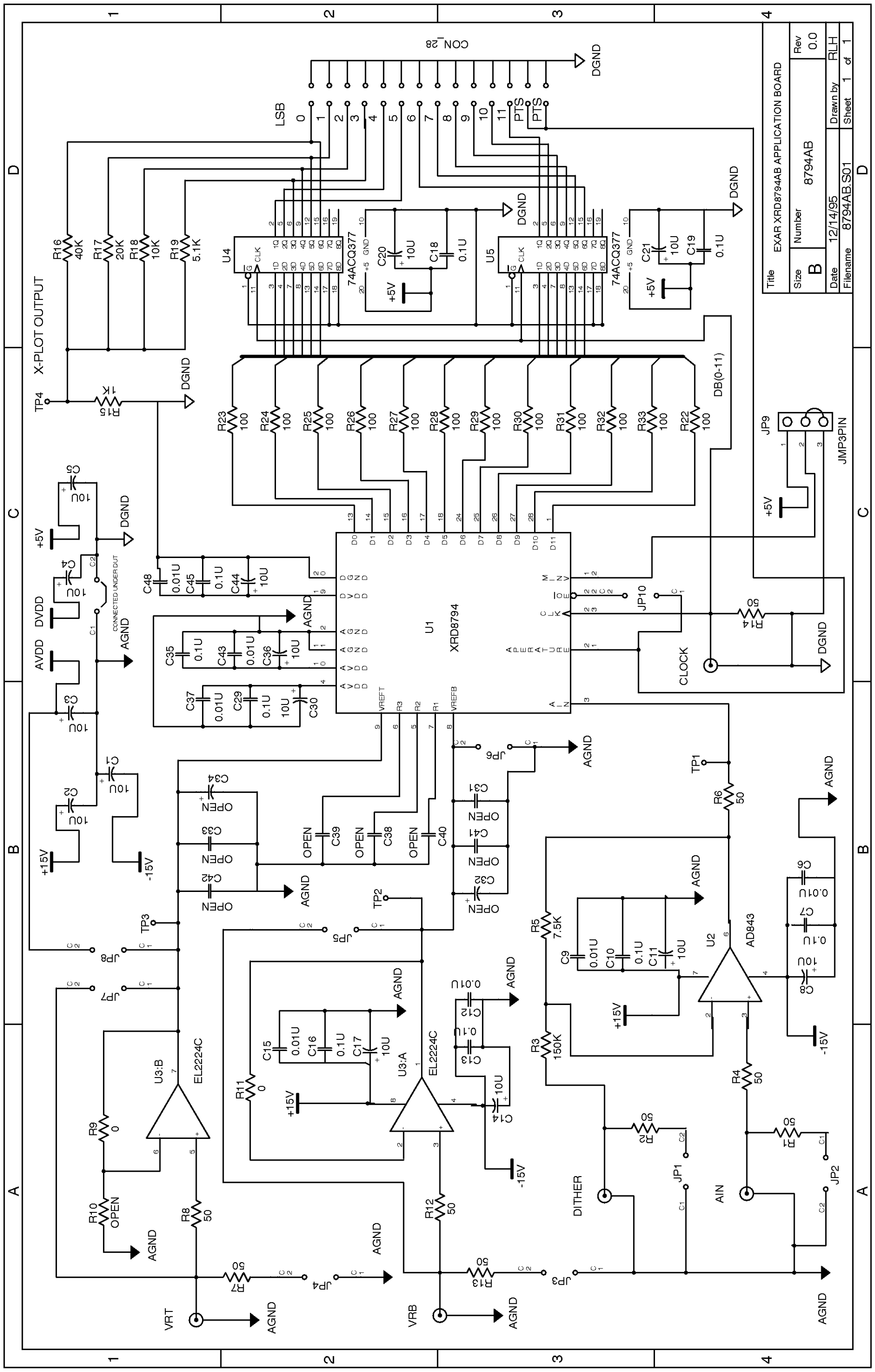
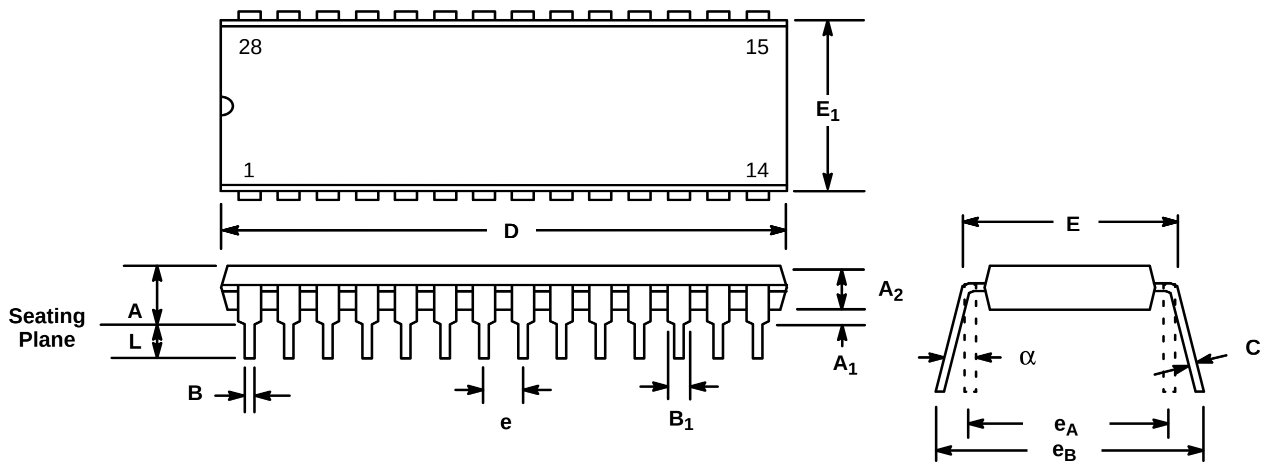


Figure 8. XRD8794AB Schematic

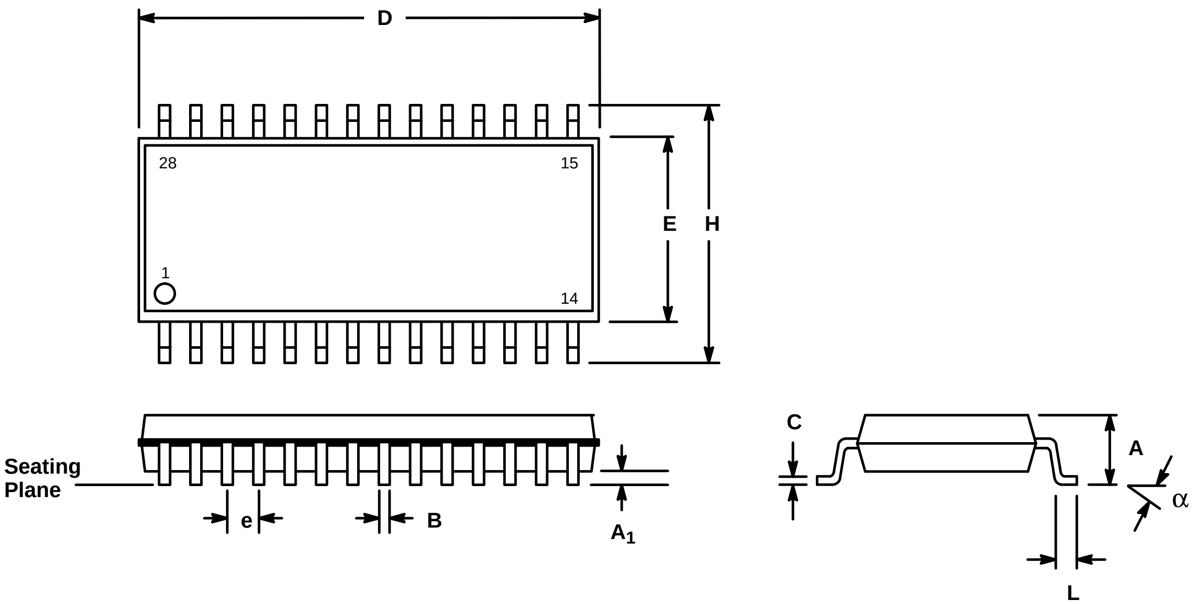
28 LEAD PLASTIC DUAL-IN-LINE (600 MIL PDIP)



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.160	0.250	4.06	6.35
A_1	0.015	0.070	0.38	1.78
A_2	0.125	0.195	3.18	4.95
B	0.014	0.024	0.36	0.56
B_1	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	1.380	1.565	35.05	39.75
E	0.600	0.625	15.24	15.88
E_1	0.485	0.580	12.32	14.73
e	0.100 BSC		2.54 BSC	
e_A	0.600 BSC		15.24 BSC	
e_B	0.600	0.700	15.24	17.78
L	0.115	0.200	2.92	5.08
α	0°	15°	0°	15°

Note: The control dimension is the inch column

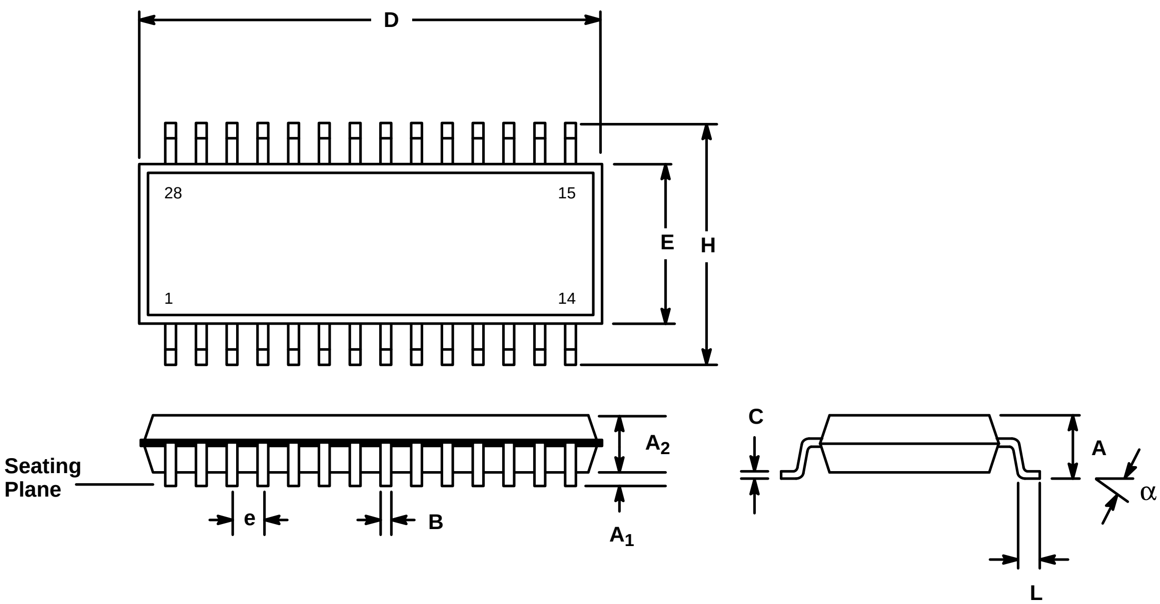
28 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.697	0.713	17.70	18.10
E	0.291	0.299	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

Note: The control dimension is the millimeter column

28 LEAD SMALL OUTLINE (8.4 mm EIAJ SOP)



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.098	0.114	2.50	2.90
A_1	0.004	0.012	0.10	0.30
A_2	0.094	0.102	2.40	2.60
B	0.012	0.020	0.30	0.50
C	0.004	0.008	0.10	0.20
D	0.693	0.713	17.60	18.10
E	0.327	0.335	8.30	8.50
e	0.050 BSC		1.27 BSC	
H	0.453	0.477	11.50	12.10
L	0.028	0.051	0.70	1.30
α	0°	10°	0°	10°

Note: The control dimension is the millimeter column

Notes

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NOTICE

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