STA8088TG

GPS/Galileo/Glonass/QZSS tracker

Data brief

Features

- STMicroelectronics® 3rd generation positioning receiver with 32 Tracking channels and 2 fast acquisition channels compatible with GPS, Galileo and Glonass systems
- Hosted optimized architecture where host resources are available to execute
  - Positioning Software
  - ST-AGPS
  - Dead Reckoning SW
- Embedded RAM enough for running acquisition/tracking tasks (Flashless solution)
- TCXO Clock Out Available
- Embedded RF Front-End with separate GPS/Galieo/QZSS and Glonass IF outputs
- Embedded low noise amplifier
- -162 dBm indoor sensitivity (tracking mode)
- Fast TTFF < 1 s in Hot start and 35 s in Cold Start
- High performance ARM946 MCU (up to 208 MHz)
- 256 Kbyte embedded SRAM
- 2 UARTs
- 3 Embedded 1.8 V voltage regulators
- I/O level selectable 1.8 V or 3.3 V
- Operating Condition:
  - V_{DD12}: 1.2 V ±10%
  - $V_{DD18/RF18}$: 1.8 V ±5%
  - V_{LPVR} 1.62 V to 3.6 V
  - V_{ddIO}: 1.8 V ±5%; 3.3 V ±10%
- ST Automotive Grade compliant
- Packages:
  - VFQFPN56 (7x7x0.85mm) 0.4 mm Pitch
  - VFQFPN56 (8x8x0.85mm) 0.5 mm Pitch
- Ambient temperature range: -40/+85°C

VFQFPN56

Description

STA8088TG is a host based positioning receivers IC working on multiple constellations (GPS/Galileo/Glonass/QZSS).

STA8088TG family enables telematic and handset manufacturers to differentiate in the market by providing the best performing solution at lowest system cost.

The device is offered with a complete GNSS firmware which performs all GNSS operations including tracking, acquisition, navigation and data output compatible with different Host operating Systems.

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1 Overview

STA8088TG is a highly integrated System-On-Chip device designed for positioning systems applications.

The embedded SRAM combined with a high performance ARM946 microprocessor allows the running of acquisition/tracking tasks without the need of external Flash.

The RF Front-End and GNSS engines are able to support simultaneously GPS/Galileo/Glonass and QZSS navigation systems.

The device is power supplied with 1.8 V and uses three on-chip voltage regulators to internally supply the RF front-End, core logic and the backup logic. In order to reduce the power consumption the chip can be directly powered with 1.2 V bypassing the embedded voltage regulators which will be put in power down mode. I/O lines are compatible with 1.8 V and 3.3V.

The chip, using STMicroelectronics CMOSRF Technology, is housed in either VFQFPN56 (7 x 7 x 0.85 mm) or VFQFPN56 (8 x 8 x 0.85 mm) packages.

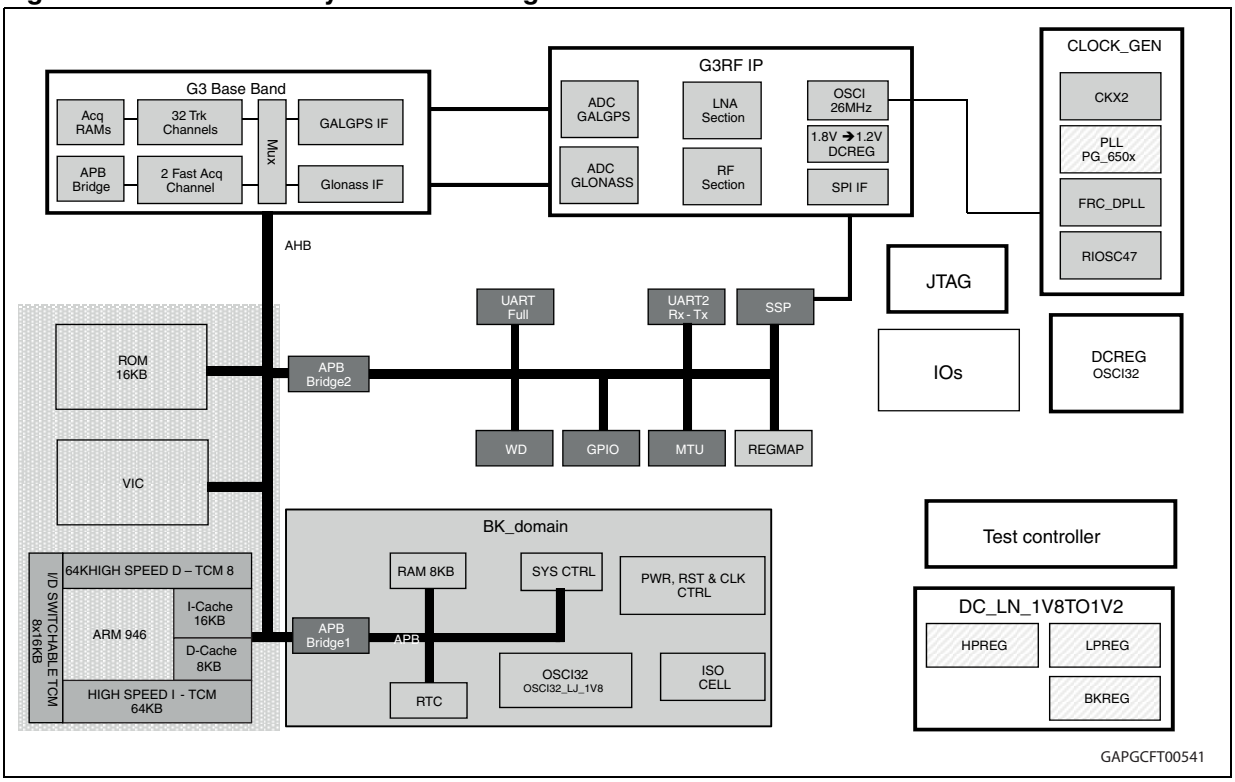
The ST Automotive Grade devices (see *Figure 4: Ordering information scheme*) with in addition to AEC-Q100 qualification include a set of production flow methodology targeting zero defect per million. They, fulfilling high quality and service level automotive market requirements, are the ideal solution for in-dash navigation and OEM telematic application.

STA8088TG family enables telematic and handset manufacturers to differentiate in the market by providing the best performing solution at lowest system cost.

2 Pin description

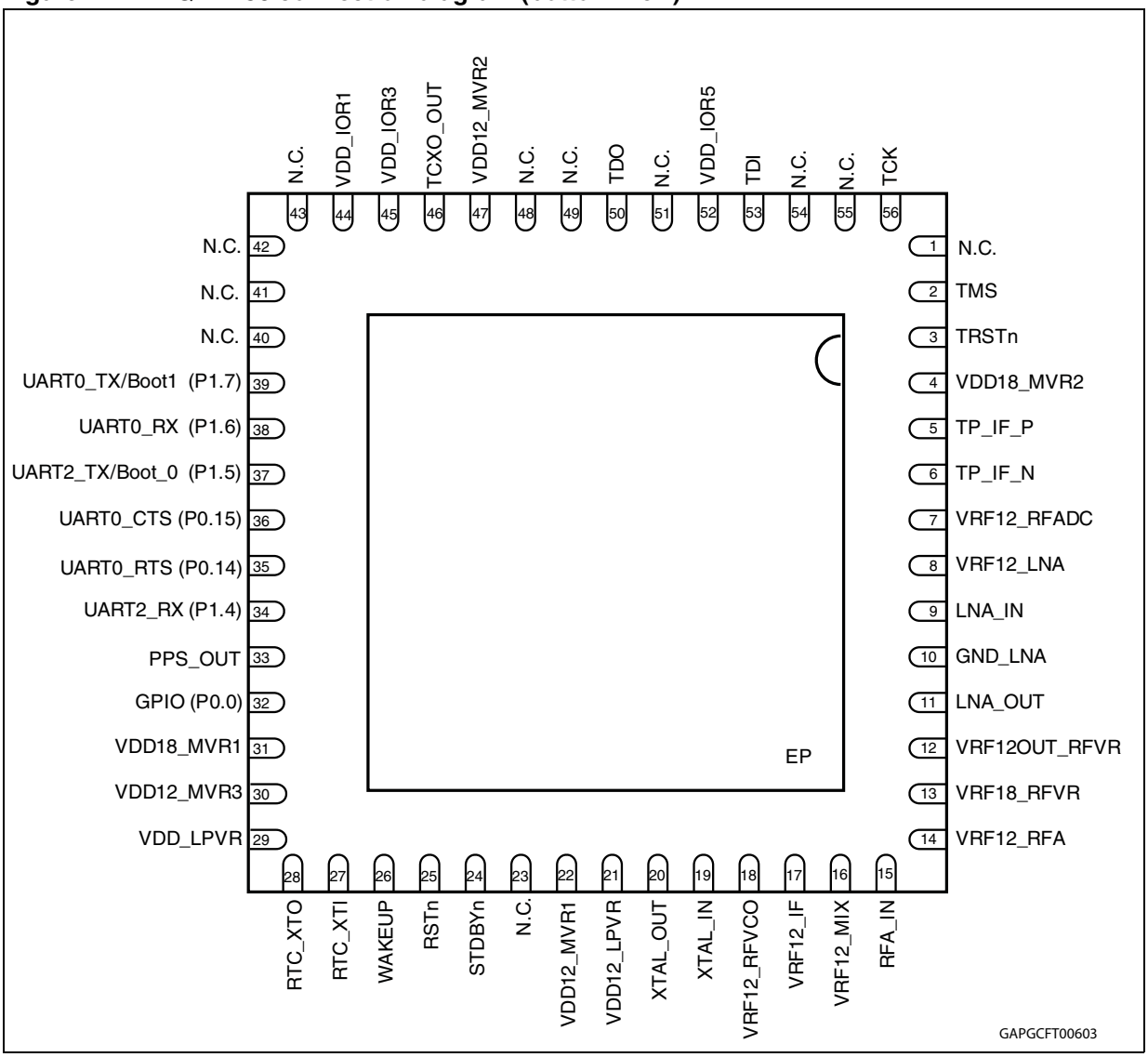
2.1 Block diagram

Figure 1. STA8088TG system block diagram



2.2 VFQFPN56 pin configuration

Figure 2. VFQFPN56 connection diagram (bottom view)



2.3 Power supply pins

Table 1. Power supply pins

Symbol	I/O	Functions	VFQFN56
VDD18_MVR[1,2]	Pwr	Digital supply voltage for main voltage regulator (1.8 V)	31,4
VDD12_MVR[1,2,3]	Pwr	Digital supply voltage for core circuitry (1.2 V). When using the MVR, this pin shall not be driven by an external voltage supply, but a capacitance shall be connected between these pins and GND to guarantee on-chip voltage stability.	22,47,30
VDD_LPVR	Pwr	Digital supply voltage for low power voltage regulator (1.62 - 3.6 V)	29
VDD12_LPVR	Pwr	Digital supply voltage for backup logic (1.2 V). When using the LPVR, this pin shall not be driven by an external voltage supply, but a capacitance shall be connected between these pins and GND to guarantee on-chip voltage stability.	21
VDD_IOR1	Pwr	Digital supply voltage for I/O ring 1 (1.8 or 3.3V)	44
VDD_IOR3	Pwr	Digital supply voltage for I/O ring 3 (1.8V)	45
VDD_IOR5	Pwr	Digital supply voltage for I/O ring 5 (3.3V)	52
VRF18_RFVR	Pwr	Analog supply voltage for RF voltage regulator (1.8V)	13
VRF12OUT_RFVR	Pwr	RF voltage regulator 1.2V output	12
VRF12_LNA	Pwr	Analog supply voltage for LNA (1.2V)	8
VRF12_RFA	Pwr	Analog supply voltage for RFA (1.2V)	14
VRF12_MIX	Pwr	Analog supply voltage for Mixer (1.2V)	16
VRF12_IF	Pwr	Analog supply voltage for IF (1.2V)	17
VRF12_RFVCO	Pwr	Analog supply voltage for VCO (1.2V)	18
VRF12_RFADC	Pwr	Analog supply voltage for RF ADC (1.2V)	7
GND_LNA	GND	Analog supply ground for LNA	10
GND	GND	Analog and digital supply ground	EP

2.4 Main function pins

Table 2. Main function pins

Symbol	I/O voltage	I/O	Functions	VFQFPN56
STDBYn	1.2V	I	When low, the chip is forced in Standby Mode - All pins in high impedance except the ones powered by Backup supply	24
RSTn	1.2V	I	Reset Input with Schmitt-Trigger characteristics and noise filter.	25
WAKEUP	1.2V	I	WAKEUP from STANDBY mode	26
RTC_XTI	1.5V (Max)	I	Input of the 32KHz oscillator amplifier circuit and input of the internal real time clock circuit.	27

Table 2. Main function pins (continued)

Symbol	I/O voltage	I/O	Functions	VFQFPN56
RTC_XTO	1.5V (Max)	O	Output of the oscillator amplifier circuit.	28
PPS_OUT	VDD_IOR1	O	Pulse per second output	33
TCXO_OUT	VDD_IOR3	O	Buffered TCXO output	46

2.5 Test/emulated dedicated pins

Table 3. Test/emulated dedicated pins

Symbol	I/O voltage	I/O	Functions	VFQFPN56
TDO	VDD_IOR5	O	JTAG test data out	50
TDI	VDD_IOR5	I	JTAG test data in	53
TCK	VDD_IOR5	I	JTAG test clock	56
TMS	VDD_IOR5	I	JTAG test mode select	2
TRSTn	VDD_IOR5	I	JTAG test circuit reset	3
TP_IF_P	VRF12_IF	O	Diff.test point for IF – positive	5
TP_IF_N	VRF12_IF	O	Diff.test point for IF – negative	6

2.6 RF front-end pins

Table 4. RF front-end pins

Symbol	I/O voltage	I/O	Functions	VFQFPN56
LNA_IN	VRF12_LNA	I	Low noise amplifier input	9
LNA_OUT	VRF12_LNA	O	Low noise amplifier output	11
RFA_IN	VRF12_RFA	I	RF amplifier input	15
XTAL_IN	VRF12_RFDig	I	Input side of crystal oscillator or TCXO input	19
XTAL_OUT	VRF12_RFDig	O	Output side of crystal oscillator	20

2.7 Port 0 pins

Port 0 consists of a 32-bit bidirectional I/O port (only 3-bit are used in STA8088TG).

It can be either used as general purpose Input or Output port, or configured according to the associated alternate functions.

Table 5. Port 0 pins

Symbol	I/O voltage	I/O	Mode	Functions	VFQFPN56
P0.0	VDD_IOR1	IO	Default	GPIO.0: General Purpose IO	32
		I	A	PPS_IN: Pulse Per Second Input	
		O	B	PPS_OUT: Pulse Per Second Output	
P0.14	VDD_IOR1	O	Default	UART0_RTS: UART0 request to send	35
		IO	A	GPIO.14: General Purpose IO	
P0.15	VDD_IOR1	I	Default	UART0_CTS: UART0 clear to send	36
		IO	A	GPIO.1: General Purpose IO	

2.8 Port 1 pins

Port 1 consists of a 32-bit bidirectional I/O port (only 4-bit are used in STA8088TG).

It can be either used as general purpose Input or Output port, or configured according to the associated alternate functions.

Table 6. Port 1 pins

Symbol	I/O Voltage	I/O	Mode	Functions	VFQFPN56
P1.4	VDD_IOR1	I	Default	UART2_RX: UART 2 Rx data	34
		I/O	A	GPIO36: general purpose I/O	
P1.5	VDD_IOR1	I/O	Default	UART2_TX / BOOT_0: UART 2 Tx data / ARM Boot 0	37
		I/O	A	GPIO37: general purpose I/O	
P1.6	VDD_IOR1	I	Default	UART0_RX: UART 0 Rx data	38
		I/O	A	GPIO38: general purpose I/O	
P1.7	VDD_IOR1	I/O	Default	UART0_TX / BOOT_1: UART 0 Tx data / ARM Boot 1	39
		I/O	A	GPIO39: general purpose I/O	

3 Package and packing information

3.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

3.2 VFQFPN56 package information

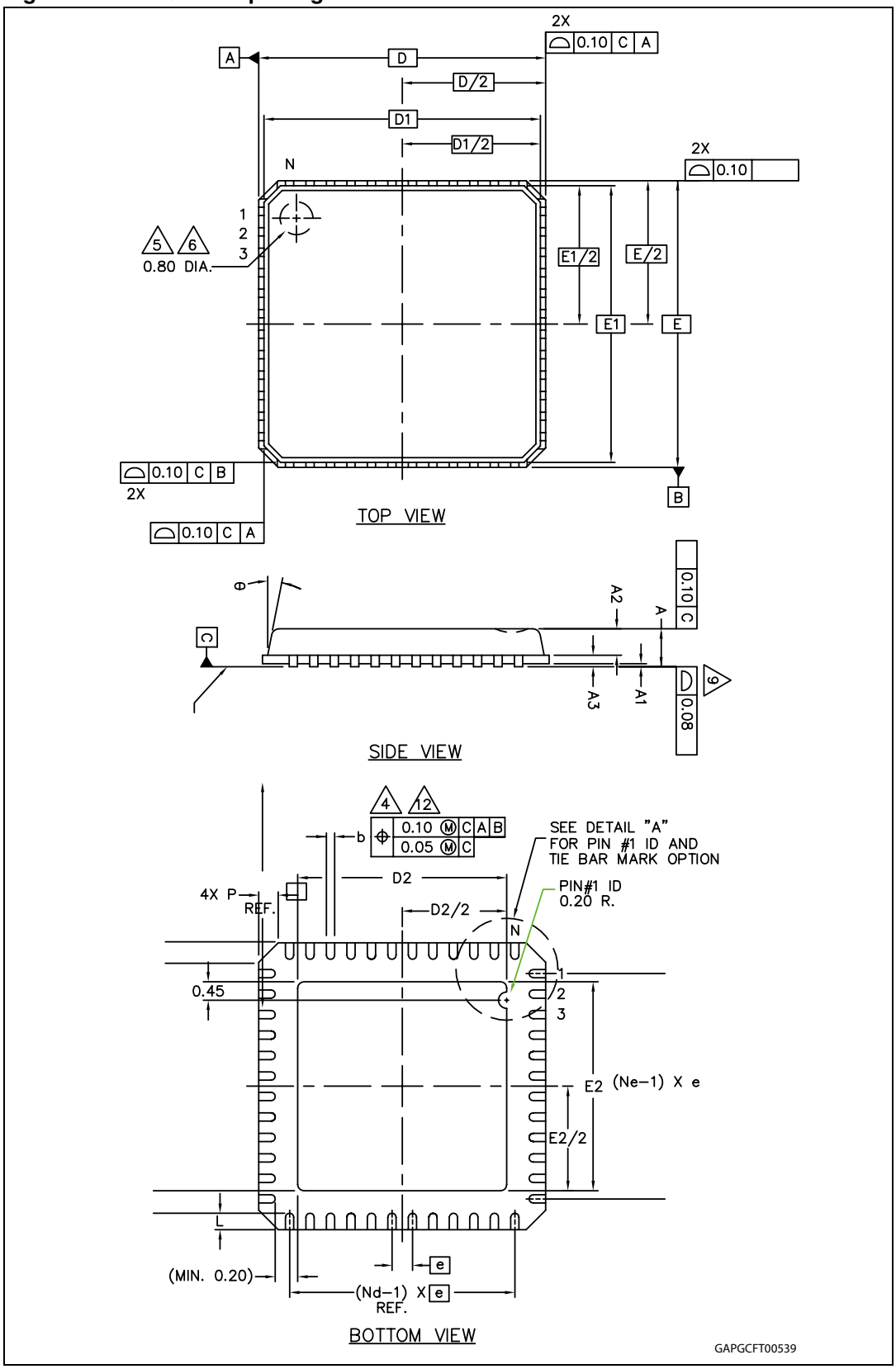
Table 7. VFQFPN56 7 x 7 x 0.85 mm package dimensions

Symbol	Min.	Typ.	Max
Common dimensions			
A	0.80	0.85	0.90
A1	0	0.01	0.05
A2	0.60	0.65	0.70
A3		0.20 REF	
b	0.15	0.20	0.25
D		7.00 BSC	
D1		6.75 BSC	
D2	5.0	5.1	5.2
E		7.00 BSC	
E1		6.75 BSC	
E2	5.0	5.1	5.2
e		0.40 BSC	
θ	0°		12°
L	0.30	0.40	0.50
N		56	
Nd		14	
Ne		14	
P	0.24	0.42	0.60

Table 8. VFQFPN56 8 x 8 x 0.85 mm package dimensions

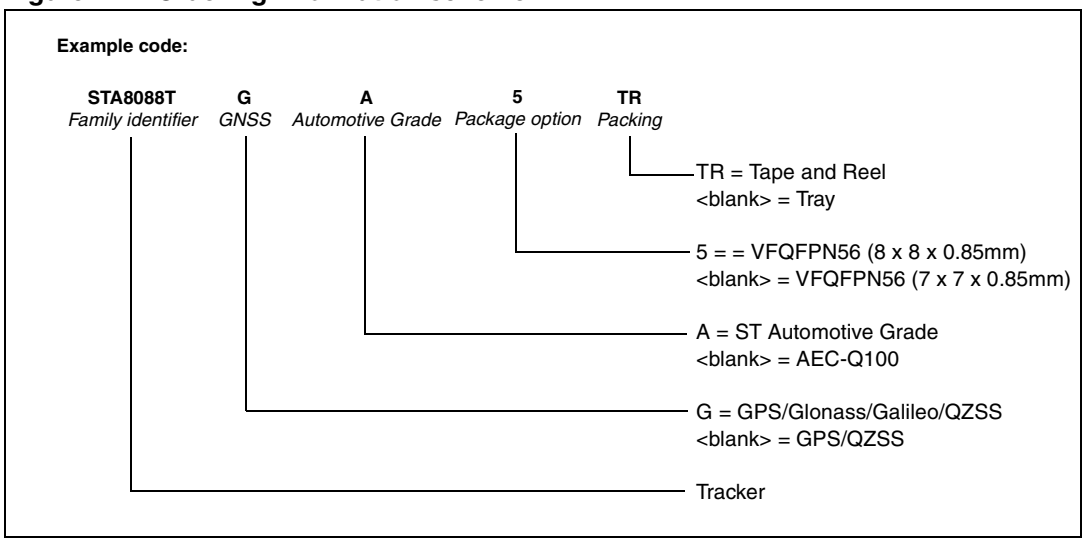
Symbol	Min.	Typ.	Max
Common dimensions			
A	0.80	0.85	0.90
A1	0	0.01	0.05
A2	0.60	0.65	0.70
A3		0.20 REF	
b	0.18	0.23	0.30
D		8.00 BSC	
D1		7.75 BSC	
D2	5.2	5.3	5.4
E		8.00 BSC	
E1		7.75 BSC	
E2	5.2	5.3	5.4
e		0.50 BSC	
θ	0°		12°
L	0.30	0.40	0.50
N		56	
Nd		14	
Ne		14	
P	0.24	0.42	0.60

Figure 3. VFQFPN56 package dimension



4 Ordering information

Figure 4. Ordering information scheme



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
26-Jan-2012	1	Initial release.
17-Feb-2012	2	Updated *Features* list. *Table 7: VFQFPN56 7 x 7 x 0.85 mm package dimensions*: – Q, R: removed rows Added *Table 8: VFQFPN56 8 x 8 x 0.85 mm package dimensions* Upfated *Figure 4: Ordering information scheme*

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