QuickSwitch® Products
High-Speed CMOS 10-Bit Bus Switch With Flow-Thru Pinout

FEATURES/BENEFITS

- Enhanced N channel FET with no inherent diode to V_{CC}
- 5Ω bidirectional switches connect inputs to outputs
- Zero propagation delay (3861), zero ground bounce
- Undershoot clamp diodes on all switch and control pins
- Available in 24-pin QSOP and in 24-pin SOIC (SO) packages
- QS32861 is 25Ω version for low noise

APPLICATIONS:

- Hot-swapping, hot-docking (Application Note AN-13)
- Voltage translation (5V to 3.3V; Application Note AN-11)
- Power conservation
- Capacitance reduction and isolation
- Bus isolation
- Clock gating

DESCRIPTION

The QS3861 and QS32861 each provide a set of ten high speed CMOS, TTL-compatible bus switches. The low ON resistance (5Ω) of the QS3861 allows inputs to be connected to outputs without adding propagation delay and without generating additional ground bounce noise. The Bus Enable (BE) signal turns the switches on.

The QS32861 includes internal 25Ω series termination resistors to reduce reflection noise in high speed applications. When closed, the switch acts as the source (series) termination for the driver connected to it.

Figure 1. Functional Block Diagram

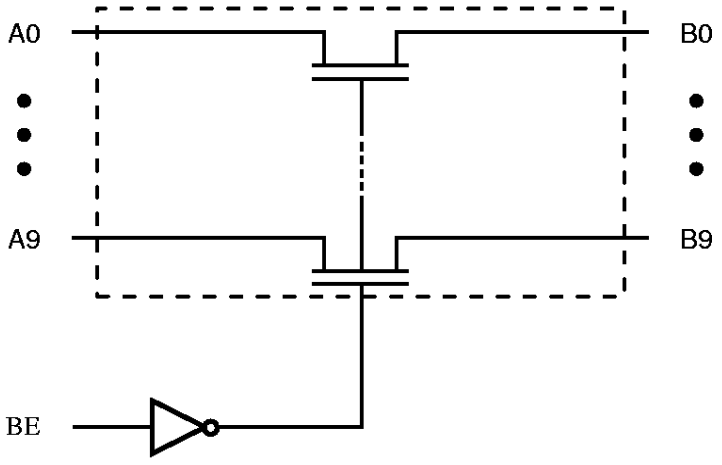


Table 1. Pin Description

Name	Function
$\overline{BE}$	Bus Enable
A0-A9	Bus A
B0-B9	Bus B

Figure 2. Pin Configuration (All Pins Top View)

QSOP, SOIC (SO)

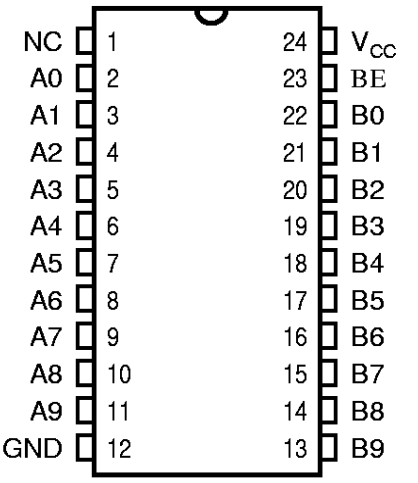


Table 2. Function Table

$\overline{BE}$	A0-A9	Function
H	Hi-Z	Disconnect
L	B0-B9	Connect

Table 3. Absolute Maximum Ratings

Supply Voltage to Ground	–0.5V to +7.0V
DC Switch Voltage V_S	–0.5V to +7.0V
DC Input Voltage V_{IN}	–0.5V to +7.0V
AC Input Voltage (for a pulse width ≤ 20ns)	–3.0V
DC Output Current Max. Sink Current/Pin	120mA
Maximum Power Dissipation	0.5 watts
T_{STG} Storage Temperature	–65° to +150°C

Note: ABSOLUTE MAXIMUM CONTINUOUS RATINGS are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum conditions is not implied.

Table 4. Capacitance

T_A = 25°C, f = 1MHz, V_{IN} = 0V

Pins	QSOP, SOIC Typ	QSOP, SOIC Max	Unit
Control Inputs	3	5	pF
QuickSwitch Channels (Switch OFF)	5	7	pF

Note: Capacitance is characterized but not production tested. For total capacitance while the switch is ON, please see Section 1 under "Input and Switch Capacitance."

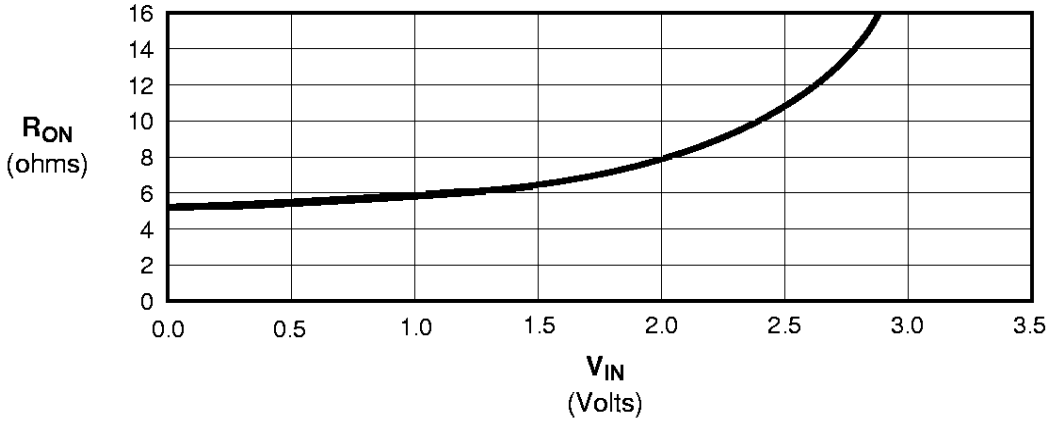
Table 5. DC Electrical Characteristics Over Operating Range

T_A = –40°C to 85°C, V_{CC} = 5.0V ± 5%

Symbol	Parameter	Test Conditions		Min	Typ(1)	Max	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs		2.0	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs		—	—	0.8	V
$\lvert I_{IN} \rvert$	Input Leakage Current (Control Input)	$0 \le V_{IN} \le V_{CC}$		—	0.01	1	µA
$\lvert I_{OZ} \rvert$	Off-State Current (Hi-Z)	$0 \le V_{OUT} \le V_{CC}$, Switches Off		—	0.01	1	µA
R_{ON}	Switch ON Resistance(2)	V_{CC} = Min. V_{IN} = 0.0V I_{ON} = 30mA	3861	—	5	7	Ω
			32861	20	28	40	
R_{ON}	Switch ON Resistance(2)	V_{CC} = Min. V_{IN} = 2.4V I_{ON} = 15mA	3861	—	10	15	Ω
			32861	20	35	48	
V_P	Pass Voltage(3)	$V_{IN} = V_{CC}$ = 5V, I_{OUT} = –5µA		3.7	4	4.2	V

Notes:
1. Typical values indicate V_{CC} = 5.0V and T_A = 25°C.
2. For a diagram explaining the procedure for R_{ON} measurement, please see Section 1 under "DC Electrical Characteristics." Max. value of R_{ON} guaranteed, but not production tested.
3. Pass Voltage is guaranteed but not production tested.

Figure 3. Typical ON Resistance vs V_{IN} at V_{CC} = 5.0V (QS3861)



Note: For QS32861, add 23Ω to R_{ON} shown.

Table 6. Power Supply Characteristics Over Operating Range

T_A = –40°C to 85°C, V_{CC} = 5.0V ± 5%

Symbol	Parameter	Test Conditions[1]	Typ[2]	Max	Unit
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}, f = 0	0.2	3.0	µA
ΔI_{CC}	Power Supply Current per Input HIGH	V_{CC} = Max., V_{IN} = 3.4V[3], f = 0 per Control Input	—	2.5	mA
Q_{CCD}	Dynamic Power Supply Current per MHz[4]	V_{CC} = Max., A and B Pins Open, $\overline{BE}$ Input Toggling @ 50% Duty Cycle	—	0.25	mA/ MHz

Notes:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Typical Values are at V_{CC} = 5.0V, +25°C Ambient.
3. Per TTL driven input (V_{IN} = 3.4V, control inputs only). A and B pins do not contribute to ΔI_{CC}.
4. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is guaranteed, but not production tested.

Table 7. Switching Characteristics Over Operating Range

T_A = –40°C to 85°C, V_{CC} = 5.0V ± 5%
C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.

		QS3861			QS32861			
Symbol	Description[1]	Min	Typ	Max	Min	Typ	Max	Unit
t_{PLH} t_{PHL}	Data Propagation Delay[2,4] A to B or B to A	—	—	0.25[3]	—	—	1.25[3]	ns
t_{PZL} t_{PZH}	Switch Turn-on Delay $\overline{BE}$ to A or B	1.5	—	6.5	1.5	—	7.5	ns
t_{PLZ} t_{PHZ}	Switch Turn-off Delay[2] $\overline{BE}$ to A or B	1.5	—	5.5	1.5	—	5.5	ns

Notes:
1. See Test Circuit and Waveforms. Minimums guaranteed but not production tested.
2. This parameter is guaranteed, but not production tested.
3. The time constant for the switch alone is of the order of 0.25ns for QS3861 and 1.25ns for QS32861 at C_L = 50pF.
4. The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.