# Self-Protected Low Side Driver with Temperature and Current Limit

# 42 V, 10 A, Single N–Channel, DPAK

NCV8408 is a single channel protected Low-Side Smart Discrete device. The protection features include overcurrent, overtemperature, ESD and integrated Drain-to-Gate clamping for overvoltage protection. Thermal protection includes a latch which can be reset by toggling the input. This device is suitable for harsh automotive environments.

#### Features

- Short Circuit Protection
- Thermal Shutdown with Latched Reset
- Gate Input Current Flag During Latched Fault Condition
- Overvoltage Protection
- Integrated Clamp for Inductive Switching
- ESD Protection
- dV/dt Robustness
- Analog Drive Capability (Logic Level Input)
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

#### **Typical Applications**

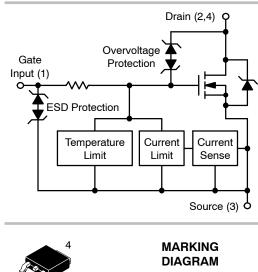
- Switch a Variety of Resistive, Inductive and Capacitive Loads
- Can Replace Electromechanical Relays and Discrete Circuits
- Automotive / Industrial

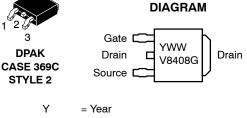


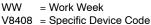
# **ON Semiconductor®**

#### http://onsemi.com

V <sub>DSS</sub> (Clamped)	R <sub>DS(on)</sub> TYP	I <sub>D</sub> MAX (Limited)
42 V	55 mΩ @ 5 V	10 A







G = Pb-Free Package

#### **ORDERING INFORMATION**

	Device	Package	Shipping <sup>†</sup>
I	NCV8408DTRKG	DPAK (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

#### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Rating		Value	Unit
Drain-to-Source Voltage Internally Clamped	V <sub>DSS</sub>	42	Vdc
Drain-to-Gate Voltage Internally Clamped $(R_{GS} = 1.0 M\Omega)$	V <sub>DGR</sub>	42	V
Gate-to-Source Voltage	V <sub>GS</sub>	±14	Vdc
Continuous Drain Current	I <sub>D</sub>	Internally Limited	
Total Power Dissipation @ $T_A = 25^{\circ}C$ (Note 1) @ $T_A = 25^{\circ}C$ (Note 2)	P <sub>D</sub>	1.8 2.3	W
Thermal Resistance Junction-to-Ambient Steady State (Note 1) Junction-to-Ambient Steady State (Note 2) Junction-to-Tab Steady State (Note 3)	$f R_{ heta JA} \ R_{ heta JA} \ R_{ heta JA} \ R_{ heta JT}$	70 55 2.1	°C/W
Single Pulse Inductive Load Switching Energy $(V_{DD} = 20 \text{ Vdc}, V_{GS} = 5.0 \text{ V}, I_L = 8.0 \text{ A})$	E <sub>AS</sub>	140	mJ
Load Dump Voltage (V_{GS} = 0 and 10 V, R_I = 2.0 $\Omega,$ R_L = 4.5 $\Omega,$ t_d = 400 ms)	V <sub>LD</sub>	63	V
Operating Junction Temperature	TJ	-40 to 150	°C
Storage Temperature	T <sub>stg</sub>	-55 to 150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Surface-mounted onto minimum pad FR4 PCB (1 oz Cu, 0.06" thick).
 Surface-mounted onto 2" square FR4 PCB, (1" square, 1 oz Cu, 0.06" thick).
 Surface-mounted onto minimum pad FR4 PCB (2 oz Cu, 0.06" thick).

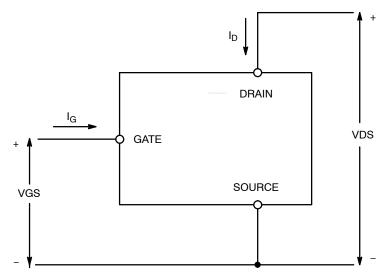
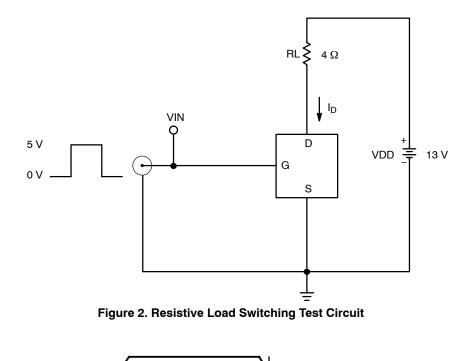


Figure 1. Voltage and Current Convention

4) V) V) (Note 6) 5, I <sub>D</sub> = 1 mA) V to V <sub>GS</sub> < 1 V) (Note 6)	V <sub>(BR)DSS</sub> I <sub>DSS</sub> I <sub>GSSF</sub> I <sub>GSSL</sub> V <sub>GS(th)</sub> V <sub>GS(th)</sub> /T <sub>J</sub> V <sub>LR</sub> t <sub>LR</sub>	42 40 43 - - - 1.0 - 0.8 10	46 45 47 0.6 2.5 25 440 1.7 5.0 1.4 40	51 51 5.0 10 50 - 2.2 - 1.9	ν           μA           μA           ν           ν           -mV/°C           ν
V) V) (Note 6) <sub>5</sub> , I <sub>D</sub> = 1 mA)	I <sub>DSS</sub> I <sub>GSSF</sub> I <sub>GSSL</sub> V <sub>GS(th)</sub> V <sub>GS(th)</sub> /T <sub>J</sub> V <sub>LR</sub>	40 43 - - - 1.0 - 0.8	45 47 0.6 2.5 25 440 1.7 5.0 1.4	51 51 5.0 10 50 - 2.2 - 1.9	μΑ μΑ μΑ V -mV/°C
V) (Note 6) <sub>3</sub> , I <sub>D</sub> = 1 mA)	IGSSF IGSSL VGS(th) VGS(th)/TJ VLR	- - 1.0 - 0.8	2.5 25 440 1.7 5.0 1.4	10 50 - 2.2 - 1.9	μΑ μΑ V -mV/°C
V) (Note 6) <sub>3</sub> , I <sub>D</sub> = 1 mA)	I <sub>GSSL</sub> V <sub>GS(th)</sub> V <sub>GS(th)</sub> /T <sub>J</sub> V <sub>LR</sub>	- 1.0 - 0.8	440 1.7 5.0 1.4	- 2.2 - 1.9	μA V -mV/°C
V) (Note 6) <sub>3</sub> , I <sub>D</sub> = 1 mA)	I <sub>GSSL</sub> V <sub>GS(th)</sub> V <sub>GS(th)</sub> /T <sub>J</sub> V <sub>LR</sub>	- 1.0 - 0.8	440 1.7 5.0 1.4	- 2.2 - 1.9	μA V -mV/°C
s, I <sub>D</sub> = 1 mA)	$\begin{array}{c} V_{GS(th)} \\ V_{GS(th)}/T_J \\ V_{LR} \end{array}$	1.0 - 0.8	1.7 5.0 1.4	- 1.9	V −mV/°C
	V <sub>GS(th)</sub> /T <sub>J</sub> V <sub>LR</sub>	- 0.8	5.0 1.4	- 1.9	-mV/°C
V to V <sub>GS</sub> < 1 V) (Note 6)	V <sub>GS(th)</sub> /T <sub>J</sub> V <sub>LR</sub>	0.8	1.4		,
V to V <sub>GS</sub> < 1 V) (Note 6)					V
V to V <sub>GS</sub> < 1 V) (Note 6)	t <sub>LR</sub>	10	40	100	
				100	μs
		-	25.5	-	kΩ
				•	
	R <sub>DS(on)</sub>		55 100	60 120	mΩ
I <sub>S</sub> = 7.0 A)	V <sub>SD</sub>	-	0.95	-	V
	t <sub>d(ON)</sub>		10	20	μs
	t <sub>r</sub>		20	40	-
$V_{GS}$ = 5 V, $V_{DS}$ = 13 V R <sub>L</sub> = 4 $\Omega$ , -40°C < T <sub>J</sub> < 150°C	t <sub>d(OFF)</sub>		30	60	
	t <sub>f</sub>		20	40	
	-dV <sub>DS</sub> /dt <sub>ON</sub>		0.5		V/µs
	dV <sub>DS</sub> /dt <sub>OFF</sub>		0.5		
unless otherwise noted) (	Note 5)				
Current Limit $V_{GS} = 5.0 \text{ V}, V_{DS} = 10 \text{ V}, T_J @ 25^{\circ}\text{C}$ $V_{GS} = 5.0 \text{ V}, V_{DS} = 10 \text{ V}, T_J = 150^{\circ}\text{C}$ (Note 6) $V_{GS} = 5.0 \text{ V}, V_{DS} = 10 \text{ V}, T_J = -40^{\circ}\text{C}$ (Note 6)		8 8 8	13 - -	16 18 16	A
V <sub>GS</sub> = 5.0 V V <sub>GS</sub> = 10 V	T <sub>LIM(off)</sub>	150 150	175 165	200 185	°C
unless otherwise noted)					
dy Model (HBM)	ESD	4000	-	-	V
odel (MM)	ESD	400	-	-	V
	= 5 V, $V_{DS}$ = 13 V 2, -40°C < T <sub>J</sub> < 150°C unless otherwise noted) ( $V_{GS}$ = 5.0 V $V_{GS}$ = 10 V unless otherwise noted) dy Model (HBM)	$I_{S} = 7.0 \text{ A})$ $V_{SD}$ $= 5 \text{ V}, \text{ V}_{DS} = 13 \text{ V}$ $\frac{t_{d}(\text{ON})}{t_{r}}$ $\frac{t_{d}(\text{OFF})}{t_{f}}$ $\frac{-d\text{V}_{DS}/dt_{ON}}{d\text{V}_{DS}/dt_{OFF}}$ unless otherwise noted) (Note 5) $I_{LIM}$ $V_{GS} = 5.0 \text{ V}$ $V_{GS} = 10 \text{ V}$ unless otherwise noted) $I_{LIM}$ $\frac{V_{GS} = 5.0 \text{ V}}{V_{GS} = 10 \text{ V}}$ $T_{LIM(off)}$ $U_{SD}$	$\begin{array}{c c c c c c c } & & & & & & & & & & & & & & & & & & &$	$\begin{array}{ c c c c c } & - & 55 \\ 100 \\ \hline I_S = 7.0 \text{ A} \end{pmatrix} & V_{SD} & - & 0.95 \\ \hline I_S = 7.0 \text{ A} \end{pmatrix} & V_{SD} & - & 0.95 \\ \hline I_S = 7.0 \text{ A} \end{pmatrix} & V_{SD} & - & 0.95 \\ \hline I_S = 7.0 \text{ A} \end{pmatrix} & V_{SD} & - & 0.95 \\ \hline I_S = 5 \text{ V}, \text{ V}_{DS} = 13 \text{ V} & 10 \\ \hline t_r & 20 \\ \hline t_d(\text{OFF}) & 30 \\ \hline t_f & 20 \\ \hline -dV_{DS}/dt_{ON} & 0.5 \\ \hline dV_{DS}/dt_{OFF} & 0.5 \\ \hline unless otherwise noted) (\text{Note 5}) \\ \hline & I_{LIM} & 8 \\ 8 \\ - \\ \hline V_{GS} = 5.0 \text{ V} \\ V_{GS} = 10 \text{ V} & T_{LIM(off)} & 150 \\ \hline 150 \\ 165 \\ \hline unless otherwise noted) \\ \hline & U_{M}(off) & 150 \\ \hline 150 \\ \hline 165 \\ \hline unless otherwise noted) \\ \hline \hline unless otherwise noted \\ \hline unless otherwise noted \\ \hline \hline unless otherwise noted \\ \hline unless otherwise noted \\ \hline unless otherwise noted \\ \hline unless otherwise nother$	$\begin{array}{ c c c c c c } & - & 55 & 60 \\ \hline & 100 & 120 \\ \hline & 120 \\ \hline \\ I_S = 7.0 \text{ A}) & V_{SD} & - & 0.95 & - \\ \hline & & & & & \\ \hline & & & & & \\ \hline & & & &$

Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.
 Fault conditions are viewed as beyond the normal operating range of the part.
 Not subject to production testing.

# TEST CIRCUITS AND WAVEFORMS



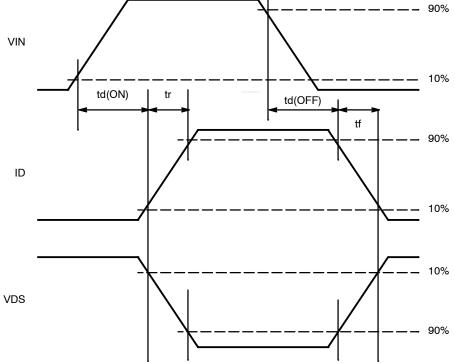


Figure 3. Resistive Load Switching Waveforms

### **TEST CIRCUITS AND WAVEFORMS**

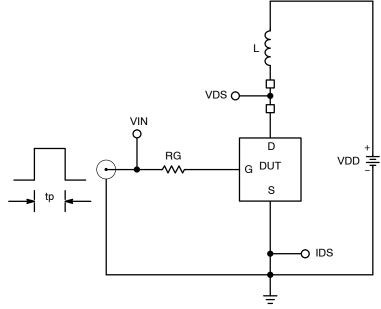


Figure 4. Inductive Load Switching Test Circuit

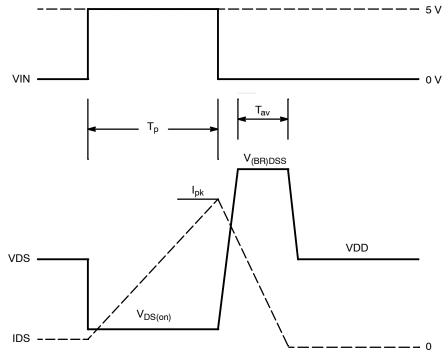
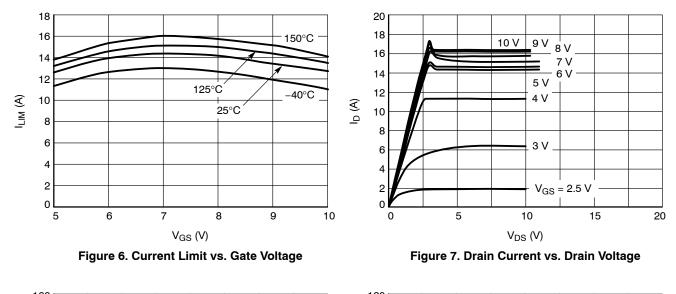
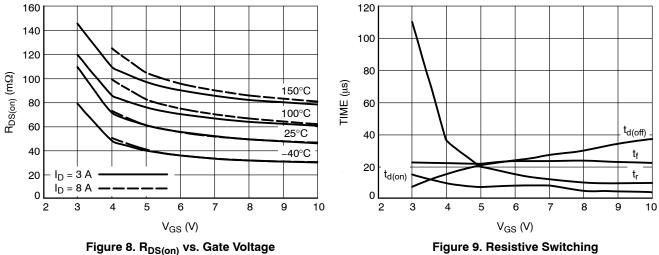


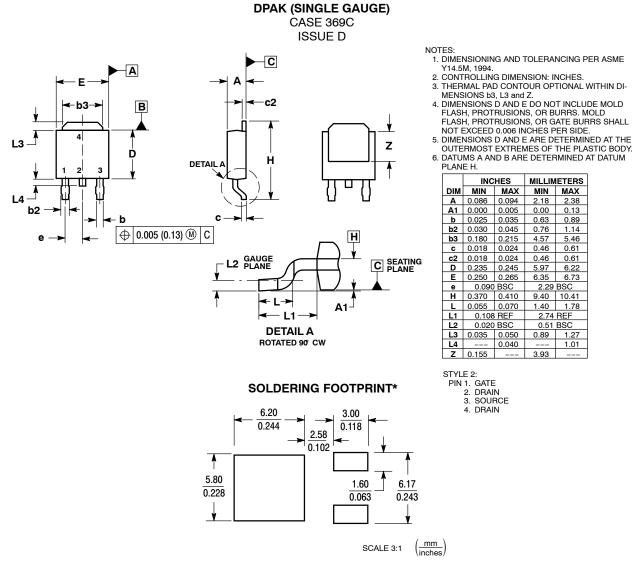
Figure 5. Inductive Load Switching Waveforms

### **TYPICAL CHARACTERISTICS**





#### PACKAGE DIMENSIONS



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and 💷 are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. Al listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without imitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and to vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

#### PUBLICATION ORDERING INFORMATION

#### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor P.O. Box 5163, Denver, Colorado 80217 USA Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

ON Semiconductor Website: www.onsemi.com Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local

MILLIMETERS

2.18

0.00

0.63

0.76

4.57

0 46

0.46

5.97

6.35

1.40 1.78 2.74 REF

0.89

3.93

2.29 BSC 9.40 10.41

0.51 BSC

2.38

0.13

0.89

1.14

5.46

0.61

0.61

6.22

6.73

1.27

1.01

Europe, Middle East and Africa Technical Support:

Phone: 421 33 790 2910 Japan Customer Focus Center Phone: 81-3-5817-1050

Sales Representative