Integrated Device Technology, Inc.

CMOS STATIC RAM 32K x 16-BIT

PRELIMINARY IDT71008

FEATURES:

- 32K x 16 advanced high-speed CMOS Static RAM
- Equal access and cycle times
  - — Commercial: 10/12/15/20ns
- One Chip Select plus one Output Enable pin
- Bidirectional data inputs and outputs directly TTL-compatible
- Low power consumption via chip deselect
- Upper and Lower Byte Enable Pins
- Available in 44-pin Plastic SOJ package and 44-pin TSOP package

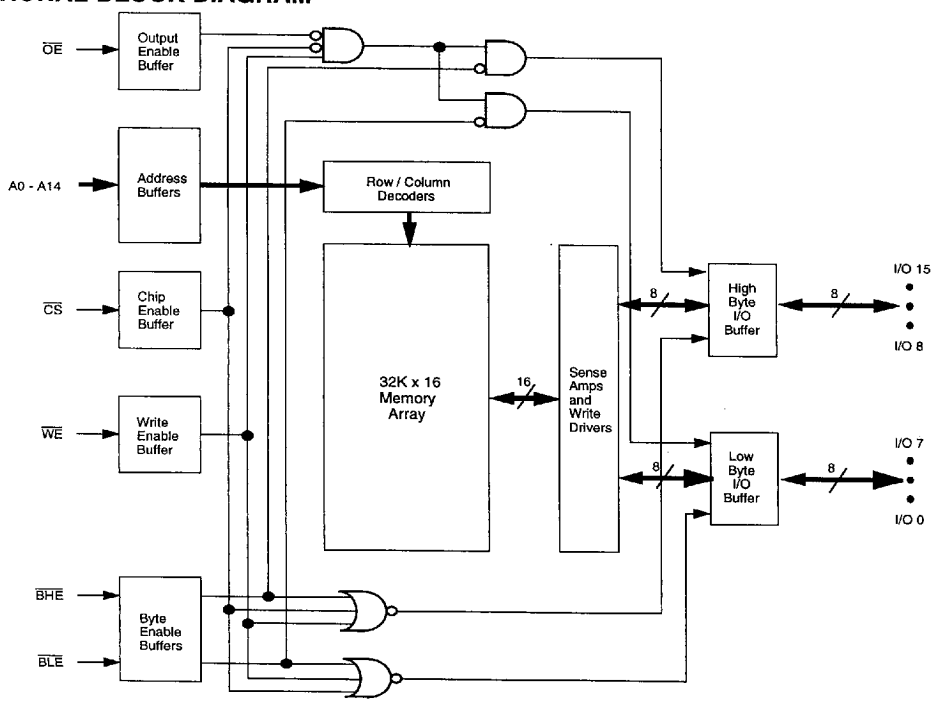
DESCRIPTION:

The IDT71008 is a 524,288-bit high-speed Static RAM organized as 32K x 16. It is fabricated using IDT's high-perfomance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

The IDT71008 has an output enable pin which operates as fast as 5ns, with address access times as fast as 12ns. All bidirectional inputs and outputs of the IDT71008 are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used, requiring no clocks or refresh for operation.

The IDT71008 is packaged in a JEDEC standard 44-pin Plastic SOJ and 44-pin TSOP Type II.

FUNCTIONAL BLOCK DIAGRAM



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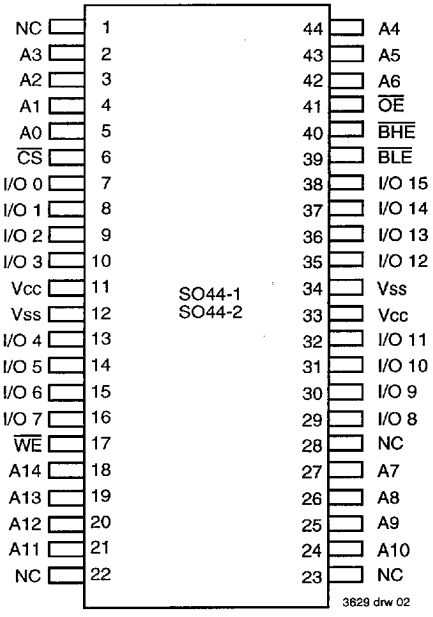
PIN CONFIGURATIONS



SOJ/TSOP
TOP VIEW

PIN DESCRIPTIONS

$A_0 - A_{14}$	Address Inputs	Input
$\overline{CS}$	Chip Select	Input
$\overline{WE}$	Write Enable	Input
$\overline{OE}$	Output Enable	Input
$\overline{BHE}$	High Byte Enable	Input
$\overline{BLE}$	Low Byte Enable	Input
$I/O_0 - I/O_{15}$	Data Input/Output	I/O
Vcc	5.0V Power	Pwr
Vss	Ground	Gnd

3629 tbl 01

TRUTH TABLE(1)

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O_0-I/O_7	I/O_8-I/O_{15}	Function
H	X	X	X	X	High-Z	High-Z	Deselected - Standby
L	L	H	L	H	$DATA_{OUT}$	High-Z	Low Byte Read
L	L	H	H	L	High-Z	$DATA_{OUT}$	High Byte Read
L	L	H	L	L	$DATA_{OUT}$	$DATA_{OUT}$	Word Read
L	X	L	L	L	$DATA_{IN}$	$DATA_{IN}$	Word Write
L	X	L	L	H	$DATA_{IN}$	High-Z	Low Byte Write
L	X	L	H	L	High-Z	$DATA_{IN}$	High Byte Write
L	H	H	X	X	High-Z	High-Z	Outputs Disabled
L	X	X	H	H	High-Z	High-Z	Outputs Disabled

NOTE:
1.H = V_{IH}, L = V_{IL}, X = Don't care.

3629 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	V_{CC}+0.5	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE:

3629 tbl 03

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	OperatingTemperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTES:

3629 tbl 04

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} + 0.5V.

CAPACITANCE

(T_A = +25°C, f = 1.0MHz, TSOP Type II package)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	6	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

NOTE:

3629 tbl 05

1. This parameter is guaranteed by device characterization, but not production tested.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%, Commercial Temperature Range

Symbol	Parameter	Test Condition	IDT71008 Min.	IDT71008 Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V

3629 tbl 06

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC}–0.2V)

Symbol	Parameter	71008S10 Com'l.	71008S10 Mil.	71008S12 Com'l.	71008S12 Mil.	71008S15 Com'l.	71008S15 Mil.	71008S20 Com'l.	71008S20 Mil.	Unit
I_{CC}	Dynamic Operating Current $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	220	—	200	—	180	—	170	—	mA
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \ge V_{IH}$, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	55	—	50	—	45	—	40	—	mA
I_{SB1}	Standby Power Supply Current (CMOS Level) $\overline{CS} \ge V_{HC}$, Outputs Open, V_{CC} = Max., f = 0[2] $V_{IN} \le V_{LC}$ or $V_{IN} \ge V_{HC}$	10	—	10	—	10	—	10	—	mA

NOTES:

3629 tbl 07

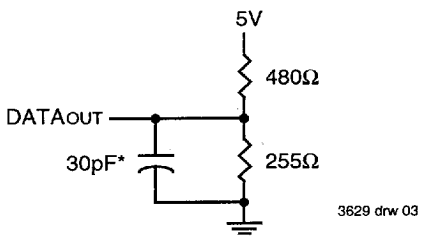
1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1.5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1, 2, and 3

3629 tbl 07

AC TEST LOADS



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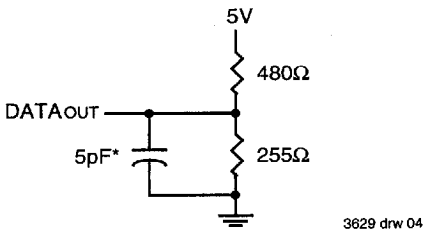

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*Including jig and scope capacitance.

Figure 1. AC Test Load

Figure 2. AC Test Load (for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, and t_{WHZ})

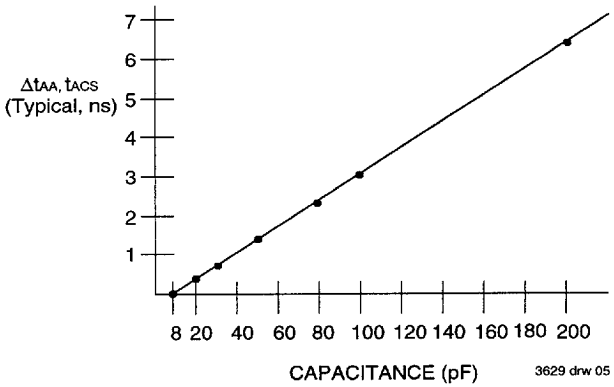

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Figure 3. Output Capacitive Derating

AC ELECTRICAL CHARACTERISTICS (VCC = 5.0V ± 10%, Commercial Temperature Range)

Symbol	Parameter	71008S10		71008S12		71008S15		71008S20		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
tRC	Read Cycle Time	10	—	12	—	15	—	20	—	ns
tAA	Address Access Time	—	10	—	12	—	15	—	20	ns
tACS	Chip Select Access Time	—	10	—	12	—	15	—	20	ns
tCLZ(1)	Chip Select Low to Output in Low-Z	3	—	3	—	3	—	3	—	ns
tCHZ(1)	Chip Select High to Output in High-Z	—	5	—	6	—	8	—	9	ns
tOE	Output Enable Low to Output Valid	—	5	—	6	—	8	—	9	ns
tOLZ(1)	Output Enable Low to Output in Low-Z	0	—	0	—	0	—	0	—	ns
tOHZ(1)	Output Enable High to Output in High-Z	—	5	—	3	—	5	—	9	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
tBE	Byte Enable Low to Output Valid	—	5	—	6	—	8	—	9	ns
tBLZ(1)	Byte Enable Low to Output in Low-Z	0	—	0	—	0	—	0	—	ns
tBHZ(1)	Byte Enable High to Output in High-Z	—	5	—	6	—	8	—	9	ns
Write Cycle										
tWC	Write Cycle Time	10	—	12	—	15	—	20	—	ns
tAW	Address Valid to End of Write	7	—	8	—	10	—	12	—	ns
tCW	Chip Select Low to End of Write	7	—	8	—	10	—	12	—	ns
tBW	Byte Enable Low to End of Write	7	—	8	—	10	—	12	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWR	Address Hold from End of Write	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	7	—	8	—	10	—	12	—	ns
tDW	Data Valid to End of Write	6	—	7	—	8	—	10	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	ns
tOW(1)	Write Enable High to Output in Low-Z	1	—	1	—	1	—	1	—	ns
tWHZ(1)	Write Enable Low to Output in High-Z	—	5	—	6	—	8	—	9	ns

NOTE:
1. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

3629 tbl 08

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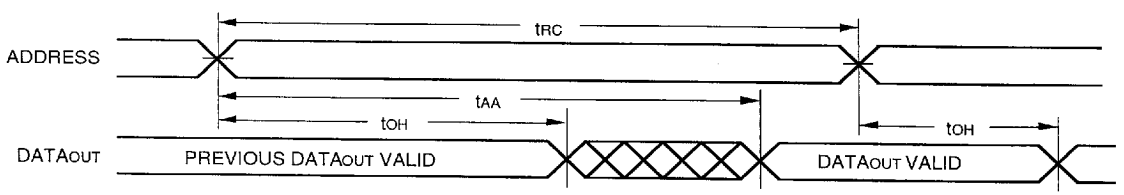
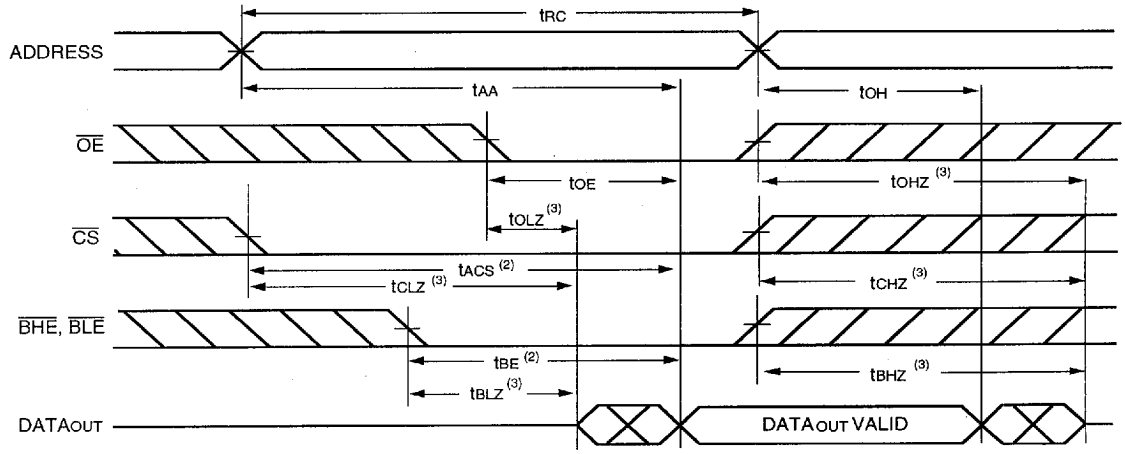
TIMING WAVEFORM OF READ CYCLE NO. 1(1,2,3)



3629 drw 06

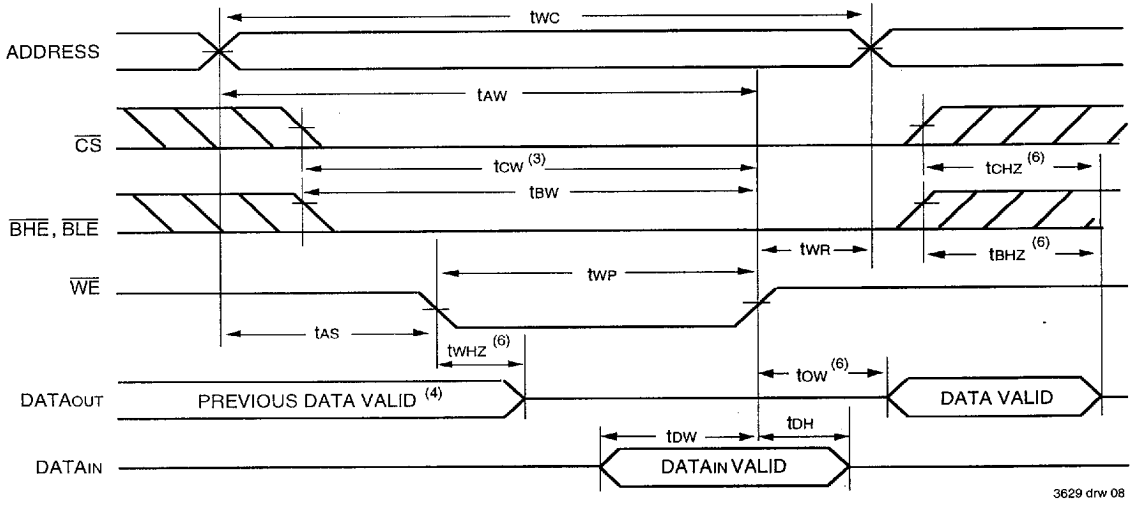
NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. $\overline{OE}$, $\overline{BHE}$, and $\overline{BLE}$ are LOW.

TIMING WAVEFORM OF READ CYCLE NO. 2(1)



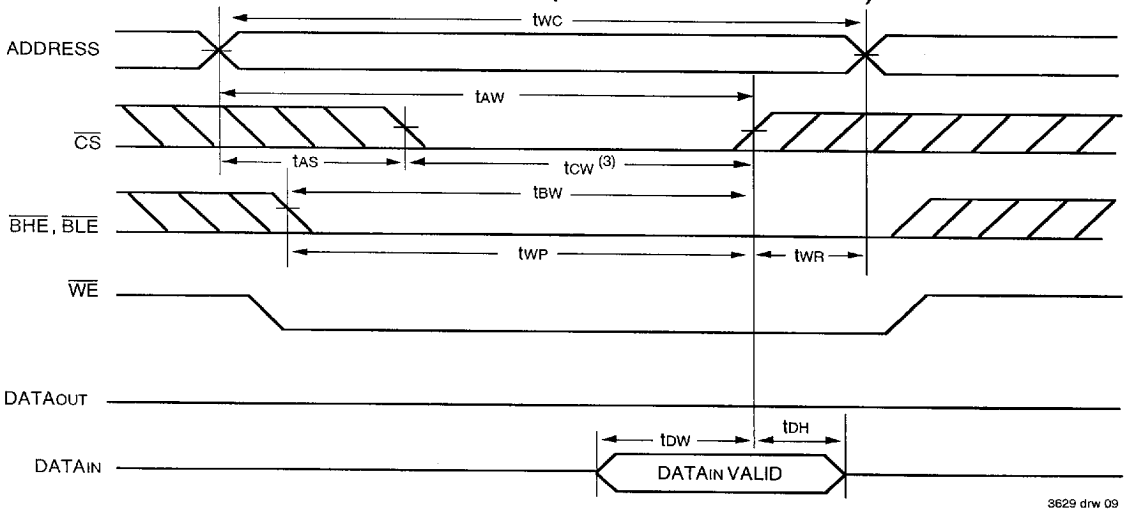
NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Address must be valid prior to or coincident with the later of $\overline{CS}$, $\overline{BHE}$, or $\overline{BLE}$ transition LOW; otherwise t_{AA} is the limiting parameter.
3. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1,2,3,5)

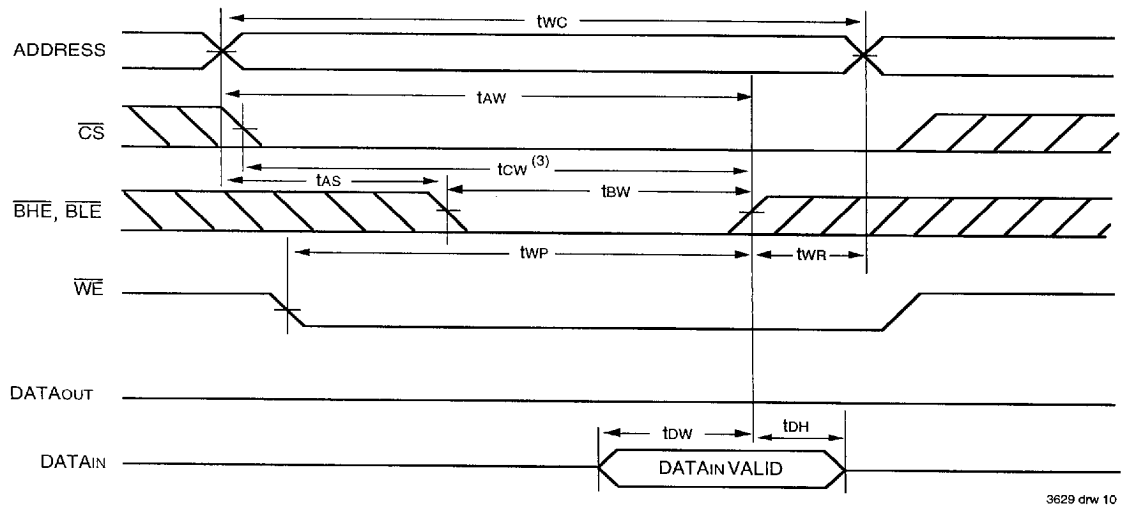


NOTES:
1. $\overline{WE}$, $\overline{BHE}$ and $\overline{BLE}$, or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$, LOW $\overline{BHE}$ or $\overline{BLE}$, and a LOW $\overline{WE}$.
3. $\overline{OE}$ is continuously HIGH. If during a $\overline{WE}$ controlled write cycle $\overline{OE}$ is LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified t_{WP}.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ LOW or $\overline{BHE}$ and $\overline{BLE}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1,2,5)



TIMING WAVEFORM OF WRITE CYCLE NO. 3 ($\overline{BHE}$, $\overline{BLE}$ CONTROLLED TIMING)(1,2,5)



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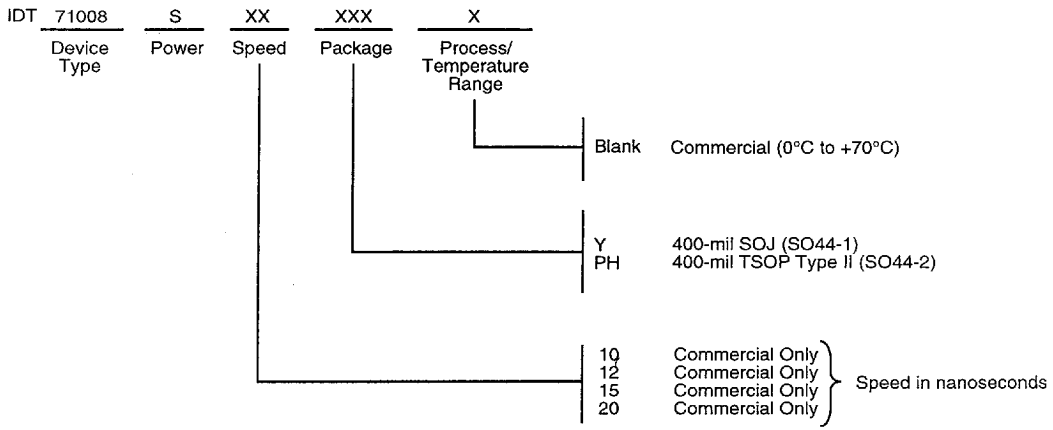
NOTES:
1. $\overline{WE}$, $\overline{BHE}$ and $\overline{BLE}$, or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$, LOW $\overline{BHE}$ or $\overline{BLE}$, and a LOW $\overline{WE}$.
3. $\overline{OE}$ is continuously HIGH. If during a $\overline{WE}$ controlled write cycle $\overline{OE}$ is LOW, tWP must be greater than or equal to tWHZ + tDW to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified tWP.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ LOW or $\overline{BHE}$ and $\overline{BLE}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured ±200mV from steady state.

ORDERING INFORMATION



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