MagnaChip *Confidential*

CMOS Image Sensor
with Image Signal Processing

HV7161SPA2
1.3 Mega Pixel CIS
(15fps@MCLK 21MHz, PLL 2x)

Preliminary

V3.0

Revision History

Revision	Script Date	Comments
V0.0	2003/11/19/Wed.	1.3Mega Pixel CIS Preliminary is released
V0.1	2004/03/19/Fri.	Some descriptions are corrected
V0.2	2004/04/01/Wed.	Some PLL registers are changed. Some descriptions are simplified.
V0.3	2004/04/06/Tue.	Pin diagram is corrected and some analog registers are removed.
V0.4	2004/04/23/Fri.	Frame timing and integration time are corrected.
V0.5	2004/06/03/Thu.	Window mode and image size are corrected.
V0.6	2004/07/20/Tue.	Fixed frame rate
V0.7	2004/08/06/Fri.	PCTRB, Anti-Banding Mode
V2.0	2004/08/12/Thu.	1st full revision Device ID, Focus value, window mode, and image size
V2.1	2004/08/27/Fri.	CLCC Package Drawing added AWB Red/Blue Gain Maximum/Minimum Value
V2.2	2004/09/17/Fri.	Typical application, pin description, and pin function
V2.3	2004/09/20/Mon.	Some register bits corrected and video mode setting modified.
V2.4	2004/10/25/Tue.	Bayer 11bit enable(OUTFMT[31h])
V2.5	2004/12/23/Thu.	* Output data according to video mode (page 54) * Pin diagram(symbol VDD:P and VDD:PH), * AC/DC characteristics (symbol and typical voltage condition), and electro-optical characteristics (description) changed. QCIF mode removed. * All 2.5V power supplies are changed to '2.5V to 2.8V'.
V2.6	2005/01/04/Tue.	DC Operating Conditions, Electro-Optical Characteristics and Condition
V3.0	2005/01/20/Thu.	2nd full revision Noise filter, Focal value generator, Contrast, Digital controlled analog gain calibration, and QCIF

Copyright by MagnaChip Semiconductor Ltd., all right reserved 2005

Disclaimer

This document has general product descriptions and is subject to change without any notice. MagnaChip Semiconductor Ltd., assumes no responsibility on using of circuit described. Also, no patent licenses are implied.

# Contents

General Description

1.3Mega pixel CIS is a highly integrated single chip CMOS color image sensor implemented by proprietary MagnaChip 0.18um CMOS sensor process realizing high sensitivity and wide dynamic range. Total active pixel array is 1.3Mega size. Each active pixel composed of 4 transistors has a micro-lens to enhance sensitivity, and converts photon energy to analog pixel voltage. On-chip 11bit Analog to Digital Converter (ADC) digitizes analog pixel voltage, and on-chip Correlated Double Sampling (CDS) scheme reduces Fixed Pattern Noise (FPN) dramatically. General image processing functions are implemented to diversify its applications, and various output formats are supported for the sensor to easily interface with different video codec chips. The integration of sensor function and image processing functions make 1.3Mega pixel CIS especially very suitable for mobile imaging systems such as digital still camera, PC input camera and IMT-2000 phone's video part that requires very low power and system compactness.

Features

- Optical format   1/3.7 inch
- Total pixel array   1298 x 982
- Active window pixel array   1280 x 960
- Optical black array   Upper: 2-line, Lower: 2-line
- Pixel size   3.2μm x 3.2μm
- Color filter array   RGB mosaic
- Micro-lens for high sensitivity and on-chip 11 bit ADC
- Correlated double sampling (CDS) for reduction of Fixed Pattern Noise (FPN)
- Auto Black Level Compensation (ABLC) for reduction of the dark signal
- Gamma correction by programmable piecewise linear approximation
- Optimized color interpolation, false color suppression, and edge enhancement
- Adaptive random noise filter
- Color correction by programmable 3x3 matrix operation
- Color space conversion from RGB to YCbCr or YUV
- Sub-sampling modes : 1/4(VGA), 1/16(QVGA), 4CIF, CIF, and QCIF
- Various output formats: CCIR-601, CCIR-656 Compatible
                              YCbCr 4:2:2, YCbCr 4:4:4, RGB 4:4:4, RGB5:6:5
                              8bit and 11bit Bayer raw
- 8bit/16bit Data Bus Mode
- Support fixed-frame rate mode and single shot mode
- Automatic Exposure control(AE) and Automatic White Balance control(AWB)
- Special image functions: hue, saturation, brightness, contrast, negative, sepia, gray, and mono.
- Focus value generation from image information for supporting auto focus function
- Hard and soft power save mode
- Typical supply voltage: Internal 1.8V and 2.5V to 2.8V, and I/O 2.5V to 2.8V
- Operation Temperature : -10 ~ +50 degrees Celsius
- Package Types: CLCC 48 PIN, COB(Chip-on-Board), COF(Chip-on-Flex)
- Internal wide-range PLL
- Frame Rate: 15fps at MCLK 21MHz and PLL 2x mode, or fixed frame rate supported.

- Total power consumption : about 73mW

Pixel Array Structure
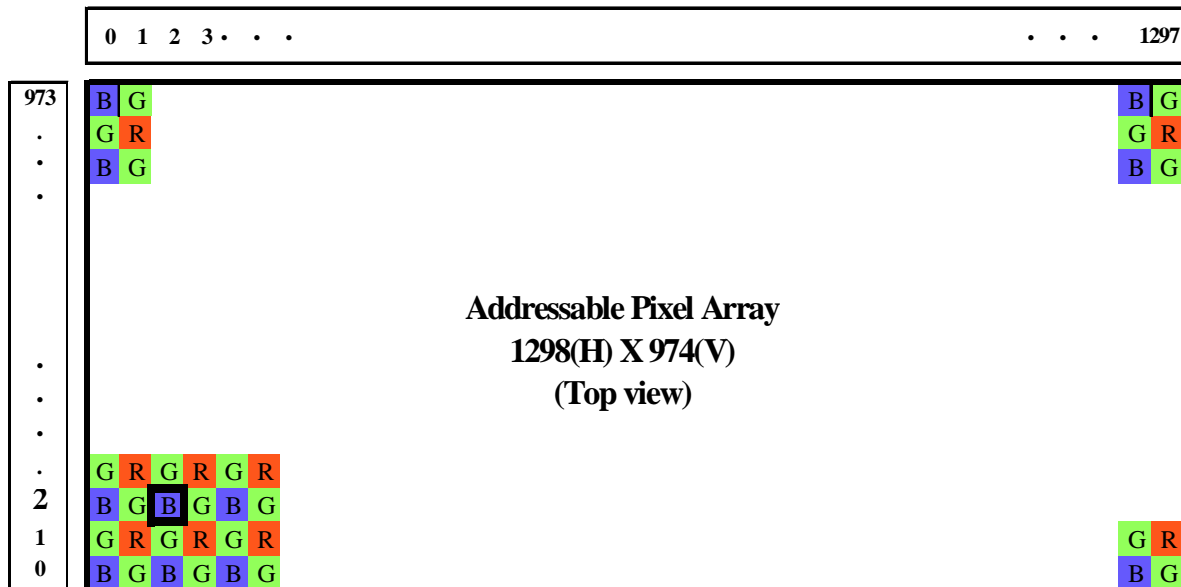
Block Diagram
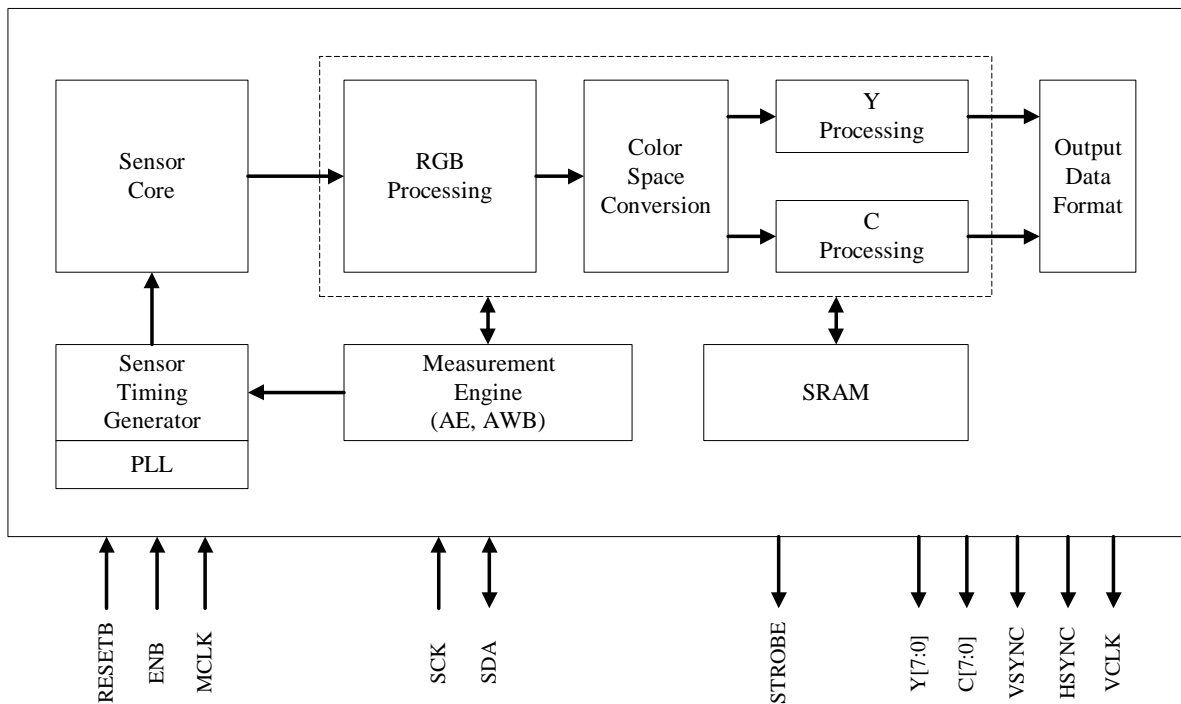
MagnaChip *Confidential*

Pin Diagram (CLCC 48LD)

Pin Description (CLCC 48LD)

※ C[7:0] should be set up as pull-up or pull-down when 8bit output mode is used.

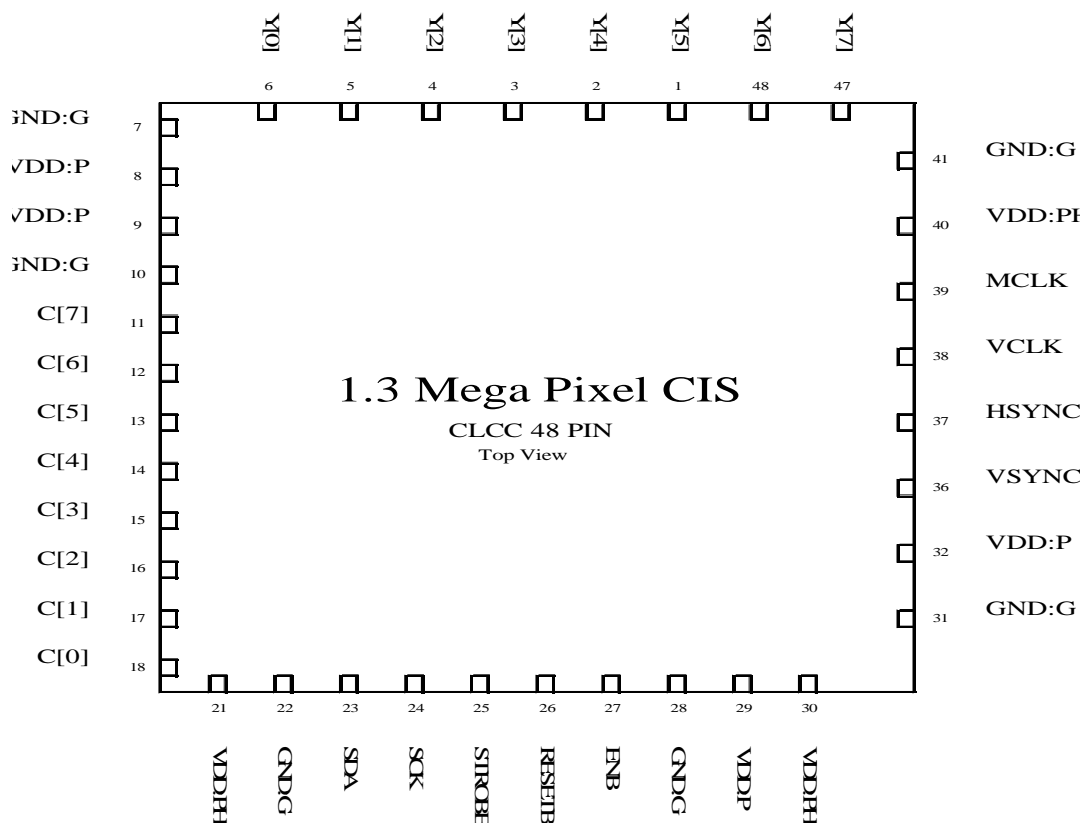| Pin	Type	Symbol	Description
47-48, 1-6	B	Y[7:0]	Video luminance data
7	G	DGNDI	Digital ground for I/O driver
8	P	DVDDI	1.8V digital power for I/O driver
9	P	DVDDC	1.8V power for internal digital block
10	G	DGNDC	Ground for internal digital block
11-18	O	C[7:0]	Video chrominance data
21	PH	DVDDIH	2.5V to 2.8V digital power for I/O driver
22	G	DGNDIH	Digital ground for I/O Driver
23	B	SDA	I2C standard data I/O port
24	I	SCK	I2C clock input
25	O	STROBE	Strobe signal output
26	I	RESETB	Sensor reset. Active low
27	I	ENB	Sensor sleep mode is controlled externally by this pin when

This document has a general product description and is subject to change without notice. MagnaChip Semiconductor Ltd. does not assume any responsibility for use of circuits described and no patent licenses are implied.

			sleep mode register bit SCTRB[4] is low. ENB low : sleep mode, ENB high : normal mode
28	G	DGNDI	Digital ground for I/O driver
29	P	DVDDI	1.8V digital power for I/O driver
30	PH	AVDDPH	2.5V to 2.8V analog power for pixel block
31	G	AGNDC	Analog ground for analog block
32	P	AVDDC	1.8V analog power for analog block
36	O	VSYNC	Video frame synchronization signal. VSYNC is active at start of image data frame.
37	O	HSYNC	Video horizontal line synchronization signal. Image data is valid, when HSYNC is high.
38	O	VCLK	Video output clock
39	I	MCLK	Master input clock
40	PH	DVDDIH	2.5V to 2.8V digital power for I/O driver
41	G	DGNDI	Digital ground for I/O driver

※ Pins 19-20, 33-35, 42-46 are not connected.

※ Pin function:　　B - CMOS Schmitt trigger, non-inverted, tri-state bidirectional buffer, 4mA drive

I - CMOS Schmitt trigger level non-inverting input

O - Tri-state non-inverting output, 4mA drive (VCLK - 8mA drive)

PH - 2.5V to 2.8V I/O or pixel power, P - 1.8V digital or analog power

G - Universal ground

MagnaChip *Confidential*

Pin Function

System power supply

DVDDC   1.8V power supply for the internal digital circuit.

AVDDC   1.8V power supply for the internal analog circuit. Separate properly from digital power, I/O power and signals.

DVDDI   1.8V I/O power supply for the input/output/bidirectional pad.

AVDDPH   2.5V to 2.8V power supply for the internal pixel array. Separate properly from digital power, I/O power and signals.

DVDDIH   2.5V to 2.8V power supply for the input/output/bidirectional pad.

※ **Note :** Attach a bypass capacitor near each power pin.

System ground

DGNDC   1.8V ground for the internal digital circuit.

AGNDC   1.8V or 2.5V to 2.8V ground for the internal analog circuit. Separate properly from digital power, I/O power and signals.

DGNDI   1.8V ground for the input/output/bidirectional pad.

DGNDIH   2.5V to 2.8V ground for the input/output/bidirectional pad.

Input pins

RESETB   When RESETB pin is an active low input, an external reset is generated. And all internal registers are initialized and are loaded by each default value. It is required that reset period is holding for more than 4 MCLK clocks when ENB pin is high level. Shorter period is not guaranteed to produce a reset scheme and make a sensor be unstably operated. Active low RESETB pin generates all output pins except VCLK pin to low level. VCLK pin is not affected to RESETB pin.

ENB   When ENB pin is an active high input, all functions of a sensor can be normally operated and so all output data are valid. If ENB pin is a low level, a sensor enters into a sleep mode and all functions are suspended. And all output pins hold each previous value. Sleep mode register SCTRB[4] bit means a soft-power down and ENB pin means a hard-power down. After RESETB pin is changed from a low to a high level, ENB pin should be changed from a low to a high level. At the external (ENB) power-down mode, all output and bidirectional pins have a state of Hi-Z (high impedance). In addition to power-down mode, Y[7:0] and C[7:0] pins have a state of Hi-Z during HSYNC pin is low level. To minimize a power consumption at the external hard power-down mode (by ENB pin), the sensor's main power should be turned off together.

MCLK   MCLK pin is a master clock of sensor and determines maximum frame rate. This pin generates video clock (VCLK) and is supplied from an external clock oscillator. Between the external clock oscillator and MCLK pin should be as near as possible.

SCK   SCK is an input pin to be supplied I2C bus clock from master device and sensor get to be a slave device. SCK clock frequency is able up to maximum

400KHz. With SDA pin, SCK timing should satisfy the standard I2C bus timing.

Output pins

Y[7:0]   Video luminance output is available only when VSYNC and HSYNC is active state, which VSYNC is low and HSYNC is high level. Data output is generated sequentially whenever VCLK is triggered from low to high level. So, you must capture the image data whenever VCLK is triggered from high to low level. If HSYNC is got to inactive state, each Y pin generates high-impedance output - necessary when an imaging system including sensor uses the common-bus mode. The first image data is normally BLUE color in the case of Bayer output mode, and LUMINANCE, YCbCr output mode. In power-down mode, Y[7:0] pins have a state of Hi-Z during HSYNC pin is low level.

C[7:0]   With data bus mode set to RGB 4:4:4-16bit output or YCbCr 4:4:4-16bit output, video chrominance output is available only when VSYNC and HSYNC is active state, that VSYNC is low and HSYNC is high level (Otherwise, with 8bit data output mode, C pin always goes to high-impedance output mode). Data output is generated sequentially whenever VCLK is triggered from low to high level. So, you must capture the image data whenever VCLK is triggered from high to low level. If HSYNC is got to inactive state, each Y pin generates high-impedance output - necessary when an imaging system including sensor uses the common-bus mode. In power-down mode, C[7:0] pins have a state of Hi-Z during HSYNC pin is low level.

VCLK   Video clock is always generated while sensor is being active operation. When HSYNC is active high, video clock has pulse count as a pixel amount corresponding to 1-line of specific image window. Data output is generated sequentially whenever VCLK is triggered from low to high level. So, you must capture the image data whenever VCLK is triggered from high to low level. When VSYNC is low and HSYNC is high level, total VCLK pulse count is equal to a total pixel amount of specific image window.

※ **Note :** With OUTINV[0] set to '1', valid data is generated when VCLK is trigged from high to low level, and you can capture the image data when VCLK is trigged from low to high level.

HSYNC   Image data is valid, when HSYNC is high

VSYNC   VSYNC is active at start of image data frame.

STROBE   Though sensor has enough integration time to capture image,   sensor can't obtain good image quality in dark environment. For this situation, sensor can generate strobe signal for driving external strobe circuit. The strobe output is active high when integration time is over than core frame time((Video Height Time + 1) X (Video   Width Time + HBLANK)). Because sensor uses progressive exposure method, strobe signal should cover all line(all pixels).

※ **Note :** If a sensor is got into hard or soft sleep mode, all output pins generate high-impedance output - necessary when an imaging system including sensor uses the common-bus mode.

Bi-directional

SDA SDA is the Serial Data line. The data on the SDA line must be stable during the HIGH period of the SCK clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCK line is LOW. Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first**.**

Functional Description

Reset sequence

Internal power –on reset (POR) Sensor resets automatically by internal power-on reset circuit when power is supplied, and after 1 frame operation is done, all reset sequence is terminated as all internal registers are loaded to each default value, and sensor is stable. Therefore, image capturing or chip configuring should be executed on 1 frame time later from power-on.

External reset When RESETB pin goes from high to low level, initialization is begun. After 1 frame operation is done, all reset sequence is terminated as all internal registers are loaded to each default value, and sensor is stable. Therefore, image capturing or chip configuring should be executed on 1 frame time later from external reset. We recommend initializing sensor by using RESETB pin before operating it. The condition to reset sensor follow,
1. MCLK is being supplied to sensor.
2. ENB pin is holding '1' and RESETB pin is '1'.
3. RESETB pin have to be keep '0' during minimum 4MCLK periods.
4. After RESETB pin set to '1' and 1 frame time is gone, reset sequence is terminated.
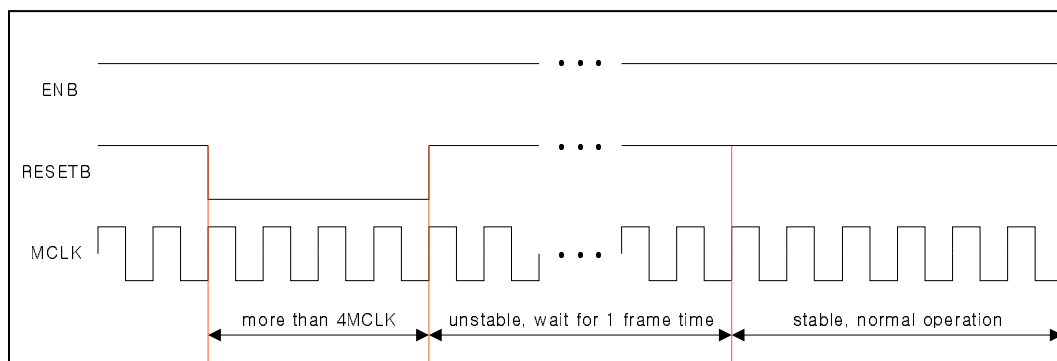
Power-down mode

Internal soft power-down For entering into soft power-down mode, set SCTRB[4] to '1'. In this mode, all internal digital and analog blocks go into an inactive mode(soft sleep), and power

consumption is decreased considerably.

※Note: You should set the integration time to multiple of AE-Step before waking power-down mode. This is because the default integration time and integration scan offset are set to multiples of 50Hz. If you leave out Integration time setting step, the banding under fluorescent light will be occurred even though other AE related registers are set appropriately. The setting order is follow,

1. Enter into the soft power-down mode.
2. Set the AE step (minimum frame rate).
3. Set the integration time to 4 times of AE step.
4. Wake the soft power-down mode.

External hard power-down   During ENB pin is '0', sensor goes to a deep-sleep mode(hard power-down mode) and all sensor operation is stopped. Also power consumption is minimized dramatically. After ENB pin goes from low to high level and 1 frame operation is done, sensor operation is stable and you can capture image data and configure each specific register. The sensor reset and hard power-down scheme   follows,
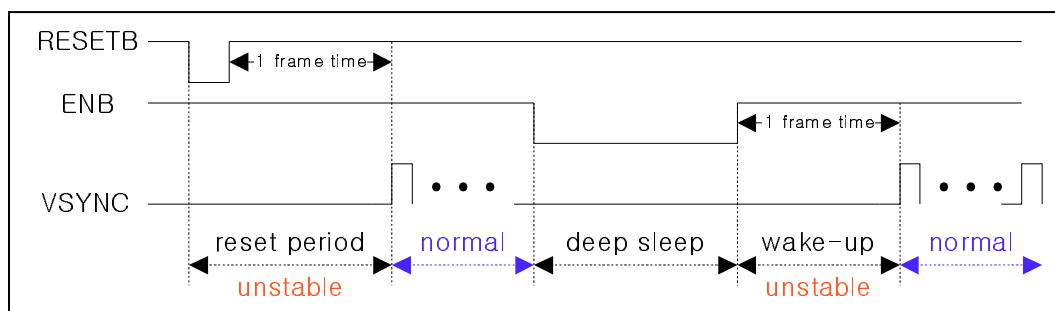
※Note: In the internal(I2C control) or external(ENB) power-down mode, all output and bidirectional pins have a state of Hi-Z(high impedance). In addition to power-down mode, Y[7:0] and C[7:0] pins have a state of Hi-Z during HSYNC pin is low level.

※Note: To minimize a power consumption at the external hard power-down mode(by ENB pin), the sensor's main power should be turned off together.

Pixel Architecture

Pixel architecture is a 4 transistor NMOS pixel design. The additional use of a dedicated transfer transistor in the architecture reduces most of reset level noise so that fixed pattern noise is not visible. Furthermore, micro-lens is placed upon each pixel in order to increase fill factor so that high pixel sensitivity is achieved.

Sensor Imaging Operation

Imaging operation is implemented by the offset mechanism of integration domain and scan domain(rolling shutter scheme). First integration plane is initiated, and after the programmed integration time is elapsed, scan plane is initiated, then image data start being produced.

Time

Integration plane frame 0		Integration time
Integration plane frame 1	Scan plane frame 0	Frame 0 time
	Scan plane frame 1	Frame 1 time
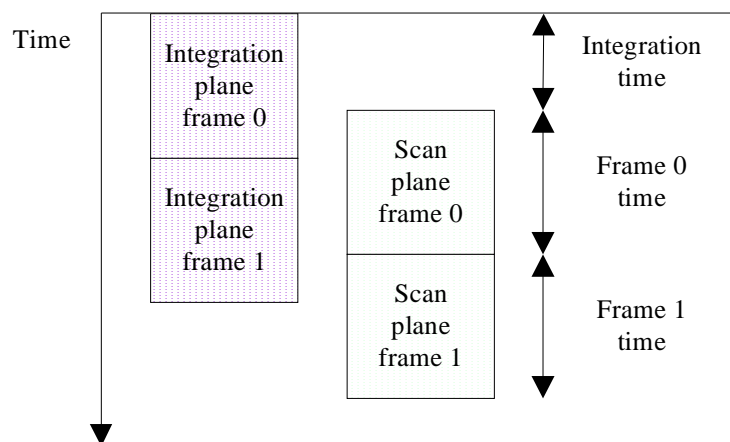
Correlated Double Sampling(CDS) and Programmable Gain Amplifier(PGA)

Correlated double sampling is a circuit for reducing any correlated noise between reset signal and video data signal. First, reset signal is taken and held at the reset sampler. Second, video signal is taken and held at the data sampler. Final, these two signal is subtracted to null any common signal(fixed pattern noise), and thereby the correlated noise that exits at both the reset signal and video signal is minimized.

The above subtracted video signal is properly scaled by each R, G, and B programmable gain amplifier and sequentially transmitted from PGA to ADC via the serial line. The amplifier's gain is mutually controlled by auto-exposure control function(AE) and auto-white balance control function(AWB). Any internal offset or noise within the amplifier is removed by internal offset elimination circuit. The scaling range of pre-amplifier for AE is from 0.5X to 16.5X, and the scaling range of color-amplifier for AWB is from 0.5X to 3.5X.

11bit on-chip ADC

On-chip ADC converts analog pixel voltage to 11bit digital data. On-chip ADC has a low power, a high resolution, and a high conversion speed to be suitable at an imaging system. Internally, to null the parasitic offset and the fixed pattern noise of pixel, on-chip ADC has an offset adjustment circuit. Also, to increase the conversion rate on-chip ADC has a bias control circuit.

Dark Noise Cancellation(DNC)

When an interesting center pixel has abnormally large value (decided to the 'dark noise') the center pixel is corrected by using neighbor pixels.

Gamma Correction

Piecewise linear approximation method is implemented. Ten-piece linear segments are supported and user-programmable.

MagnaChip *Confidential*

OUT

255
pt9
pt8

pt7
pt6
pt5

pt4

pt3

pt2

pt1
pt0

IN

8 32 64 128   256 384 512   1024   1536   2047
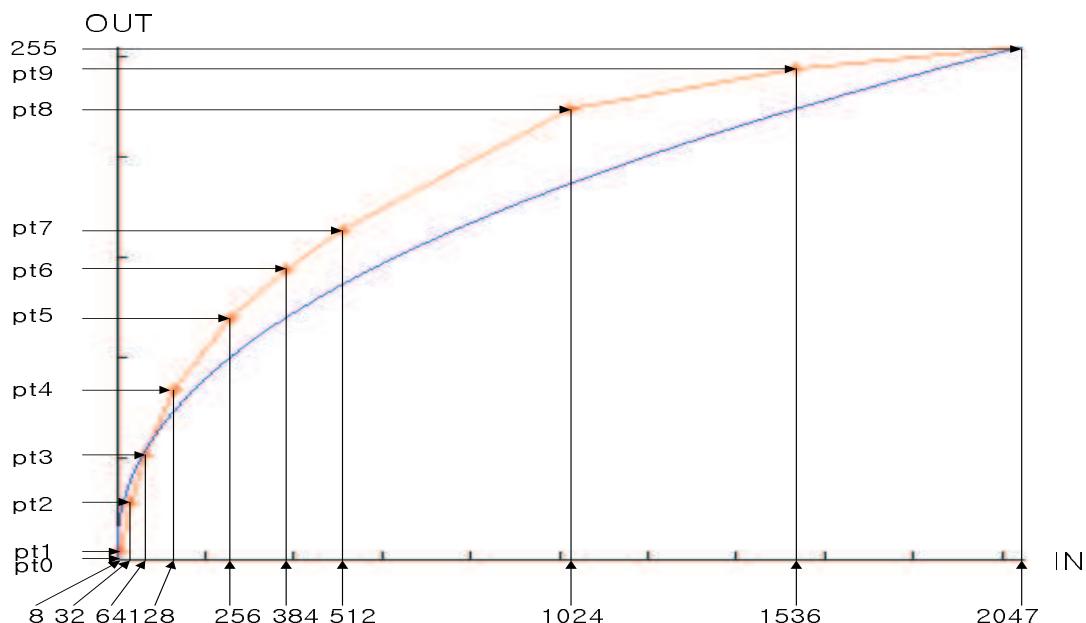
In the above figure, the blue curve is 0.45 gamma effect and the red is default gamma effect. The x-axis label is value fixed by our sensor and it isn't able to be changed by user. User is able to change only pt0 ~ pt9(programmable gamma pointer : GMAP0 ~ GMPP9) and slp0 ~ slp9(gamma slop : GMAS0 ~ GMAS9) to be calculated by below equation,

x-axis(xpt) = [0, 8, 32, 64, 128, 256, 384, 512, 1024, 1536, 2047]   - input data
gamma pointer(pt) = [0, 4, 28, 52, 84, 120, 144, 164, 224, 244, 255]   - output data (default)
gamma slop(slp) = 128 * $\triangle$xpt / $\triangle$pt

Color Interpolation

This method is supported to interpolate missing R, G, or B for mosaic image data from pixel array. Interpolation method for missing color is done by moving window, and the missing color on center of window is neighbor pixels.

Color Correction

Color Correction is implemented by 3x3 matrix operation. Color correction matrix may be resolved by measuring sensor's color spread characteristics for primary color source and calculating the inverse matrix of color spread matrix. Matrix coefficients are programmable from −127/64 to 127/64. Programming register value for matrix coefficients should be resolved by the following equations.

For positive values, CMAxx = Integer(RealCoefficientValue x 64);
For negative values, CMAxx = TwoComplement(Integer(RealCoefficientValue x 64));
RealCoefficientValue values from −127/64 to 127/64 can be programmed.

Color-Correction Matrix(CCM) to correct the mismatch of Color Filter Array(CFA)
R'   = 1.189R − 0.315G + 0.126B
G'   = -0.259R + 1.838G − 0.579B

B'   = -0.029R – 0.374G + 1.403B

※ Color-corrected R'G'B' = CCM * Gamma-corrected RGB

※ In the above equations, R, G, and B are gamma-corrected values.

Color Space Conversion

For color space conversion matrix, the equation from CCIR-601 standard is normally used.

1. RGB to YUV Color Space Conversion(CSC) equation

V   = (131R' – 110G' – 21B') / 256 + 128 Range: 16 ~ 240

Y   = (77R' + 150G' + 29B') / 256   Range: 16 ~ 235

U   = (-44R' –87G' + 131B') / 256 + 128   Range: 16 ~ 240

※ VYU = CSC * Color-corrected R'G'B' + [128   0   128]

YUV to RGB reverse conversion equation

R = Y + 1.371(V – 128)

G = Y – 0.698(V – 128) – 0.336(U – 128)

B = Y + 1.732(U – 128)

2. RGB to YCbCr Color Space Conversion(CSC) equation

Cr   = (112R' – 94G' – 18B') / 256 + 128 Output range: 16 ~ 240

Y   = (66R' + 129G' + 25B') / 256 + 16   Output range: 16 ~ 235

Cb   = (-38R' –74G' + 112B') / 256 + 128 Output range: 16 ~ 240

※ CrYCb = CSC * Color-corrected R'G'B' + [128   16   128]

YCbCr to RGB reverse conversion equation

R   = 1.1636Y – 0.0029Cb + 1.5991Cr – 222.9271

G   = 1.1636Y – 0.3914Cb – 0.8184Cr + 136.2322

B   = 1.1636Y + 2.0261Cb + 0.0016Cr – 278.1660

Output Formatter

The output formats such as 8bit Bayer Raw Data, 16bit RGB 4:4:4, 16bit YCbCr 4:4:4, 8bit/16bit YCbCr 4:2:2, and 8bit RGB5:6:5 are supported. Possible output bus widths are 8 bits or 16bits, and the sequence of Cb and Cr are programmable. The output formats are compatible with Recommendation CCIR-601, CCIR-656.

Auto Exposure Control

Y mean value is continuously calculated every frame, and the integration time and the analog preamplifier gain value are mutually increased or decreased according to difference between target and current frame Y mean value.

Auto White Balance Control

Cb, Cr frame mean value is calculated every frame, and according to Cb, Cr frame mean values'

displacement from Cb, Cr white target point, R, B scaling values for R, B data are resolved and R, G color gain is mutually increased or decreased.

On-chip frequency synthesizer (PLL)

The PLL is a 1.8V CMOS analog programmable frequency synthesizer based on charged pump type PLL for an on-chip application. PLL has a wide output range. Operating frequency and loop characteristics of PLL are fully programmable. When it is used with the default mode(2x), the output frame rate is supported up to 15frame per second at MCLK 21MHz and VCLK generates up to 42MHz.

Luminance processing - Contrast and brightness

For contrast adjustment, Y digital channels are scaled by the contrast factor. Contrast factor resolution is 1/128 and its range is 0 ~ 255/128.

For brightness adjustment, there is added a brightness factor to Y digital channels. Brightness factor range is –128 ~ 127 and register value for brightness adjustment is following below.

For positive values, Brightness factor = Integer;

For negative values, Brightness factor = Two's Complement(Integer);

For example, if brightness factor is 3, register value is 8'h03 and if brightness factor is -3, register value is 8'hfd.

Contast
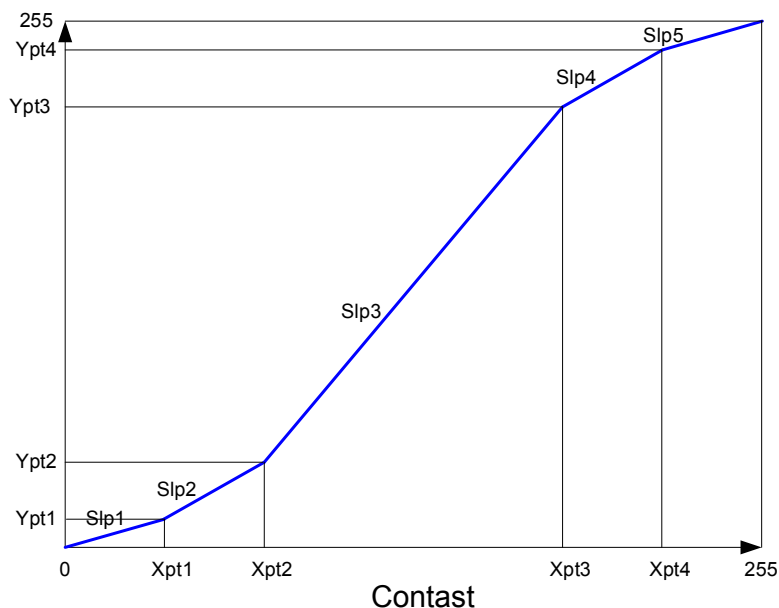
Chrominance processing - Hue, saturation, chroma suppression, and false color suppression

For saturation adjustment, Cb, Cr digital Channels are scaled by the saturation factor. Saturation factor resolution is 1/128 and its range is 0 ~ 255/128.

Chroma suppression is performed in the dark environment for suppressing the color and decreasing dark bad pixel effect. Suppression level is varied in accordance with amplifier gain and

saturation level is user-programmable.

Edge enhancement
Edge enhancement is performed for increasing sharpness of image. Edge weight factor is user-programmable.

Special image functions
Special image functions support the negative, mono, gray, level, and sepia image.

Frame Timing
For clear description of frame timing, clocks' acronym and relation are reminded in here again.

< Clock Acronym Definition >

MCP : Master Clock Period	DCP : Divided Clock Period
SCP : Sensor Clock Period	ICP : Image Processing Clock Period
VCP : Video Clock Period	LCP : Line Clock Period

< Clock Frequency Relation >

MCP : MCP	DCP : MCP * Clock Division	
SCP : DCP * 2	ICP	SCP for color interpolation, SCP * 2 for 1/4 subsampling mode SCP * 4 for 1/16 subsampling mode
VCP : ICP for 16bit output, ICP / 2 for 8bit output	LCP : HBLANK Period + HSYNC Period	

HBLANK Period : HBLANK Time register value * SCP

HSYNC Period : HSYNC Active Time

< Frame Time Calculation >
Core Frame Time is (IDLE SLOT + Video Height * LCP), and Real Frame Time is resolved as follows.

When Integration Time > Core Frame Time, Real Frame Time is (Integration Time + VBLANK * LCP),

otherwise is (Core Frame Time + VBLANK * LCP).

If Integration Time < Core Frame Time, Real Frame Time is

{(1280 + 214) * (960 + 10) + SCTRC[0] * 4928} * SCP = 1454108 * 47.62ns = 0.069245sec,

else Real Frame Time is

{Integration Time + 8 * (208 + 1280) } * SCP.

1. 1/4 Sub-sampling Timing
In 1/4 subsampling mode, valid video data is produced every other line, i.e. for 960 lines, active video lines are 432 lines. HSYNC active time is equal to HSYNC active time of color interpolation

mode, but video clock frequency is half of color interpolation mode's to produce half size output in horizontal direction. Frame rate at the 1/4 ISP sub-sampling mode is equal to the full mode, but at the 1/4 Bayer sub-sampling mode, double of the full mode.

2. 1/16 Sub-sampling Timing

In 1/16 subsampling mode, valid video data is produced every four line, i.e. for 960 lines, active video lines are 216 lines. HSYNC active time is equal to HSYNC active time of color interpolation mode, but video clock frequency is a quarter of color interpolation mode's to produce a quarter size output in horizontal direction. Frame rate at the 1/16 ISP sub-sampling mode is equal to the full mode, but at the 1/16 Bayer sub-sampling mode, 4 times of the full mode.

Anti-Banding Configuration

For Anti-Banding mode to work correctly, the following registers should be configured to the appropriate values.

AE Mode1	70h	Anti-Banding Enable[6]
AE Anti-Banding Step	7a-7ch	SCP * (2 x power line frequency)
AE Integration Time Limit	7d-7fh	The value should be multiples of AE Anti-Banding Step

When Anti-Banding is enabled, AE initializes Integration Time registers[73-75h] to 4 x Anti-Banding Step value[7a-7ch], and integration increment/decrement amount is set to Anti-Banding Step value in order to remove anti-banding noise caused by intrinsic energy waveform of light sources. Banding noise is inherent in CMOS image sensor that adopts rolling shutter scheme for image acquisition.

MagnaChip *Confidential*

Register Description

Symbol	Address (Hex)	Default (Hex)	Recommend (Hex)	Description
DEVID	00	61		Device ID
SCTRA	01	23	13	Sensor Control A
SCTRB	02	00		Sensor Control B
SCTRC	03	01		Sensor Control C
RSAU	08	00		Row Start Address Upper
RSAL	09	02		Row Start Address Lower
CSAU	0A	00		Column Start Address Upper
CSAL	0B	02		Column Start Address Lower
WIHU	0C	03		Window Height Upper
WIHL	0D	C0		Window Height Lower
WIWU	0E	05		Window Width Upper
WIWL	0F	00		Window Width Lower
HBLU	10	00		Horizontal Blank Time Upper
HBLL	11	D0		Horizontal Blank Time Lower
VBLU	12	00		Vertical Blank Time Upper
VBLL	13	08		Vertical Blank Time Lower
RCG	14	15	20	Red Color Gain
GCG	15	15	20	Green Color Gain
BCG	16	15	20	Blue Color Gain
PGAVAL	17	08	22	Amp Gain for Pixel Output
PGAMIN	18	00	14	Amp Gain Minimum Value
PGAMAX	19	FF	5F	Amp Gain Maximum Value
PGANOM	1A	08	22	Amp Gain Normal Value
RCLMP	1C	07	07	Clamp Enable, Reset Level Clamp Enable
PXLBS	1D	11	66	Pixel Bias and Shift Bias controls
PGABS	1E	77	d3	PGA Bias and CDS Bias controls

ADCBS	1F	20		ADC Bias controls
OREDI	21	7F	85	ADC Initial Offset Value for Optical Black Red
OGRNI	22	7F	A0	ADC Initial Offset Value for Optical Black Green
OBLUI	23	7F	85	ADC Initial Offset Value for Optical Black Blue
OREDU	24	RO		ADC Red Update Offset
OGRNU	25	RO		ADC Green Update Offset
OBLUU	26	RO		ADC Blue Update Offset
BLKTH	**27**	**FF**		**Black Level Threshold Value**
CREDI	**28**	**00**		**Digital Compensation Red Offset Value**
CGRNI	**29**	**00**		**Digital Compensation Green Offset Value**
CBLUI	**2A**	**00**		**Digital Compensation Blue Offset Value**
ISPFUN	30	02	FE	Image Signal Processing Functions Enable
OUTFMT	31	30		Image Data Output Format
OUTINV	32	00		Output Signal Inversion
DNCMODE	33	21		Dark Noise Cancellation Mode
DNCGAIN	34	3E		Preamp. Gain to activate Dark Noise Cancellation
DNCINTH	35	13	26	Integration time to activate Dark Noise Cancellation
DNCINTM	36	12	26	Integration time to activate Dark Noise Cancellation
CRCM11	37	2F	2C	Color Correction matrix coefficient 11
CRCM12	38	DB	D5	Color Correction matrix coefficient 12
CRCM13	39	F6	FE	Color Correction matrix coefficient 13
CRCM21	3A	0F	13	Color Correction matrix coefficient 21
CRCM22	3B	28	2E	Color Correction matrix coefficient 22
CRCM23	3C	08	00	Color Correction matrix coefficient 23
CRCM31	3D	F5	F0	Color Correction matrix coefficient 31
CRCM32	3E	C3	BD	Color Correction matrix coefficient 32
CRCM33	3F	3D	51	Color Correction matrix coefficient 33
GMAP0	40	00	00	Start point for gamma line segment 0
GMAP1	41	01	04	Start point for gamma line segment 1

GMAP2	42	08	0B	Start point for gamma line segment 2
GMAP3	43	20	13	Start point for gamma line segment 3
GMAP4	44	3A	20	Start point for gamma line segment 4
GMAP5	45	58	36	Start point for gamma line segment 5
GMAP6	46	6D	49	Start point for gamma line segment 6
GMAP7	47	7D	5A	Start point for gamma line segment 7
GMAP8	48	AE	98	Start point for gamma line segment 8
GMAP9	49	D7	CE	Start point for gamma line segment 9
GMAS0	4A	10	40	Slope value for gamma line segment 0
GMAS1	4B	25	27	Slope value for gamma line segment 1
GMAS2	4C	60	1F	Slope value for gamma line segment 2
GMAS3	4D	34	1A	Slope value for gamma line segment 3
GMAS4	4E	1E	16	Slope value for gamma line segment 4
GMAS5	4F	15	13	Slope value for gamma line segment 5
GMAS6	50	10	12	Slope value for gamma line segment 6
GMAS7	51	0C	0F	Slope value for gamma line segment 7
GMAS8	52	0A	0D	Slope value for gamma line segment 8
GMAS9	53	0A	0C	Slope value for gamma line segment 9
RCRCONST	54	57		Inverse Color Space Conversion Constant for R
GCRCONST	55	D4		Inverse Color Space Conversion Constant for G
GCBCONST	56	EB		Inverse Color Space Conversion Constant for G
BCBCONST	57	6E		Inverse Color Space Conversion Constant for B
SINX	58	00		Hue Sin value
COSX	59	80		Hue Cos value
BRIGHTNESS	5B	00		Brightness value
SATURATION	5C	80		Saturation value
EGWTCON	5D	00	03	Edge Weight Control Value
EDTHLO	5E	10	07	Edge Enhancement Threshold Low
SUPGMIN	60	24		Suppression Pre Amp Gain Min

SATGMIN	61	24		Saturation Pre Amp Gain Min
EDGGMIN	62	24		Edge Enhancement Preamp. Gain Min
HIEDGVAL	63	FF		Edge Enhancement Higher Limit Value
FCORTHLO	64	00		False Color Suppression Threshold Low
FCORTHHI	65	FF		False Color Suppression Threshold High
CONSTRAST	**66**	**00**		**Contrast**
CONTVALUE	**67**	**00**		**Contrast Control Value**
SPESEL	**68**	**00**		**Special Image Functions Mode**
SPETHVALUE	69	00		Special Image Functions Threshold value
AF_CTRL	**6A**	**A6**		**Auto Focus Value Control**
AF_WinWgt	**6B**	**CD**		**Window Weight Control for AF**
AF_EdgTh	**6C**	**00**		**Edge Threshold for AF**
AF_StateThH	**6D**	**00**		**State-decision Threshold High for AF**
AF_StateThL	**6E**	**0A**		**State-decision Threshold Low for AF**
AEMODE1	70	29	69	AE Mode1
AEMODE2	71	ED		AE Mode2
AEWINWGT	72	CD		AE Window Weight
INTH	73	02		Integration Time High
INTM	74	71		Integration Time Middle
INTL	75	03		Integration Time Low
LUTARGET1	76	5A	50	AE In-Door Target
LUTARGET2	77	5A	50	AE Out-Door Target
AELOCKFINEBND	78	F6	F4	AE Lock Boundary
AEUNLOCKBND	79	2A	2B	AE Unlock Boundary
AEINTSTEPH	7A	01	01	AE Anti-Flicker Step High
AEINTSTEPM	7B	38	96	AE Anti-Flicker Step Middle
AEINTSTEPL	7C	80	E6	AE Anti-Flicker Step Low
AEINTLIMITH	7D	09	26	AE Maximum Limit High
AEINTLIMITM	7E	C4	25	AE Maximum Limit Middle
AEINTLIMITL	7F	00	90	AE Maximum Limit Low

AWBMODE	80	18	38	AWB Mode
AWBWINWGT	82	00		AWB Window Weight
CBTARGT	83	80	7C	AWB Cb Target Position
CRTARGT	84	80	7C	AWB Cr Target Position
AWBLOCKBND	85	04		AWB Lock Boundary
AWBUNLOCKBND	86	20		AWB Unlock Boundary
CBWHITEBND	87	30		AWB Cb White Pixel Boundary
CRWHITEBND	88	30		AWB Cr White Pixel Boundary
AWBCBND	89	30		AWB Cb + Cr Boundary
AEFSM	8C	RO		AE State Machine
AWBFSM	8D	RO		AWB State Machine
LUFMEAN	8E	RO		Lu Frames Mean
CBFMEAN	8F	RO		Cb Frame Mean
CRFMEAN	90	RO		Cr Frame Mean.
KLBNDMIN	91	14		Anti Banding Preamp Gain Min
KLBNDMAX	92	3D	2D	Anti Banding Preamp Gain Max
AWBWHITE	93	FF		Awb White Pixel Boundary
AWBBLACK	94	00		Awb Black Pixel Boundary
AWBNUMBER	95	02		Awb Valid Number
INTSCNOFSH	96	RO		Integration – Scan Plane Offset High
INTSCNOFSM	97	RO		Integration – Scan Plane Offset Mid
INTSCNOFSL	98	RO		Integration – Scan Plane Offset Low
AWBRGAINMAX	9A	7F	3F	AWB Red Gain Maximum Value
AWBRGAINMIN	9B	00		AWB Red Gain Minimum Value
AWBBGAINMAX	9C	7F	3F	AWB Blue Gain Maximum Value
AWBBGAINMIN	9D	00		AWB Blue Gain Minimum Value
PCTRA	A0	01	00	PLL Control Register A
PCTRB	A1	1D	10	PLL Control Register B
PREFDIV	A3	01		PLL Reference Divisor
PFDDIVH	A4	00		PLL Feedback Divisor High

PFDDIVL	A5	02		PLL Feedback Divisor Low
AF_State	**B0**	**RO**		**Current State for AF**
AF_Value4	**B1**	**RO**		**Focal Value 4th Byte for AF (Upper)**
AF_Value3	**B2**	**RO**		**Focal Value 3rd Byte for AF**
AF_Value2	**B3**	**RO**		**Focal Value 2nd Byte for AF**
AF_Value1	**B4**	**RO**		**Focal Value 1st Byte for AF (Lower)**
NFILTERCON	**B5**	**04**	**84**	**Adaptive Noise Filter Control**

Device ID [DEVID : 00h : 61h]

7	6	5	4	3	2	1	0
Product ID				Revision Number			
0	1	1	0	0	0	0	1

High Nibble represents product number, Low Nibble represents revision number.

Sensor Control A [SCTRA : 01h : 23h]

7	6	5	4	3	2	1	0
Reserved	Fixed Frame Rate	X-Flip	Y-Flip	CifMode	SSSel	Video Mode	
0	0	1	0	0	0	1	1

Fixed Frame Rate	Sensor supports the fixed frame rate with anti-banding mode
X-Flip	Image is horizontally flipped
Y-Flip	Image is vertically flipped
CifMode	4CIF, CIF(1/4 sub-sampling), or QCIF(1/16 sub-sampling) mode enable
SSSel	Sub-Sampling mode
	0 — ISP Sub-Sampling. Image quality is better than Bayer Sub-Sampling, but Core Frame Rate doesn't change.
	1 — Bayer Sub-Sampling. Image quality is lower than ISP Sub-Sampling, but Core Frame Rate is double.
Video Mode	11 — No Scaling mode
	10 — 1/4 sub-sampling
	01 — 1/16 sub-sampling
	00 — No Scaling mode (equal to '11')

Sensor Control B [SCTRB : 02h : 00h]

7	6	5	4	3	2	1	0
AE/AWB Block Sleep	Datapath Block Sleep	Analog Block Sleep	Sleep Mode	Strobe Enable	Clock Division		
0	0	0	0	0	0	0	0
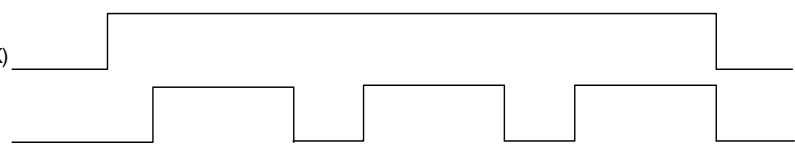
AE/AWB Block Sleep	AE/AWB block goes into sleep mode with this bit set to high.
Datapath Block Sleep	Image processing datapath block goes into sleep mode with this bit set to high.
Analog Block Sleep	All internal analog block goes into sleep mode with this bit set to high. With All Digital Block Sleep active, sensor goes into power down mode.
Sleep Mode	All internal digital and analog block goes into soft sleep with this bit set to

This document has a general product description and is subject to change without notice. MagnaChip Semiconductor Ltd. does not assume any responsibility for use of circuits described and no patent licenses are implied.

MagnaChip *Confidential*

	high.
Strobe Enable	When strobe signal is enabled by this bit, STROBE pin will indicates when strobe light should be splashed in the dark environment to get adequate lighted image.
Clock Division	Divides input master clock(IMC) for internal use. Internal divided clock frequency(DCF) is defined as master clock frequency(MCF) divided by specified clock divisor. Internal divided clock frequency(DCF) is as follows. 000 : MCF, 001 : MCF/2, 010 : MCF/4, 011 : MCF/8 100 : MCF/16, 101 : MCF/32, 110 : MCF/64, 111 : MCF/128

Sensor Control C [SCTRC : 03h : 01h]

7	6	5	4	3	2	1	0
Bayer Output Enable	Single Shot Mode	Black Level Average Output	HSYNC in VBLANK	reserved	reserved	Black Level Data Enable	Black Level Compens ation
0	0	0	0	0	0	0	1

Bayer Output Enable	More information is available on Bayer Data Format section.
Single Shot Mode	With this register set to High, single video image is streamed out.
Black Level Average Output	This bit enable R/G/B Active Offset registers[24h-26h] to represent black level average value, instead of updated active offset values
HSYNC in VBLANK	VBLANK is equivalent to VSYNC, and HSYNC is the inversion of HBLANK, and this bit controls whether HSYNC is active or not when VBLANK unit is LCF. VSYNC (VBLANK) HSYNC
Black Level Data Enable	HSYNC is generated for light-shielded pixels in 4 lines.
Black Level Compensation	Black level average values of light-shielded pixels are compensated when active image data is produced.

Row Start Address Upper [RSAU : 08h : 00h]

7	6	5	4	3	2	1	0
Reserved						Row Start Address Upper	
R0	R0	R0	R0	R0	R0	0	0

MagnaChip *Confidential*

Row Start Address Lower [RSAL : 09h : 02h]

7	6	5	4	3	2	1	0
Row Start Address Lower							
0	0	0	0	0	0	1	0

Row Start Address register defines the row start address of image read-out operation.

Column Start Address Upper [CSAU : 0ah : 00h]

7	6	5	4	3	2	1	0
Reserved					Column Start Address Upper		
R0	R0	R0	R0	R0	0	0	0

Column Start Address Lower [CSAL : 0bh : 02h]

7	6	5	4	3	2	1	0
Column Start Address Lower							
0	0	0	0	0	0	1	0

Column Start Address register defines the column start address of image read-out operation.

Window Height Upper [WIHU : 0ch : 03h]

7	6	5	4	3	2	1	0
Reserved						Window Height Upper	
R0	R0	R0	R0	R0	R0	1	1

Window Height Lower [WIHL : 0dh : c0h]

7	6	5	4	3	2	1	0
Window Height Lower							
1	1	0	0	0	0	0	0

Window Height register defines the height of image to be read-out.

Window Width Upper [WIWU : 0eh : 05h]

7	6	5	4	3	2	1	0
Reserved					Window Width Upper		
R0	R0	R0	R0	R0	1	0	1

Window Width Lower [WIWL : 0fh : 00h]

7	6	5	4	3	2	1	0
Window Width Lower							
0	0	0	0	0	0	0	0

MagnaChip *Confidential*

Window Width Address register defines the width of image to be read-out.

Horizontal Blank Time Upper [HBLU : 10h : 00h]

7	6	5	4	3	2	1	0
Horizontal Blank Time Upper							
0	0	0	0	0	0	0	0

Horizontal Blank Time Lower [HBLL : 11h : d0h]

7	6	5	4	3	2	1	0
Horizontal Blank Time Lower							
1	1	0	1	0	0	0	0

HBLANK Time register defines data blank time between current line and next line by using Sensor Clock Period unit, and should be larger than 208(d0h).

Vertical Blank Time Upper [VBLU : 12h : 00h]

7	6	5	4	3	2	1	0
Vertical Blank Time Upper							
0	0	0	0	0	0	0	0

Vertical Blank Time Lower [VBLL : 13h : 08h]

7	6	5	4	3	2	1	0
Vertical Blank Time Lower							
0	0	0	0	1	0	0	0

VBLANK Time register defines active high duration of VSYNC output. Active high VSYNC indicates frame boundary between continuous frames.

Red Color Gain [RCG : 14h : 15h]

7	6	5	4	3	2	1	0
Reserved	Red Amplifier Gain						
0	0	0	1	0	1	0	1

Green Color Gain [GCG : 15h :15h]

7	6	5	4	3	2	1	0
Reserved	Green Amplifier Gain						
0	0	0	1	0	1	0	1

Blue Color Gain [BCG : 16h :15h]

7	6	5	4	3	2	1	0

Reserved	Blue Amplifier Gain						
0	0	0	1	0	1	0	1

There are three color gain registers for R, G, and B pixels, respectively. Programmable range is from 0.5X ~ 3.5X. Effective Gain = 0.5 + B<6:0>/42.4. These registers may be used for white balance and color effect with independent R,G,and B color control. Recommend gain is 1.0X (15h).

Amp Gain for Pixel Output [PGAVAL : 17h : 08h]

7	6	5	4	3	2	1	0
Amp Gain							
0	0	0	0	1	0	0	0

Amp Gain is common gain for R, G, B channel and used for auto exposure control. Programmable range is from 0.5X ~ 16.5X. Default gain is 1.0X.
Gain = 0.5 + B<7:0>/16

Amp Gain Minimum Value [PGAMIN : 18h : 00h]

7	6	5	4	3	2	1	0
Amp Gain Minimum							
0	0	0	0	0	0	0	0

Amp Gain Minimum Value is minimum value of amplifier gain when sensor adjusts amplifier gain for auto exposure control. Programmable range is same as Amp Gain. Default value is 0.5X.

Amp Gain Maximum Value [PGAMAX : 19h : ffh]

7	6	5	4	3	2	1	0
Amp Gain Maximum							
1	1	1	1	1	1	1	1

Amp Gain Maximum Value is maximum value of amplifier gain when sensor adjusts amplifier gain for auto exposure control. Programmable range is same as Amp Gain. Default value is 16.5X.

Amp Gain Normal Value [PGANOM : 1ah : 08h]

7	6	5	4	3	2	1	0
Amp Gain Normal							
0	0	0	0	1	0	0	0

Amp Gain Normal Value is reference value of amp gain when sensor adjusts amp gain for auto exposure control. First, sensor controls integration time before adjusting amp gain for auto exposure control. After integration time is changed to the minimum or maximum value, sensor adjusts amp gain from this register value. Refer to figure of AE mode2 register(71H).
Programmable range is same as Amp Gain. Default value is 1.0X.

This document has a general product description and is subject to change without notice. MagnaChip Semiconductor Ltd. does not assume any responsibility for use of circuits described and no patent licenses are implied.

Reset Level Clamp [RCLMP : 1ch : 17h]

7	6	5	4	3	2	1	0
Reserved			Clamp On	Reset Level Clamp			
0	0	0	1	0	1	1	1

Because extremely bright image like sun affects reset data voltage of pixel to lower, bright image is captured as black image in image sensor regardless of correlated double sampling. To solve this extraordinary phenomenon, we adopt the method to clamp reset data voltage. Reset Level Clamp controls the reset data voltage to prevent inversion of extremely bright image. The larger register value clamps the reset data level at highest voltage level. Default value is 7 to clamp the reset data level at appropriate voltage level.

Pixel Bias [PXLBS : 1dh : 11h]

7	6	5	4	3	2	1	0
Reserved	Pixel Bias			Reserved	Shift Bias		
0	0	0	1	0	0	0	1

Pixel Bias and Shift Bias controls the amount of current in pixel bias circuit to operate Pixel effectively.

Programmable Amplifier Bias [PGABS : 1eh : 77h]

7	6	5	4	3	2	1	0
PGA Bias				CDS Bias			
0	1	1	1	0	1	1	1

PGA Bias and CDS Bias control the amount of current in PGA and CDS bias circuit to operate PGA and CDS effectively.

ADC Bias Control [ADCBS : 1fh : 20h]

7	6	5	4	3	2	1	0
Reserved	ADC Bias			Reserved			
0	0	1	0	0	0	0	0

ADC Bias controls the amount of current in ADC bias circuit to operate ADC effectively.

Auto black level compensation

Each sensor has little different photo-diode characteristics so that the sensor provides internal adjustment registers that calibrates internal sensing circuit in order to get optimal performance. Sensor characteristics adjustment registers are as below.

MagnaChip *Confidential*

ADC Initial Offset Value for Optical Black Red [OREDI : 21h : 7fh]

7	6	5	4	3	2	1	0
Red Pixel Black Offset							
0	1	1	1	1	1	1	1

ADC Initial Offset Value for Optical Black Green [OGRNI : 22h : 7fh]

7	6	5	4	3	2	1	0
Green Pixel Black Offset							
0	1	1	1	1	1	1	1

ADC Initial Offset Value for Optical Black Blue [OBLUI : 23h : 7fh]

7	6	5	4	3	2	1	0
Blue Pixel Black Offset							
0	1	1	1	1	1	1	1

These registers control the offset voltage of ADC that changes the black level value for light-shielded pixels, R,G,and B respectively. Register bit functions are composed as follows.

Pixel Black Offset[7]	The bit specifies whether to subtract or add the offset voltage in ADC input for light-shielded pixels.
Pixel Black Offset[6:0]	This value specifies the amount of offset voltage for light-shielded pixels.

Red Pixel Active Offset [OREDU : 24h : RO]

7	6	5	4	3	2	1	0
Red Pixel Active Offset							
RO	RO	RO	RO	RO	RO	RO	RO

Green Pixel Active Offset [OGRNU : 25h : RO]

7	6	5	4	3	2	1	0
Green Pixel Active Offset							
RO	RO	RO	RO	RO	RO	RO	RO

Blue Pixel Active Offset [OBLUU : 26h : RO]

7	6	5	4	3	2	1	0
Blue Pixel Active Offset							
RO	RO	RO	RO	RO	RO	RO	RO

These registers represent black level average offset values for light-shielded pixels R,G,B or updated active offset values for R,G,B, respectively. What values are monitored is decided by

SCTRC[5].

Black Level Threshold Value [BLKTH : 27h : ffh]

7	6	5	4	3	2	1	0
Black Level Threshold							
0	0	1	1	1	1	1	1

The register specifies the maximum value that determines whether light-shielded pixel output is valid. When light-shielded pixel output exceeds this limit, the pixel is not accounted for black level calculation.

ADC Compensation Offset Value for Optical Black Red [CREDI : 28h : 00h]

7	6	5	4	3	2	1	0
Red Pixel Compensation Offset							
0	1	1	1	1	1	1	1

ADC Compensation Offset Value for Optical Black Green [CGRNI : 29h : 00h]

7	6	5	4	3	2	1	0
Green Pixel Compensation Offset							
0	1	1	1	1	1	1	1

ADC Compensation Offset Value for Optical Black Blue [CBLUI : 2ah : 00h]

7	6	5	4	3	2	1	0
Blue Pixel Compensation Offset							
0	1	1	1	1	1	1	1

These registers manually control the offset value of ADC addition to ADC initial offsets. Register bit functions are composed as follows.

Compensation Offset[7]	The bit specifies whether to subtract or add the offset level.
Compensation Offset[6:0]	This value specifies the amount of offset level.

ISP Function Enable [ISPFUN : 30h : 02h]

7	6	5	4	3	2	1	0
Saturation Suppression Enable	Color Suppression Enable	False Color Suppression Enable	Smooth Filter Enable	Edge Enhance Enable	Edge Algorithm Select	Gamma Correction	Y+16 Enable
0	0	0	0	0	0	1	0

Output Format [OUTFMT : 31h : 30h]

7	6	5	4	3	2	1	0
Reserved	Bayer 11bit Output	U First	Y First	16bit Bus	RGB 5:6:5	4:4:4 Format	24bit RGB
0	0	1	1	0	0	0	0

Bayer 11bit Output	If this bit is high, then 11bit Bayer raw values are continuously outputted through output ports, Y0[7:0] = Bayer[10:3], Y1[2:0] = Bayer[2:0], else 8bit Bayer raw only, Y[7:0] = Bayer[10:3]. And when this bit is high and 16bit bus mode is enabled, Y[7:0] is outputted Bayer[10:3] and C[2:0] is outputted Bayer[2:0]. For more information, refer page 62, Bayer data format.
U First	Cb(B) pixel in front of Cr(R) pixel in 16bit or 8bit video data output modes.
Y First	Y pixel in front of Cb and Cr pixels in 8bit video output mode. This option is meaningful only with YCbCr 4:2:2 8bit output mode.
16Bit Bus	If this bit is high, output format is 16bit mode(YCbCr 4:2:2, YCbCr 4:4:4, or RGB 4:4:4), otherwise output format is 8bit mode(YCbCr 4:2:2, RGB 5:6:5, Bayer).
RGB 5:6:5	Data format of RGB 5:6:5 mode is composed with {R[7:3]/G[7:5]}, {G[4:2]/B[7:3]} or {B[7:3]/G[7:5]}, {G[4:2]/R[7:3]}. OUTFMT[5](Cb/B First) register affects above data form.
4:4:4 Format	YCbCr 4:4:4 or RGB 4:4:4 24bit data for a pixel is produced with 16bit output mode. (16bit Bus = '1')
24Bit RGB	R,G,B 4:4:4 24bit data for a pixel is produced with 16bit output mode.(16bit Bus = '1' and 4:4:4 Format = '1')

Default mode of Output Format is YCbCr 4:2:2 8bit bus mode.

Output Signal Inversion [OUTINV : 32h : 00h]

7	6	5	4	3	2	1	0
Reserved				Clocked HSYNC	VSYNC inversion	HSYNC inversion	VCLK inversion
0	0	0	0	0	0	0	0

Clocked HSYNC	In HSYNC, VCLK is embedded, that is, HSYNC is toggling at VCLK rate during normal HSYNC time
VSYNC inversion	VSYNC output polarity is inverted
HSYNC inversion	HSYNC output polarity is inverted
VCLK inversion	VCLK output polarity is inverted

Dark Noise Cancellation [DNCMODE : 33h : 21h]

7	6	5	4	3	2	1	0
DNC Always Performing Zone				DNC Threshold		DNC Mode	
0	0	1	0	0	0	0	1

DNC Always Performing Zone		In this zone, DNC function is always enabled regardless of DNC Mode.
DNC Threshold		Degree of the dark noise strength (Tight)11 - 10 - 01 - 00(Loose)
DNC Mode	00	Always disabled
	01	Conditional enabled - Integration Time [73h-75h] > (DNC enable integration Time [35h-36h] * 256) - Pre-Amp Gain [17h] > Dnc Gain [34h]
	10	Always enabled

DNC Enable Gain [DNCGAIN : 34h : 3eh]

7	6	5	4	3	2	1	0
Dnc Enable Gain							
0	0	1	1	1	1	1	0

DNC Enable Int. Time High [DNCINTH : 35h : 13h]

7	6	5	4	3	2	1	0
DNC Enable Int. Time High							
0	0	0	1	0	0	1	1

DNC Enable Int. Time Mid [DNCINTM : 36h : 12h]

7	6	5	4	3	2	1	0
DNC Enable Int. Time Min							
0	0	0	1	0	0	1	0

Color Correction Matrix Coefficient 11 [CRCM11 : 37h : 2fh]

7	6	5	4	3	2	1	0
Color Correction Matrix Coefficient 11							
0	0	1	0	1	1	1	1

Color Correction Matrix Coefficient 12 [CRCM 12 : 38h : dbh]

7	6	5	4	3	2	1	0
Color Correction Matrix Coefficient 12							
1	1	0	1	1	0	1	1

Color Correction Matrix Coefficient 13 [CRCM 13 : 39h : f6h]

7	6	5	4	3	2	1	0
Color Correction Matrix Coefficient 13							
1	1	1	1	0	1	1	0

Color Correction Matrix Coefficient 21 [CRCM 21 : 3ah 0fh]

7	6	5	4	3	2	1	0
Color Correction Matrix Coefficient 21							
0	0	0	0	1	1	1	1

Color Correction Matrix Coefficient 22 [CRCM 22 : 3bh : 28h]

7	6	5	4	3	2	1	0
Color Correction Matrix Coefficient 22							
0	0	1	0	1	0	0	0

Color Correction Matrix Coefficient 23 [CRCM 23 : 3ch : 08h]

7	6	5	4	3	2	1	0
Color Correction Matrix Coefficient 23							
0	0	0	0	1	0	0	0

Color Correction Matrix Coefficient 31 [CRCM 31 : 3dh : f5h]

7	6	5	4	3	2	1	0
Color Correction Matrix Coefficient 31							
1	1	1	1	0	1	0	1

Color Correction Matrix Coefficient 32 [CRCM 32 : 3eh : c3h]

7	6	5	4	3	2	1	0
Color Correction Matrix Coefficient 32							
1	1	0	0	0	0	1	1

Color Correction Matrix Coefficient 33 [CRCM 33 : 3fh : 3dh]

7	6	5	4	3	2	1	0
Color Correction Matrix Coefficient 33							
0	0	1	1	1	1	0	1

Gamma Segment Start Points

MagnaChip *Confidential*

Gamma Segment Start Points specify the start points of nine line segments for piecewise gamma approximation. Current default gamma curve is much selected for optimum gray gradation.

Gamma Point 0 [GAMP0 : 40h : 00h]

7	6	5	4	3	2	1	0
Gamma Point 0							
0	0	0	0	0	0	0	0

Gamma Point 1 [GMAP1 : 41h : 01h]

7	6	5	4	3	2	1	0
Gamma Point 1							
0	0	0	0	0	0	0	1

Gamma Point 2 [GMAP2 : 42h : 08h]

7	6	5	4	3	2	1	0
Gamma Point 2							
0	0	0	0	1	0	0	0

Gamma Point 3 [GMAP3 : 43h 20h]

7	6	5	4	3	2	1	0
Gamma Point 3							
0	0	1	0	0	0	0	0

Gamma Point 4 [GMAP4 : 44h : 3ah]

7	6	5	4	3	2	1	0
Gamma Point 4							
0	0	1	1	1	0	1	0

Gamma Point 5 [GMAP5 : 45h : 58h]

7	6	5	4	3	2	1	0
Gamma Point 5							
0	1	0	1	1	0	0	0

Gamma Point 6 [GMAP6 : 46h : 6dh]

7	6	5	4	3	2	1	0
Gamma Point 6							
0	1	1	0	1	1	0	1

MagnaChip *Confidential*

Gamma Point 7 [GMAP7 : 47h : 7dh]

7	6	5	4	3	2	1	0
Gamma Point 7							
0	1	1	1	1	1	0	1

Gamma Point 8 [GMAP8 : 48h : aeh]

7	6	5	4	3	2	1	0
Gamma Point 8							
1	0	1	0	1	1	1	0

Gamma Point 9 [GMAP9 : 49h : d7h]

7	6	5	4	3	2	1	0
Gamma Point 9							
1	1	0	1	0	1	1	1

Gamma Slope 0 [GMAS0 4ah : 10h]

7	6	5	4	3	2	1	0
Gamma Slope 0							
0	0	0	1	0	0	0	0

Gamma Slope 1 [GMAS1 : 4bh : 25h]

7	6	5	4	3	2	1	0
Gamma Slope 1							
0	0	1	0	0	1	0	1

Gamma Slope 2 [GMAS2 : 4ch : 60h]

7	6	5	4	3	2	1	0
Gamma Slope 2							
0	1	1	0	0	0	0	0

Gamma Slope 3 [GMAS3 : 4dh : 34h]

7	6	5	4	3	2	1	0
Gamma Slope 3							
0	0	1	1	0	1	0	0

Gamma Slope 4 [GMAS4 : 4eh : 1eh]

7	6	5	4	3	2	1	0
Gamma Slope 4							
0	0	0	1	1	1	1	0

Gamma Slope 5 [GMAS5 : 4fh : 15h]

7	6	5	4	3	2	1	0
Gamma Slope 5							
0	0	0	1	0	1	0	1

Gamma Slope 6 [GMAS6 : 50h : 10h]

7	6	5	4	3	2	1	0
Gamma Slope 6							
0	0	0	1	0	0	0	0

Gamma Slope 7 [GMAS7 : 51h : 0ch]

7	6	5	4	3	2	1	0
Gamma Slope 7							
0	0	0	0	1	1	0	0

Gamma Slope 8 [GMAS8 : 52h : 0ah]

7	6	5	4	3	2	1	0
Gamma Slope 8							
0	0	0	0	1	0	1	0

Gamma Slope 9 [GMAS9 : 53h : 0ah]

7	6	5	4	3	2	1	0
Gamma Slope 9							
0	0	0	0	1	0	1	0

Inverse Color Space Conversion

Inverse color space conversion converts from YUV to RGB and default values support the CCIR-601 standard.   This is activated only when RGB5:6:5 or RGB 4:4:4 formats are used.

$R = Y + A(Cr-128)$

$G = Y - B(Cr-128) – C(Cb-128)$

B = Y + D(Cb-128)

A : Inverse Color constant for R[54h]

B : Inverse Color constant for G[55h]

C : Inverse Color constant for G[56h]

D : Inverse Color constant for B[57h]

Inverse Color constant for R [RCRCONST : 54h : 57h]

7	6	5	4	3	2	1	0
Inverse Color constant for R							
0	1	0	1	0	1	1	1

Inverse Color constant for G [GCRCONST : 55h : d4h]

7	6	5	4	3	2	1	0
Inverse Color constant for G							
1	1	0	1	0	1	0	0

Inverse Color constant for G [GCBCONST : 56h : ebh]

7	6	5	4	3	2	1	0
Inverse Color constant for G							
1	1	1	0	1	0	1	1

Inverse Color constant for B [BCBCONST : 57h : 6eh]

7	6	5	4	3	2	1	0
Inverse Color constant for B							
0	1	1	0	1	1	1	0

Image Enhancement

User is able to control Hue, Saturation, Contrast, and Brightness registers.

Hue value 1 [SINX : 58h : 00h]

7	6	5	4	3	2	1	0
Hue value 1							
0	0	0	0	0	0	0	0

Hue value 2 [COSX : 59h : 80h]

7	6	5	4	3	2	1	0
Hue value 2							

MagnaChip *Confidential*

| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

<Hue Register Setting Parameter>

* SinX , CosX is multiplied by 128.

Angle (°)	SinX (hex)	CosX (hex)	Angle (°)	SinX (hex)	CosX (hex)	Angle (°)	SinX (hex)	CosX (hex)
-30	C0	6E	-9	EC	7E	12	1A	7D
-29	C2	6F	-8	EF	7E	13	1C	7C
-28	C4	71	-7	F1	7F	14	1E	7C
-27	C6	72	-6	F3	7F	15	21	7B
-26	C8	73	-5	F5	7F	16	23	7B
-25	CA	74	-4	F8	7F	17	25	7A
-24	CC	74	-3	FA	7F	18	27	79
-23	CE	75	-2	FC	7F	19	29	79
-22	D1	76	-1	FE	7F	20	2B	78
-21	D3	77	0	00	80	21	2D	77
-20	D5	78	1	02	7F	22	2F	76
-19	D7	79	2	04	7F	23	32	75
-18	D9	79	3	06	7F	24	34	74
-17	DB	7A	4	08	7F	25	36	74
-16	DD	7B	5	0B	7F	26	38	73
-15	DF	7B	6	0D	7F	27	3A	72
-14	E2	7C	7	0F	7F	28	3C	71
-13	E4	7C	8	11	7E	29	3E	6F
-12	E6	7D	9	14	7E	30	40	6E
-11	E8	7D	10	16	7E			
-10	EA	7E	11	18	7D			

Brightness value [BRIGHTNESS : 5bh : 00h]

7	6	5	4	3	2	1	0
Brightness value							
0	0	0	0	0	0	0	0

Brightness value range is from -127 to +128(2's complement).

Saturation value [SATURATION : 5ch : 80h]

7	6	5	4	3	2	1	0
Saturation value							
1	0	0	0	0	0	0	0

MagnaChip *Confidential*

Saturation value range is from 0.0x to 1.99x

< Contrast & Saturation parameter >
* Parameter is multiplied by 128.

Number	Contrast & Saturation (hex)	Number	Contrast & Saturation (hex)
0.1	0D	1.1	8D
0.2	1A	1.2	9A
0.3	26	1.3	A6
0.4	33	1.4	B3
0.5	40	1.5	C0
0.6	4D	1.6	CD
0.7	5A	1.7	DA
0.8	66	1.8	E6
0.9	73	1.9	F3
1.0	80	1.99	FF

Edge Weight Control value [EGWTCON : 5dh : 00h]

7	6	5	4	3	2	1	0
Reserved				Edge Weight			
0	0	0	0	0	0	0	0

Edge weight control value range is from 0.5x to 8.0x.

Edge Enhancement Vth Low [EDTHLO : 5eh : 10h]

7	6	5	4	3	2	1	0
Edge Enhancement Vth Low							
0	0	0	1	0	0	0	0

Suppression Pre Amp Gain Min [SUPGMIN : 60h : 24h]

7	6	5	4	3	2	1	0
Suppression Pre Amp Gain Min							
0	0	1	0	0	1	0	0

Saturation Pre Amp Gain Min [SATGMIN : 61h : 24h]

7	6	5	4	3	2	1	0

Saturation Pre Amp Gain Min							
0	0	1	0	0	1	0	0

Edge Pre Amp Gain Min [EGEGMIN : 62h : 24h]

7	6	5	4	3	2	1	0
Edge Pre Amp Gain Min							
0	0	1	0	0	1	0	0

Hi Edge Value [HIEDGVAL : 63h : ffh]

7	6	5	4	3	2	1	0
Hi Edge Value							
1	1	1	1	1	1	1	1

False Color Th. Low [FCORTHLO : 64h : 00h]

7	6	5	4	3	2	1	0
False Color Th. High							
0	0	0	0	0	0	0	0

False Color Th. High [FCORTHHI : 65h : ffh]

7	6	5	4	3	2	1	0
False Color Th. High							
1	1	1	1	1	1	1	1

False Color Th. High [FCORTHHI : 65h : ffh]

7	6	5	4	3	2	1	0
False Color Th. High							
1	1	1	1	1	1	1	1

Contrast [CONTRAST : 66h : 00h]

7	6	5	4	3	2	1	0
Reserved		Contrast Control		Contrast Control Value Select			
0	0	0	0	0	0	0	0

Contrast Control	00	Disable
	01	Updates the contrast control values.
	11	Enable

This document has a general product description and is subject to change without notice. MagnaChip Semiconductor Ltd. does not assume any responsibility for use of circuits described and no patent licenses are implied.

MagnaChip *Confidential*

Contrast Control Value Select	0000 ~ 0100	Selects the contrast X-point values. (Xpt1 ~ Xpt4)
	0101 ~ 1001	Selects the contrast slope values. (Slp1 ~ Slp5)

Contrast Control Value [CONTVALUE : 67h : 00h]

7	6	5	4	3	2	1	0
Contrast Control Value							
0	0	0	0	0	0	0	0

Special Image Functions

Available functions are mono tone, gray scale, sepia, and negative. Sepia Cb/Cr Value bits and special image functions threshold value register can be used when you want to change Cb and Cr sense of image for sepia mode. Mono value bit and special image functions threshold value register are can be used when you want to change a threshold value determining white and black level at mono tone.

Special Image Functions mode [SPESEL : 68h : 00h]

7	6	5	4	3	2	1	0
Sepia Cb/Cr Value		Mono Value	Reserved		Function Mode		
0	0	0	0	0	0	0	0

Function Mode	000	Normal image (default)
	001	Gray scale image
	010	Sepia tone image
	011	Negative image
	100	Mono tone image
	110	Auto level image
Mono Value	If function mode is mono tone image and this pin is high, using this register can change a threshold value determining white and black level. After set SPESEL to 24h, set SPETHVALUE register to a value which you want.	
Sepia Cb/Cr Value	If you want other image tone, but not sepia, using this bits and SPETHVALUE register is possible. First, set SPESEL to 42h and set SPETHVALUE register to a Cb value which you want. Final, set SPESEL to 82h and set SPETHVALUE register to a Cr value which you want.	
	00	Cb and Cr are set to default value.
	01	Cb value is set to SPETHVALUE register.
	10	Cr value is set to SPETHVALUE register.

Special Image Functions Threshold value [SPETHVALUE : 69h : 00h]

7	6	5	4	3	2	1	0
Special Image Functions Threshold Value							
0	0	0	0	0	0	0	0

Auto Focus Value Control [AF_CTRL : 6ah : a6h]

7	6	5	4	3	2	1	0
State Select	Window Ratio			Reserved		Edge Selection	Focus Value Enable
1	0	1	0	0	1	1	0

Window Weight Control for AF [AF_WinWgt : 6bh : cdh]

7	6	5	4	3	2	1	0
Window Weight Control							
1	1	0	0	1	1	0	1

Edge Threshold for AF [AF_EdgTh : 6ch : 00h]

7	6	5	4	3	2	1	0
Edge Threshold							
0	0	0	0	0	0	0	0

State-decision Threshold for AF [AF_StateThH : 6dh : 00h]

7	6	5	4	3	2	1	0
State-decision Threshold High							
0	0	0	0	0	0	0	0

State-decision Threshold for AF [AF_StateThL : 6eh : 0ah]

7	6	5	4	3	2	1	0
State-decision Threshold Low							
0	0	0	0	1	0	1	0

Current State for AF [AF_State : b0h : ROh]

7	6	5	4	3	2	1	0
Current State							

RO	RO	RO	RO	RO	RO	RO	RO

Focal Value 4th Byte for AF [AF_StateThL : b1h : ROh]

7	6	5	4	3	2	1	0
Focal Value 4th Byte							
RO	RO	RO	RO	RO	RO	RO	RO

Focal Value 3rd Byte for AF [AF_StateThL : b2h : ROh]

7	6	5	4	3	2	1	0
Focal Value 3rd Byte							
RO	RO	RO	RO	RO	RO	RO	RO

Focal Value 2nd Byte for AF [AF_StateThL : b3h : ROh]

7	6	5	4	3	2	1	0
Focal Value 2nd Byte							
RO	RO	RO	RO	RO	RO	RO	RO

Focal Value 1st Byte for AF [AF_StateThL : b4h : RO]

7	6	5	4	3	2	1	0
Focal Value 1st Byte							
RO	RO	RO	RO	RO	RO	RO	RO

Adaptive Noise Filter Control [NFILTERCON : b5h : 04h]

7	6	5	4	3	2	1	0
Enable	Manual Filter Coefficient			Automatic Filter Coefficient			Reserved
0	0	0	0	0	1	0	0

Auto Exposure

Y mean value is continuously calculated every frame, and the integration time value is increased or decreased according to the displacement between current frame Y mean value and target Y mean value.

```
FFh


         ┊ AE Unlock Boundary [68h]

         ┊ AE Lock Boundary [67h]

80h      ┊ AE Target [66h]

         ┊ AE Lock Boundary [67h]


         ┊ AE Unlock Boundary [68h]


0h
     Y Frame Mean
```
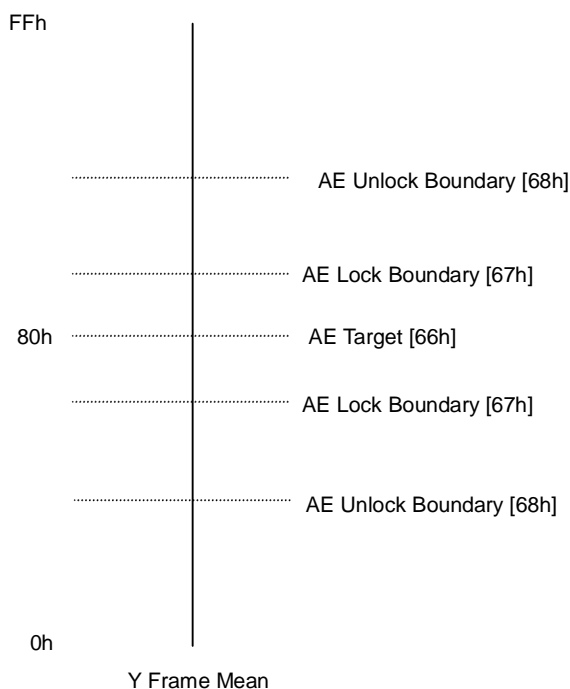
AE Mode Control 1 [AEMODE1 : 70h : 29h]

7	6	5	4	3	2	1	0
User-Defined Time	Anti-Banding Mode	Anti-Banding Min. Break	Ae Window Enable	Time Speed		AE Mode	
0	0	1	0	1	0	0	1

User-Defined Time	This pin make user to be able to put starting value of the integration time. If it sets this pin to high and it writes the integration time, the exposure control is started with the written integration time.

Anti-Banding Mode	When Anti-Banding is enabled, AE initializes Integration Time registers[73h-75h] to 2 x Anti-Banding Step value[7ah-7ch], and integration increment/decrement amount is set to Anti-Banding Step value in order to remove banding noise caused by intrinsic energy waveform of light sources. Banding noise is inherent in CMOS image sensor that adopts rolling shutter scheme for image acquisition. In this mode, AE operates with very large unit, typically a reciprocal of (2 x power line frequency), so that minute integration time tuning is not liable. Therefore, this mode is recommended for only indoor use.
Anti-Banding Min. Break	When AE is still of out lock state despite that AE preamp analog gain update value exceeds preamp minimum gain value(18h) and integration time(73h-75h) is reached to AE Anti-Banding Step(7ah-7ch), integration time(73h-75h) is broken to less than AE Anti-Banding Step(7ah-7ch).
AE Window Enable	AE window mode enables. With this bit set to high, window mode is discarded and full image data is accounted for AE Y frame mean evaluation.
Time Speed	(fast)11 – 10 – 01 – 00(slow)
AE Mode	11 — Gain-Only control mode. Only preamp gain is controlled to get optimum exposure state.
	10 — Time-Only control mode. Only integration time is controlled to get optimum exposure state.
	01 — Time-Gain control mode. Integration time and preamp gain are controlled to get optimum exposure state.
	00 — AE function is disabled

AE Mode Control 2 [AEMODE2 : 71h : edh]

7	6	5	4	3	2	1	0
Gain Speed 1		Gain Speed 2		Time Fine Tune	Gain Fine Tune	Digital Gain Control	Analog Gain Control
1	1	1	0	1	1	0	1

|	
Gain Speed1	This value means the speed of pre-amp. Gain changed when the environment condition moves rapidly from low luminance to high luminance.
Gain Speed2	Gain update speed is specified as follows at the normal condition. (fast)11 – 10 – 01 – 00(slow)
Time Fine Tune	Integration time fine tuning is performed when AE arrive around AE Fine Tune Boundary to settle into AE lock state smoothly.
Gain Fine Tune	Amp gain fine tuning is performed when AE arrive around AE Fine Tune Boundary to settle into AE lock state smoothly.

Digital Gain Control	If this bit is high and Amp Gain register(17h) is less than Anti-Banding Gain Min(91h), digital gain controls the amplitude of Bayer raw data to prevent not to reach the saturation level.(very high luminance compensation)
Analog Gain Control	AE updates Amp Gain register(17h) in order to reach optimum exposure state

AE Windows Weight [AEWINWGT : 72h : cdh]

7	6	5	4	3	2	1	0
Top window		Center window		Bottom window		Side window	
1	1	0	0	1	1	0	1

Value	Weight
00	1
01	1/4
10	1/8
11	1/16

Top(1/16)		
Side(1/4)	Center(1)	Side(1/4)
Bottom(1/16)		
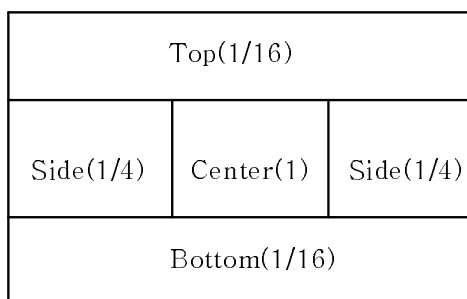
Integration Time High [INTH: 73h : 02h]

7	6	5	4	3	2	1	0
Integration Time Higher							
0	0	0	0	0	0	1	0

Integration Time Middle [INTM: 74h: 71h]

7	6	5	4	3	2	1	0
Integration Time Middle							
0	1	1	1	0	0	0	1

Integration Time Low [INTL: 75h: 03h]

7	6	5	4	3	2	1	0
Integration Time Lower						1)	
0	0	0	0	0	0	1	1

Integration time value register defines the time which active pixel element evaluates photon energy that is converted to digital data output by internal ADC processing. Integration time is equivalent to exposure time of general camera so that integration time needs to be increased in dark environment and decreased according to lighting condition. Maximum integration time is

register maximum value(2^{24}-1) x sensor clock period (SCP = 47.62ns, SCF = 21MHz) = 0.7989sec.
1) And the lower 2bit of Integration Tim[75h] is always masking as to "11", thus Integration time increase/decrease 4code step.

SCF = Sensor Clock Frequency

AE Target Outdoor[LUTARGET1 : 76h : 5ah]

7	6	5	4	3	2	1	0
AE Target Outdoor							
0	1	0	1	1	0	1	0

AE Target Indoor[LUTARGET2 : 77h : 5ah]

7	6	5	4	3	2	1	0
AE Target Indoor							
0	1	0	1	1	0	1	0

AE Lock Boundary [AELOCKFINEBND : 78h : f6h]

7	6	5	4	3	2	1	0
AE Fine Boundary				AE Lock Boundary			
1	1	1	1	0	1	1	0

AE Lock Boundary specifies the displacement of Y Frame Mean value(7dh) from AE Target in which AE goes into LOCK state. With Anti-Banding is enabled, this displacement condition is discarded, and instead AE Speed Unlock Boundary is used as Lock boundary.
AE Fine Boundary specifies the displacement of Y Frame Mean value(7dh) from AE Target in which AE start to tune fine integration time or amp gain in order to goes into lock state smoothly.

AE Unlock Boundary [AEUNLOCKBND : 79h : 2ah]

7	6	5	4	3	2	1	0
AE Unlock Boundary							
0	0	1	0	1	0	1	0

AE Speed Boundary 0 specifies Y Frame Mean displacement from AE Target where integration time increment/decrement speed changes from 2x (integration unit step) to 1x (integration unit step). In anti-banding mode, this boundary is used as lock boundary for exposure control.

AE Anti-Banding Step High [AEINTSTEPH : 7ah : 01h]

7	6	5	4	3	2	1	0
Reserved						Integration Step Higher	
0	0	0	0	0	0	0	1

MagnaChip *Confidential*

AE Anti-Banding Step Middle [AEINTSTEPM : 7bh : 38h]

7	6	5	4	3	2	1	0
Integration Step Middle							
0	0	1	1	1	0	0	0

AE Anti-Banding Step Low [AEINTSTEPL : 7ch : 80h]

7	6	5	4	3	2	1	0
Integration Step Lower							
1	0	0	0	0	0	0	0

AE Anti-Banding Step specifies integration time unit value that AE uses when Anti-Banding is enabled. Anti-Banding Step value is resolved by the following equation.

Anti-Banding Step Value = Sensor Clock Frequency (SCF) / (2x power line frequency)

The recommend value is set with SCF 21MHz, 60Hz power line, that is,

Anti-Banding Step Value = 21MHz / (2 x 60) = 175000(dec) = 2AB98(hex)

AE Integration Time Limit High [AEINTLIMITH : 7dh : 09h]

7	6	5	4	3	2	1	0
AE Integration Time Limit Higher							
0	0	0	0	1	0	0	1

AE Integration Time Limit Middle [AEINTLIMITM : 7eh : c4h]

7	6	5	4	3	2	1	0
AE Integration Time Limit Middle							
1	1	0	0	0	1	0	0

AE Integration Time Limit Low [AEINTLIMITL : 7fh : 00h]

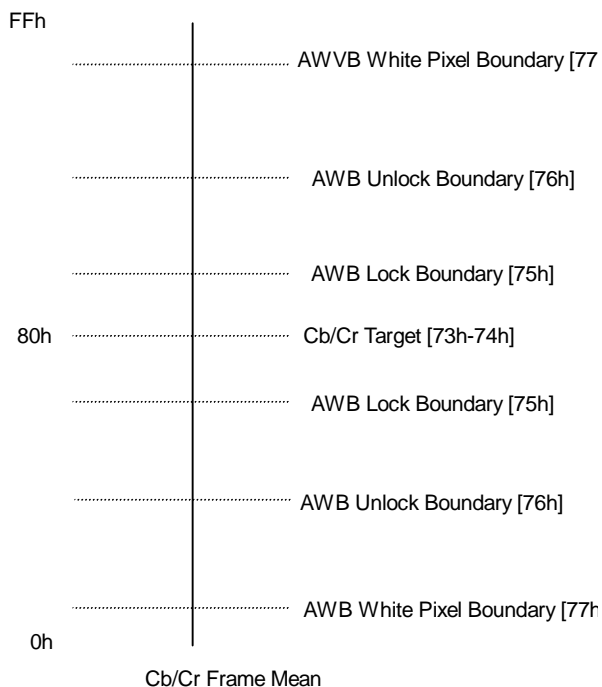| 7	6	5	4	3	2	1	0
AE Integration Time Limit Lower							
0	0	0	0	0	0	0	0

These three registers define the maximum integration time value that is allowed to sensor operation. It is desirable to set the value to multiples of AE Anti-Banding Step to easily operate with Anti-banding mode enabled. The recommend value is set to 5 frames per second with SCF set to 21MHz.

21MHz / 5 = 4200000(dec) = 401640(hex)

Auto White Balance

Cb/Cr frame mean value is calculated every frame and according to Cb/Cr frame mean values' displacement from Cb/Cr white target point, R/B scaling values for R/B data are resolved.

```
FFh
                    AWVB White Pixel Boundary [77

                    AWB Unlock Boundary [76h]

                    AWB Lock Boundary [75h]

80h                 Cb/Cr Target [73h-74h]

                    AWB Lock Boundary [75h]

                    AWB Unlock Boundary [76h]

                    AWB White Pixel Boundary [77h
0h
        Cb/Cr Frame Mean
```

AWB Mode Control [AWBMODE : 80h : 18h]

7	6	5	4	3	2	1	0
Reserved	Test Mode Enable	User Color Matrix Enable	AWB Enable	AWB Full Window Enable	AWB Speed		AWB Low Speed
0	0	0	1	1	0	0	0

|	
Test Mode Enable	This value is using at only simulation or test
User Color Matrix Enable	When this bit set to high, color matrix coefficient[CMA11~CMA33] is used for color space conversion matrix. And if this bit set to low, the equation from CCIR-601 is used.
AWB Enable	Auto White Balance Control Enabled
AWB Full Window Enable	With this bit set to low, AWB windows weight can be changed
AWB Speed	(Fast)11 - 10 - 01 - 00(slow)

AWB Low Speed	With this bit set to high, analog gain speed is decreased to 1/4 of the normal speed

AWB Windows Weight [AWBWINWGT : 82h : 00h]

7	6	5	4	3	2	1	0
Top window		Center window		Bottom window		Side window	
0	0	0	0	0	0	0	0

Value	Weight
00	1
01	1/4
10	1/8
11	1/16

Top(1)		
Side(1)	Center(1)	Side(1)
Bottom(1)		
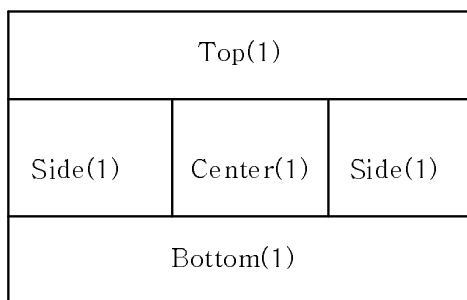
Cb Frame Mean Value [CBTARGT : 83h : 80h]

7	6	5	4	3	2	1	0
Cb Frame Mean							
1	0	0	0	0	0	0	0

This register defines Cb target frame mean value for AWB operation.

Cr Frame Mean Value [CRTARGT : 84h : 80h]

7	6	5	4	3	2	1	0
Cr Frame Mean							
1	0	0	0	0	0	0	0

This register defines Cr target frame mean value for AWB operation.

AWB Lock Boundary [AWBLOCKBND : 85h : 04h]

7	6	5	4	3	2	1	0
Reserved				AWB Lock Boundary			
0	0	0	0	0	1	0	0

It specifies Cb/Cr frame mean values' displacement from Cb/Cr Target (73h-74h) value where AWB goes into LOCK state.

AWB Unlock Boundary [AWBUNLOCKLBND : 86h : 20h]

7	6	5	4	3	2	1	0

AWB Unlock Boundary							
0	0	1	0	0	0	0	0

It specifies Cb/Cr frame mean values' displacement from Cb/Cr Target (73h-74h) where AWB is released from LOCK state. AWB operation retains LOCK state unless Cb/Cr frame mean values' displacement value exceeds this boundary. The value should be larger AWB Lock Boundary.

AWB Cb White Pixel Boundary [CBWHITEBND : 87h : 30h]

7	6	5	4	3	2	1	0
AWB Cb White Pixel Boundary							
0	0	1	1	0	0	0	0

AWB Cr White Pixel Boundary [CRWHITEBND : 88h : 30h]

7	6	5	4	3	2	1	0
AWB Cr White Pixel Boundary							
0	0	1	1	0	0	0	0

AWB C Boundary [AWBCBND : 89h : 30h]

7	6	5	4	3	2	1	0
AWB C Boundary							
0	0	1	1	0	0	0	0

AE State Machine [AEFSM : 8ch : RO]

7	6	5	4	3	2	1	0
AE Mode State				AE Lock state			
RO	RO	RO	RO	RO	RO	RO	RO

AWB State Machine [AWBFSM : 8dh : RO]

7	6	5	4	3	2	1	0
reserved			AE/AWB Lock	Cb Lock State		Cr Lock State	
RO	RO	RO	RO	RO	RO	RO	RO

Lu Frame Mean [LUFMEAN : 8eh : RO]

7	6	5	4	3	2	1	0
Lu Frame Mean							
RO	RO	RO	RO	RO	RO	RO	RO

Cb Frame Mean [CBFMEAN : 8fh : RO]

7	6	5	4	3	2	1	0
			Cb Fram	e Mean			
RO	RO	RO	RO	RO	RO	RO	RO

Cr Frame Mean [CRFMEAN : 90h : RO]

7	6	5	4	3	2	1	0
			Cr Fram	e Mean			
RO	RO	RO	RO	RO	RO	RO	RO

Anti-Banding Gain Min [KLBNDMIN : 91h : 14h]

7	6	5	4	3	2	1	0
			Anti-Bandin	g Gain Min			
0	0	0	1	0	1	0	0

Anti-Banding Gain Max [KLBNDMAX : 92h : 3dh]

7	6	5	4	3	2	1	0
			Anti-Bandin	g Gain Max			
0	0	1	1	1	1	0	1

AWB White Pixel Boundary [AWBWHITE : 93h : ffh]

7	6	5	4	3	2	1	0
			AWB White Pi	xel Boundary			
1	1	1	1	1	1	1	1

AWB Black Pixel Boundary [AWBBLACK : 94h : 00h]

7	6	5	4	3	2	1	0
			AWB Black Pi	xel Boundary			
0	0	0	0	0	0	0	0

AWB Valid Number [AWBNUMBER : 95h : 02h]

7	6	5	4	3	2	1	0
			AWB Vali	d Number			
0	0	0	0	0	0	1	0

Integration-Scan Plane Offset High [INTSCNOFSH : 96h : RO]

7	6	5	4	3	2	1	0
Integration-Scan Offset High							
RO	RO	RO	RO	RO	RO	RO	RO

Integration-Scan Plane Offset Middle [INTSCNOFSM : 97h : RO]

7	6	5	4	3	2	1	0
Integration-Scan Offset Middle							
RO	RO	RO	RO	RO	RO	RO	RO

Integration-Scan Plane Offset Low [INTSCNOFSL : 98h : RO]

7	6	5	4	3	2	1	0
Integration-Scan Offset Low							
RO	RO	RO	RO	RO	RO	RO	RO

AWB Red Gain Maximum Value [AWBRGAINMAX : 9ah : 7f]

7	6	5	4	3	2	1	0
R/B Gain Maximum Value							
0	1	1	1	1	1	1	1

AWB Red Gain Minimum Value [AWBRGAINMIN : 9bh : 00]

7	6	5	4	3	2	1	0
R/B Gain Minimum Value							
0	0	0	0	0	0	0	0

AWB Blue Gain Maximum Value [AWBBGAINMAX : 9ch : 7f]

7	6	5	4	3	2	1	0
R/B Gain Maximum Value							
0	1	1	1	1	1	1	1

AWB Blue Gain Minimum Value [AWBBGAINMIN : 9dh : 00]

7	6	5	4	3	2	1	0
R/B Gain Minimum Value							
0	0	0	0	0	0	0	0

PLL Control Mode A [PCTRA : a0h : 01h]

7	6	5	4	3	2	1	0
Reserved					VCO Power Down	PLL Power Down	Bypass Mode
0	0	0	0	0	0	0	1

VCO Power Down (Active High)	When VCO Power Down is active, VCO does not oscillate. For getting out of VCO Power Down, VCO initialization is required.
PLL Power Down (Active High)	When PLL Power Down is active, digital circuits of PLL do not operate and the charge pump circuit is disabled. Also Bypass Mode or Sleep Mode(SCTRB[4]) register is set to high, PLL goes into sleep.
Bypass Mode	0 PLL output clock is 1/F(ck). 1 PLL output clock is the same of PLL input clock.

* VCO initialization

To ensure the proper operation of the PLL, the activation of VCO initialization signal is required just after the deactivation of the VCO Power Down. During power-up sequence VCO initialization signal is recommended for more than 100ns.

PLL Control Mode B [PCTRB : a1h : 1dh]

7	6	5	4	3	2	1	0
Reserved		Post Divisor		Charge Pump Bias			
0	0	0	1	1	1	1	0

The value of Post Divisor according to the output frequency

Post Divisor	F(ck)	
	Min	**Max**
11	5MHz	12.5MHz
10	10MHz	25MHz
01	20MHz	50MHz
00	40MHz	100MHz

PLL Reference Divisor [PREFDIV : a3h : 01h]

7	6	5	4	3	2	1	0
PLL Reference Divisor							
0	0	0	0	0	0	0	1

PLL Feedback Divisor High [PFDDIVH : a4h : 00h]

7	6	5	4	3	2	1	0
Reserved		PLL Feedback Divisor High					
0	0	0	0	0	0	0	0

PLL Feedback Divisor Low [PFDDIVL : a5h : 02h]

7	6	5	4	3	2	1	0
PLL Feedback Divisor Low							
0	0	0	0	0	0	1	0

The operation frequency of PLL is related to the proportion of Reference(PREFDIV) to Feedback(PFDDIV) Divisor. F(ck) is actually determined by the following equation.

$$F(ck) = \frac{F(ref)*(Feedback\ \ Divisor)}{(Reference\ \ Divisor)}$$

F(ck) : frequency of output
F(ref) : frequency of PLL input
Feedback Divisor : PFDDIV[13:0] + 2
Reference Divisor : PREFDIV[7:0] + 1

Data Output Timing and Interface
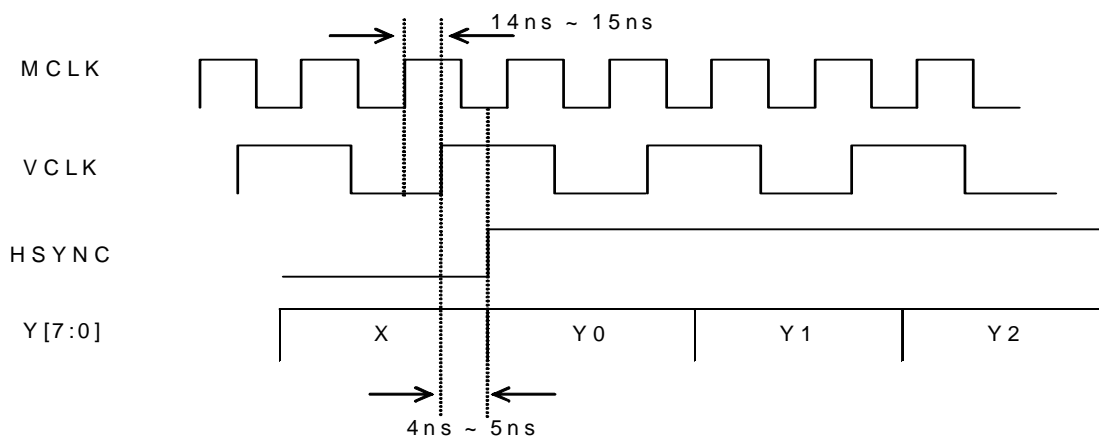
As specified is the above data output timing diagram, the timing margin between video clock pin(VCLK) and data pins(Y[7:0]) is about 4n~5ns. This margin may be sufficient or not according to how much video clock and data pins are delayed internally in the backend chip, respectively. To safely latch the data output in the backend chip, it is recommended that data be latched at negative edge of VCLK.

The above timing margin diagram represents 16bit output interface, but is also valid for 8bit output interface..

Output Data according to Video Mode

Output Data according to Video Mode is controlled by configuring Sensor Control A[01h]. Configurable options are specified again for your reference.

< Video Mode Setting (@ MCLK 21MHz, PLL 2x)

Format / Mode	Sub-Sampling Mode (SCTRA[4])	* YCbCr 4:2:2 SCTRC[7] = 0h OUTFMT[3:0] = 0h * RGB 5:6:5 SCTRC[7] = 0h OUTFMT[3:0] = 4h	Video Clock (MHz)	Frame Rate (± 1fps)	Bayer Output SCTRC[7] = 1h OUTFMT[3:0] = 0h	Video Clock (MHz)	Frame Rate (± 1fps)
SXGA SCTRA[3] = 0h SCTRA[1:0] = 3h	(don't care)	O	42	15	O	21	15
VGA SCTRA[3] = 0h SCTRA[1:0] = 2h	ISP(0)	O	21	15	X	X	X
	Bayer(1)	O	21	28	O	10.5	28
QVGA SCTRA[3] = 0h SCTRA[1:0] = 1h	ISP(0)	O	10.5	15	X	X	X
	Bayer(1)	O	10.5	55	O	5.25	56
4CIF SCTRA[3] = 1h SCTRA[1:0] = 3h	(don't care)	O	42	15	X	X	X
CIF SCTRA[3] = 1h SCTRA[1:0] = 2h	ISP(0)	O	21	15	X	X	X
	Bayer(1)	X	X	X	X	X	X
QCIF SCTRA[3] = 1h SCTRA[1:0] = 1h	ISP(0)	O	10.5	15	X	X	X
	Bayer(1)	X	X	X	X	X	X

Output timings for general configurations are described below. Slot named as "X" means that it is has no meaningful value and should be discarded.

If a clock division(SCTRB[2:0]) is nothing(3'b000), VCLK is equal to MCLK in the case of PLL off, and twice of MCLK in the case of PLL 2x. Output data should be captured when VCLK is falling edge. If you have OUTINV = 0x01, should capture at the rising edge.

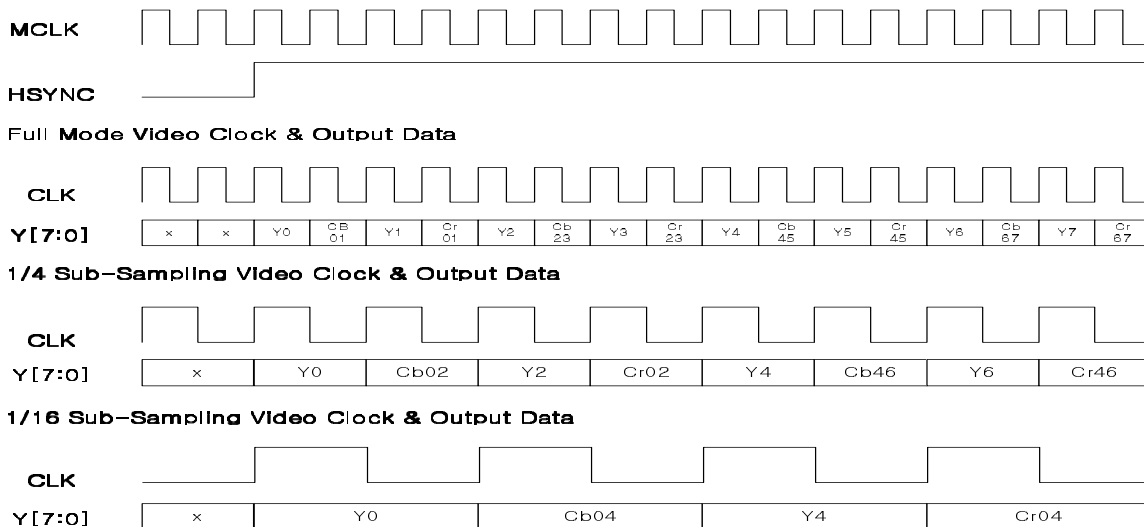**SXVGA(Full), VGA(1/4), QVGA(1/16) Mode** (Operating clock = MCLK, PLL off)

1. **YCbCr 4:2:2 with 8bit output**

   Register bit configurations :

   Sensor Control A : Full or Sub-sampling Mode

   Output Format : 8bit Output, Y First, Cb(Blue) First

MCLK

HSYNC

Full Mode Video Clock & Output Data

CLK

| Y[7:0] | × | × | Y0 | CB 01 | Y1 | Cr 01 | Y2 | Cb 23 | Y3 | Cr 23 | Y4 | Cb 45 | Y5 | Cr 45 | Y6 | Cb 67 | Y7 | Cr 67 |

1/4 Sub-Sampling Video Clock & Output Data

CLK

| Y[7:0] | × | Y0 | Cb02 | Y2 | Cr02 | Y4 | Cb46 | Y6 | Cr46 |

1/16 Sub-Sampling Video Clock & Output Data

CLK
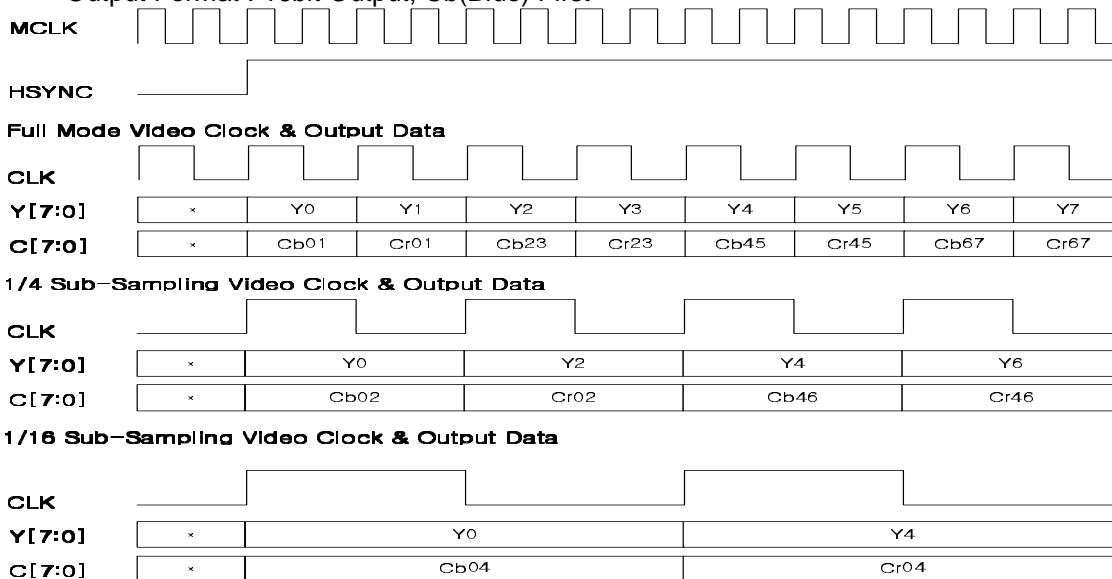
| Y[7:0] | × | Y0 | Cb04 | Y4 | Cr04 |

2. YCbCr 4:2:2 with 16bit output

Register bit configurations :

Sensor Control A : Full or Sub-sampling Mode

Output Format : 16bit Output, Cb(Blue) First

MCLK

HSYNC

Full Mode Video Clock & Output Data

CLK

| Y[7:0] | × | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| C[7:0] | × | Cb01 | Cr01 | Cb23 | Cr23 | Cb45 | Cr45 | Cb67 | Cr67 |

1/4 Sub-Sampling Video Clock & Output Data

CLK

| Y[7:0] | × | Y0 | Y2 | Y4 | Y6 |
| C[7:0] | × | Cb02 | Cr02 | Cb46 | Cr46 |

1/16 Sub-Sampling Video Clock & Output Data

CLK

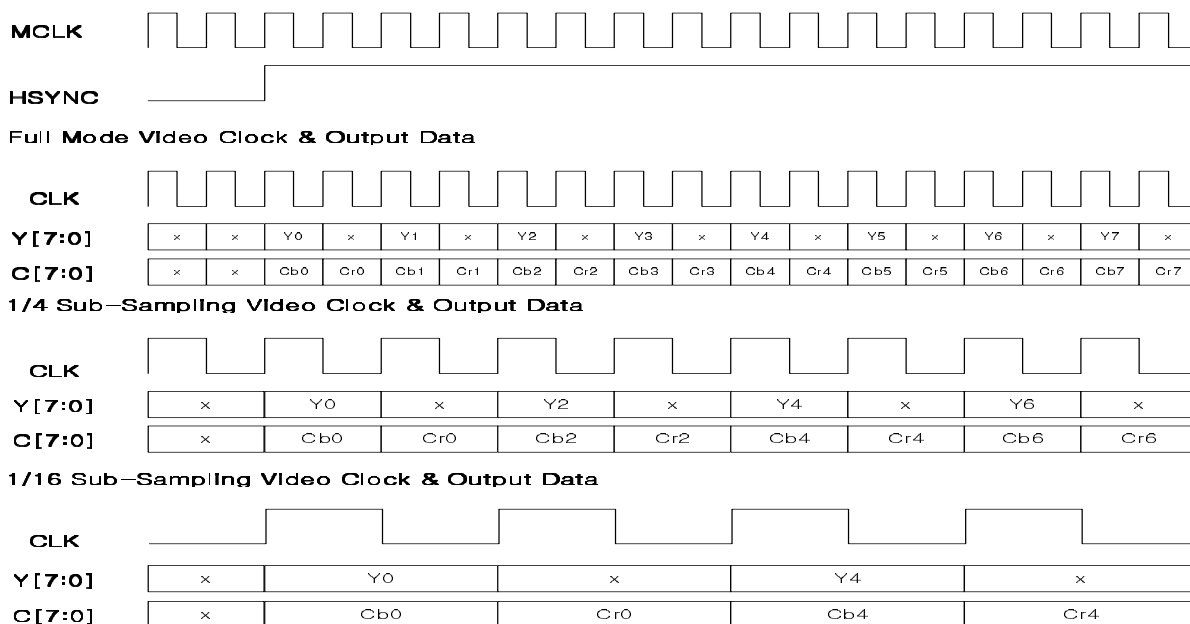| Y[7:0] | × | Y0 | Y4 |
| C[7:0] | × | Cb04 | Cr04 |

3. YCbCr 4:4:4 with 16bit output

Register bit configurations

Sensor Control A : Full or Sub-sampling Mode

Output Format : 16bit Output, Y First, Cb(Blue) First

MCLK

HSYNC

Full Mode Video Clock & Output Data

CLK

| Y[7:0] | × | × | Y0 | × | Y1 | × | Y2 | × | Y3 | × | Y4 | × | Y5 | × | Y6 | × | Y7 | × |

| C[7:0] | × | × | Cb0 | Cr0 | Cb1 | Cr1 | Cb2 | Cr2 | Cb3 | Cr3 | Cb4 | Cr4 | Cb5 | Cr5 | Cb6 | Cr6 | Cb7 | Cr7 |

1/4 Sub−Sampling Video Clock & Output Data

CLK

| Y[7:0] | × | Y0 | × | Y2 | × | Y4 | × | Y6 | × |

| C[7:0] | × | Cb0 | Cr0 | Cb2 | Cr2 | Cb4 | Cr4 | Cb6 | Cr6 |

1/16 Sub−Sampling Video Clock & Output Data

CLK

| Y[7:0] | × | Y0 | × | Y4 | × |

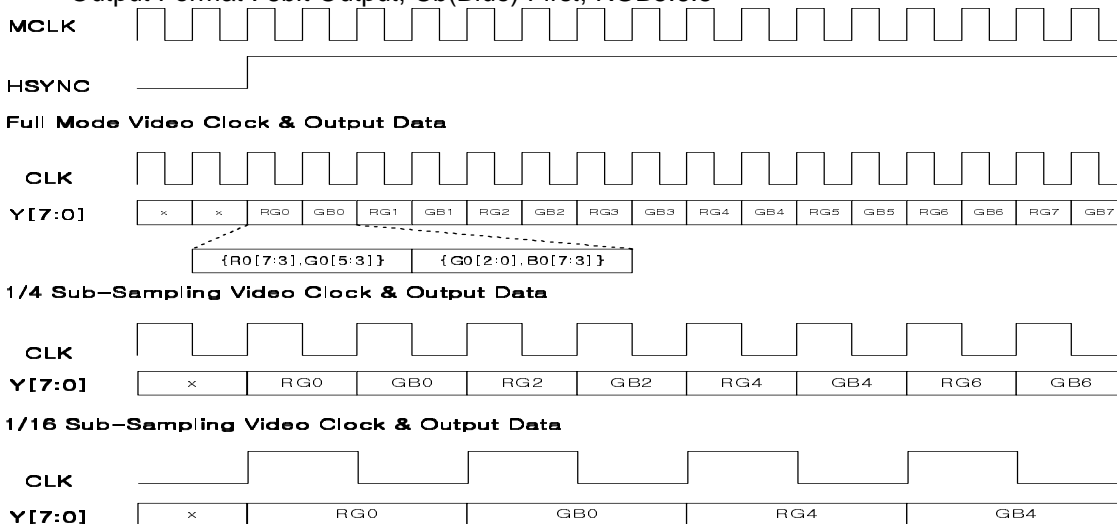| C[7:0] | × | Cb0 | Cr0 | Cb4 | Cr4 |

4. RGB 5:6:5 with 8bit output

Register bit configurations :

Sensor Control A :Full or Sub-sampling Mode

Output Format : 8bit Output, Cb(Blue) First, RGB5:6:5

MCLK

HSYNC

Full Mode Video Clock & Output Data

CLK

| Y[7:0] | × | × | RG0 | GB0 | RG1 | GB1 | RG2 | GB2 | RG3 | GB3 | RG4 | GB4 | RG5 | GB5 | RG6 | GB6 | RG7 | GB7 |

{R0[7:3],G0[5:3]}   {G0[2:0],B0[7:3]}

1/4 Sub−Sampling Video Clock & Output Data

CLK

| Y[7:0] | × | RG0 | GB0 | RG2 | GB2 | RG4 | GB4 | RG6 | GB6 |

1/16 Sub−Sampling Video Clock & Output Data
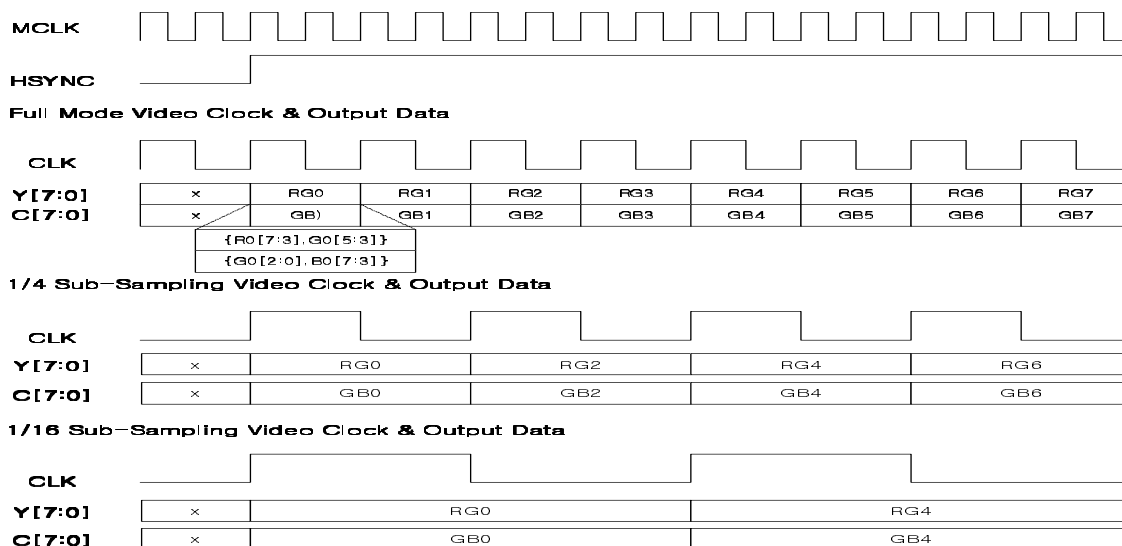
CLK

| Y[7:0] | × | RG0 | GB0 | RG4 | GB4 |

5. RGB 5:6:5 with 16bit output

Register bit configurations :

Sensor Control A : Full or Sub-sampling Mode

Output Format : 16bit Output, Cb(Blue) First, RGB5:6:5

MCLK

HSYNC

Full Mode Video Clock & Output Data

CLK									
Y[7:0]	×	RG0	RG1	RG2	RG3	RG4	RG5	RG6	RG7
C[7:0]	×	GB) GB1	GB2	GB3	GB4	GB5	GB6	GB7

{R0[7:3],G0[5:3]}
{G0[2:0],B0[7:3]}

1/4 Sub-Sampling Video Clock & Output Data

CLK					
Y[7:0]	×	RG0	RG2	RG4	RG6
C[7:0]	×	GB0	GB2	GB4	GB6

1/16 Sub-Sampling Video Clock & Output Data

CLK			
Y[7:0]	×	RG0	RG4
C[7:0]	×	GB0	GB4

6. RGB 4:4:4 with 16bit output

Register bit configurations :

Sensor Control A : Full or Sub-sampling Mode

Output Format : 16bit Output, Cb(Blue) First, RGB4:4:4

MCLK

HSYNC

Full Mode Video Clock & Output Data

CLK																	
Y[7:0]	×	×	G0	×	G1	×	G2	×	G3	×	G4	×	G5	×	G6	×	G7	×
C[7:0]	×	×	B0	R0	B1	R1	B2	R2	B3	R3	B4	R4	B5	R5	B6	R6	B7	R7

1/4 Sub-Sampling Video Clock & Output Data

CLK									
Y[7:0]	×	G0	×	G2	×	G4	×	G6	×
C[7:0]	×	B0	R0	B2	R2	B4	R4	B6	R6

1/16 Sub-Sampling Video Clock & Output Data

CLK				
Y[7:0]	×	G0	×	G4	×
C[7:0]	×	B0	R0	B4	R4

4CIF(Full) or CIF(1/4) Mode (Operating clock = MCLK, PLL off)

1. YCbCr 4:2:2 with 8bit output

Register bit configurations :

Sensor Control A : CIF Mode, Full or Sub-sampling Mode

This document has a general product description and is subject to change without notice. MagnaChip Semiconductor Ltd. does not assume any responsibility for use of circuits described and no patent licenses are implied.
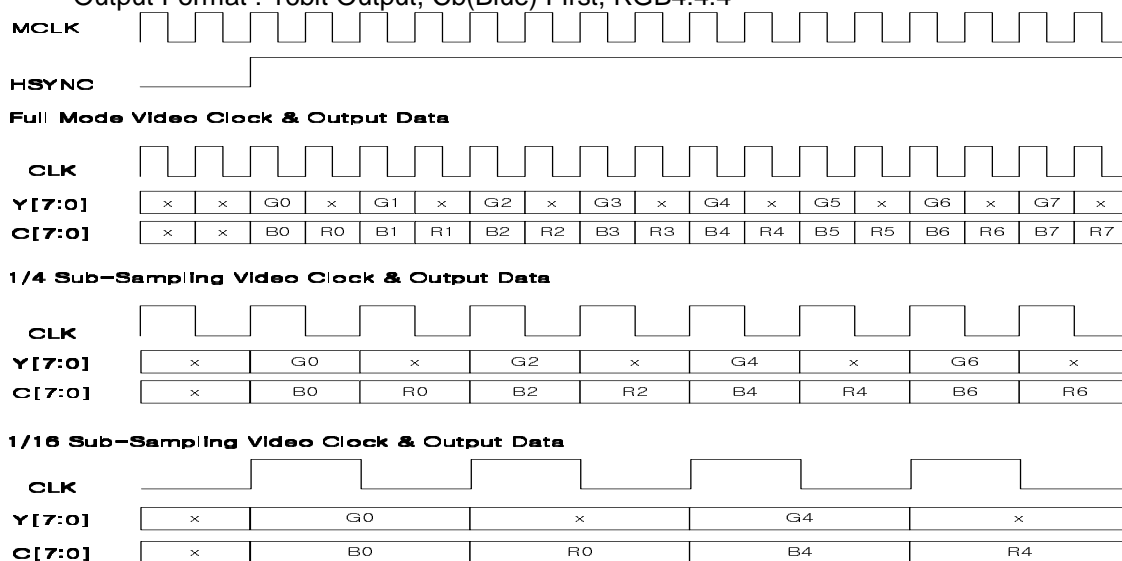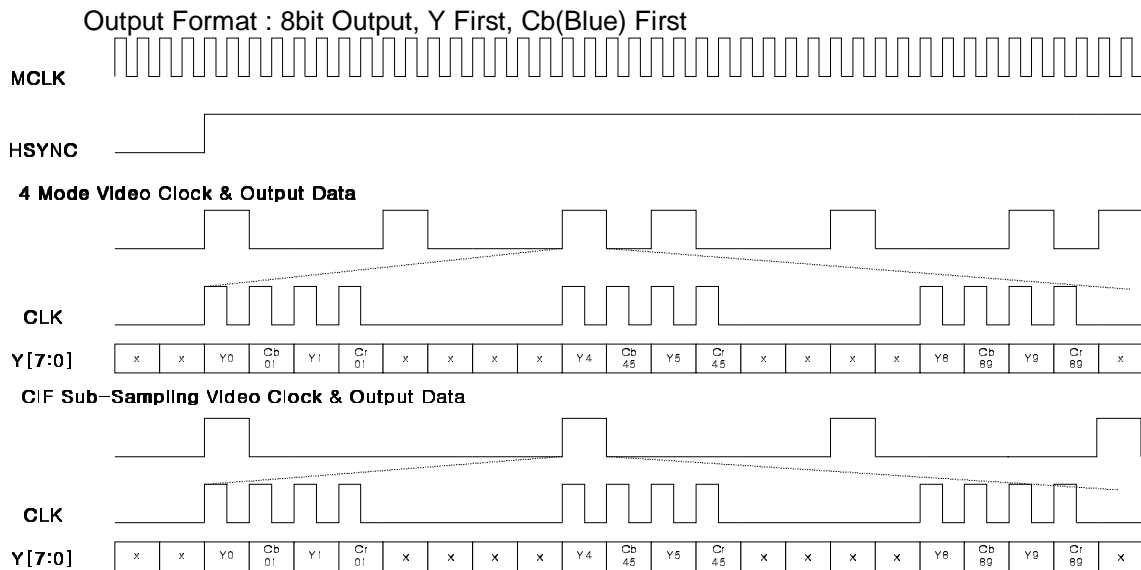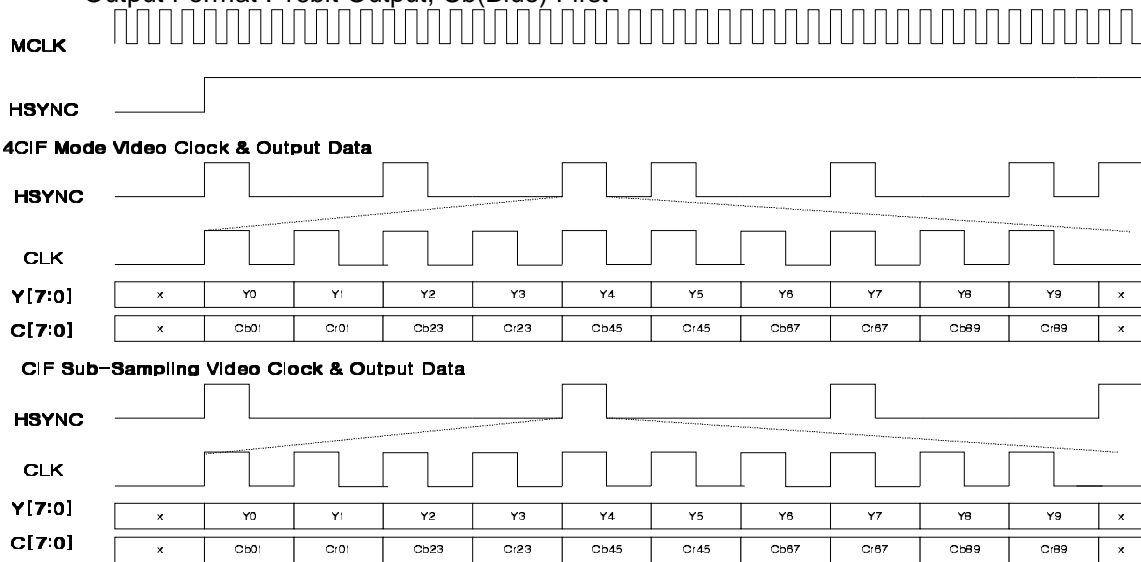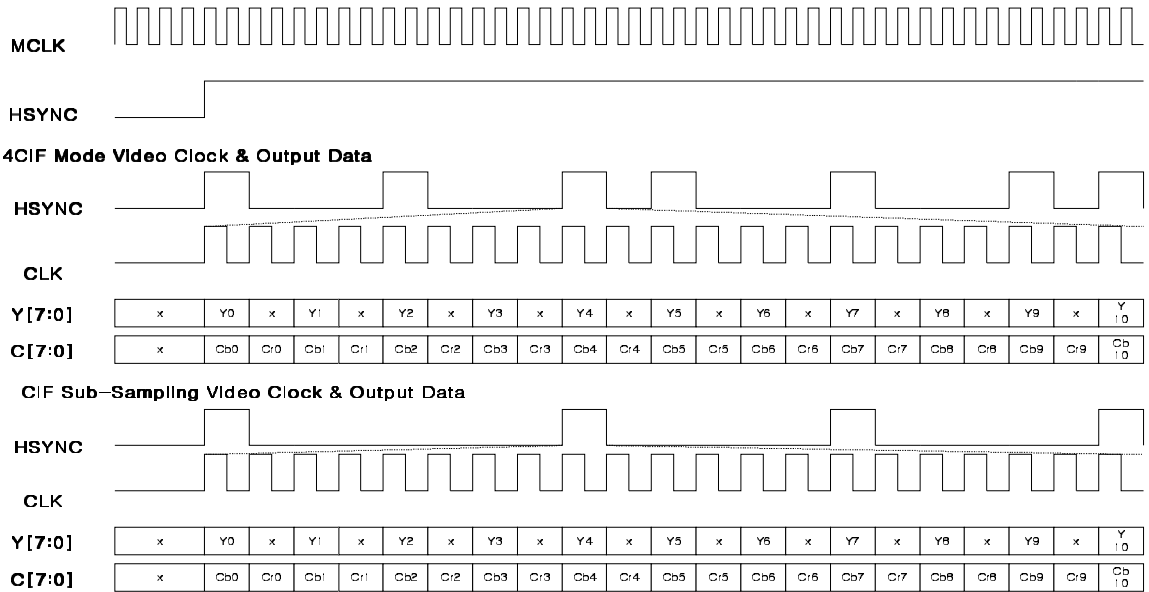
Output Format : 8bit Output, Y First, Cb(Blue) First

MCLK

HSYNC

4 Mode Video Clock & Output Data

CLK

Y[7:0] | x | x | Y0 | Cb 01 | Y1 | Cr 01 | x | x | x | x | Y4 | Cb 45 | Y5 | Cr 45 | x | x | x | x | Y8 | Cb 89 | Y9 | Cr 89 | x

CIF Sub-Sampling Video Clock & Output Data

CLK

Y[7:0] | x | x | Y0 | Cb 01 | Y1 | Cr 01 | x | x | x | x | Y4 | Cb 45 | Y5 | Cr 45 | x | x | x | x | Y8 | Cb 89 | Y9 | Cr 89 | x

2. YCbCr 4:2:2 with 16bit output

Register bit configurations :

Sensor Control A : CIF Mode, Full or Sub-sampling Mode

Output Format : 16bit Output, Cb(Blue) First

MCLK

HSYNC

4CIF Mode Video Clock & Output Data

HSYNC

CLK

Y[7:0] | x | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 | Y8 | Y9 | x
C[7:0] | x | Cb01 | Cr01 | Cb23 | Cr23 | Cb45 | Cr45 | Cb67 | Cr67 | Cb89 | Cr89 | x

CIF Sub-Sampling Video Clock & Output Data

HSYNC

CLK

Y[7:0] | x | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 | Y8 | Y9 | x
C[7:0] | x | Cb01 | Cr01 | Cb23 | Cr23 | Cb45 | Cr45 | Cb67 | Cr67 | Cb89 | Cr89 | x

3. YCbCr 4:4:4 with 16bit output

Register bit configurations :

Sensor Control A : CIF Mode, Full or Sub-sampling Mode

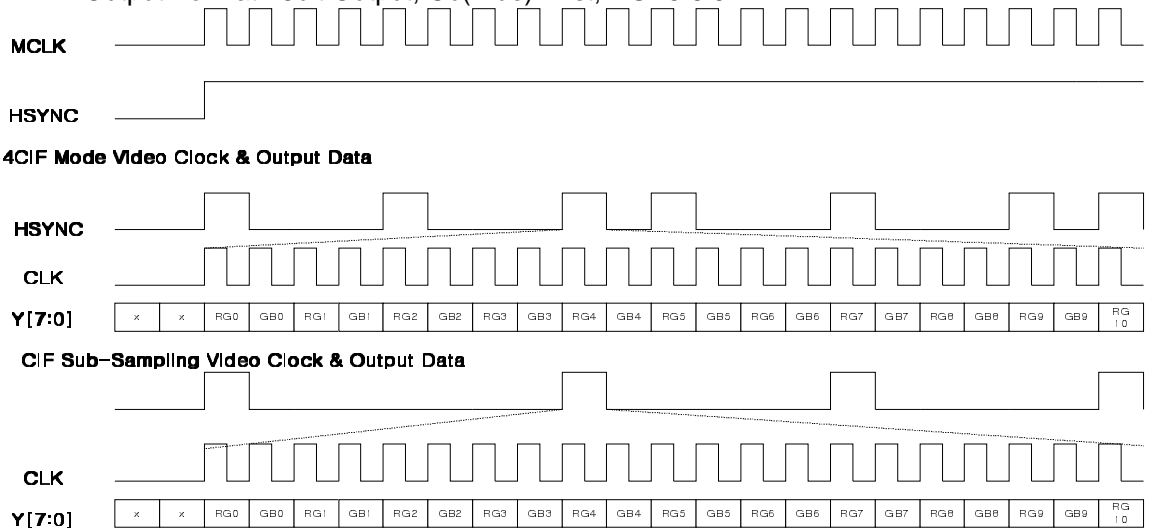Output Format : 16bit Output, Y First, Cb(Blue) First

4. RGB 5:6:5 with 8bit output

Register bit configurations :

Sensor Control A : CIF Mode, Full or Sub-sampling Mode

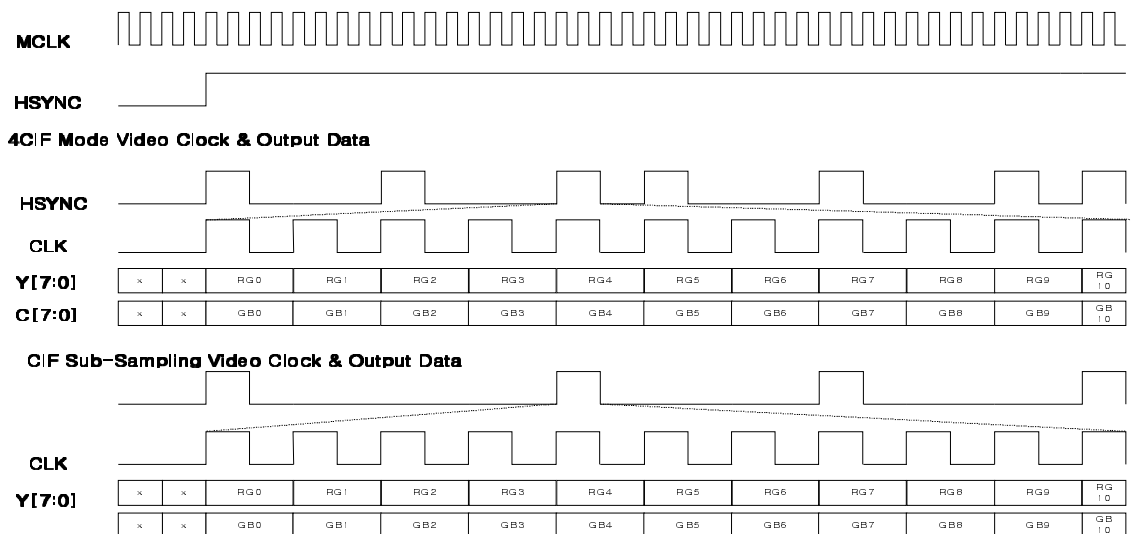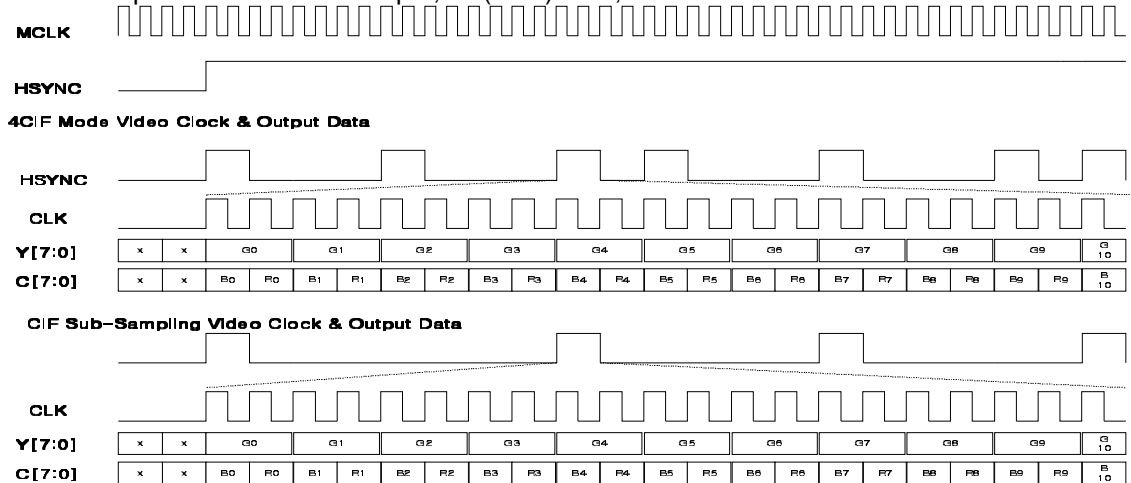Output Format : 8bit Output, Cb(Blue) First, RGB5:6:5

5. RGB 5:6:5 with 16bit output

Register bit configurations :

Sensor Control A : CIF Mode, Full or Sub-sampling Mode
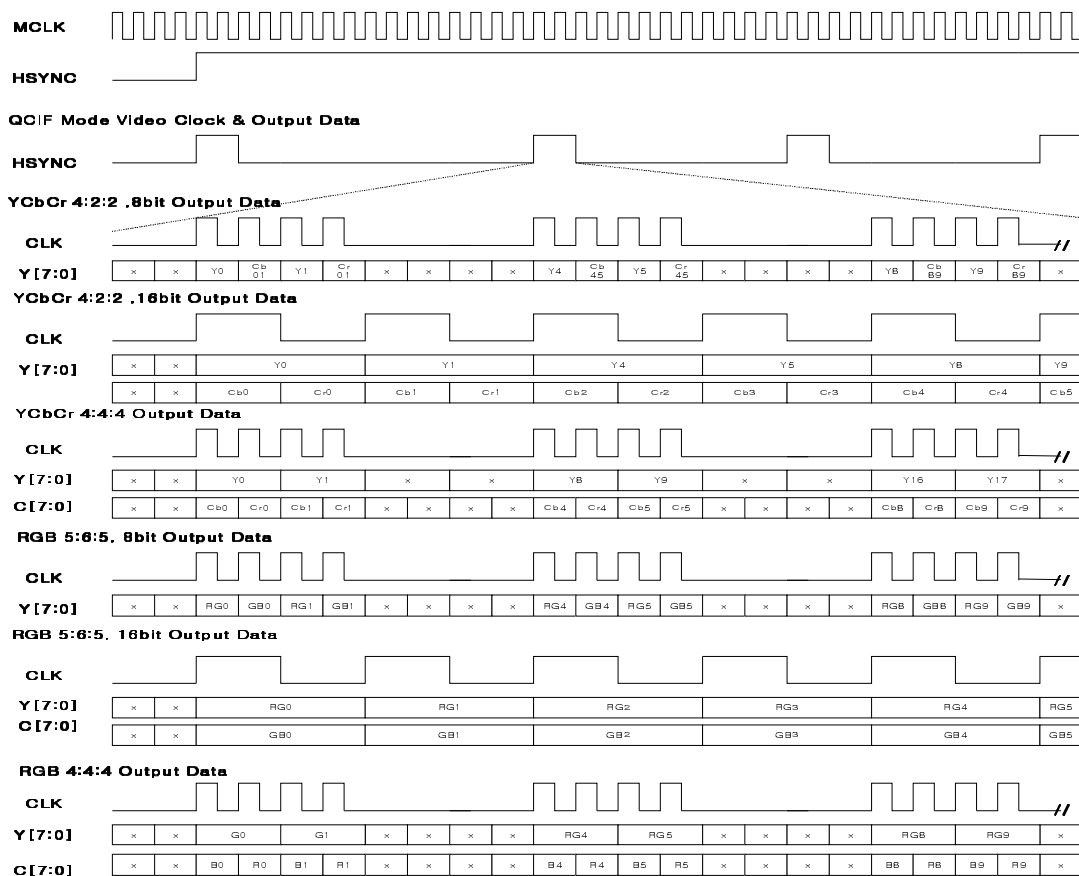
Output Format : 16bit Output, Cb(Blue) First, RGB5:6:5

MCLK

HSYNC

4CIF Mode Video Clock & Output Data

HSYNC

CLK

Y[7:0] | x | x | RG0 | RG1 | RG2 | RG3 | RG4 | RG5 | RG6 | RG7 | RG8 | RG9 | RG10

C[7:0] | x | x | GB0 | GB1 | GB2 | GB3 | GB4 | GB5 | GB6 | GB7 | GB8 | GB9 | GB10

CIF Sub-Sampling Video Clock & Output Data

CLK

Y[7:0] | x | x | RG0 | RG1 | RG2 | RG3 | RG4 | RG5 | RG6 | RG7 | RG8 | RG9 | RG10

| x | x | GB0 | GB1 | GB2 | GB3 | GB4 | GB5 | GB6 | GB7 | GB8 | GB9 | GB10

6. RGB 4:4:4 with 16bit output

Register bit configurations :

Sensor Control A : CIF Mode, Full or Sub-sampling Mode

Output Format : 16bit Output, Cb(Blue) First, RGB4:4:4

MCLK

HSYNC

4CIF Mode Video Clock & Output Data

HSYNC

CLK

Y[7:0] | x | x | G0 | G1 | G2 | G3 | G4 | G5 | G6 | G7 | G8 | G9 | G10

C[7:0] | x | x | B0 | R0 | B1 | R1 | B2 | R2 | B3 | R3 | B4 | R4 | B5 | R5 | B6 | R6 | B7 | R7 | B8 | R8 | B9 | R9 | B10

CIF Sub-Sampling Video Clock & Output Data

CLK

Y[7:0] | x | x | G0 | G1 | G2 | G3 | G4 | G5 | G6 | G7 | G8 | G9 | G10

C[7:0] | x | x | B0 | R0 | B1 | R1 | B2 | R2 | B3 | R3 | B4 | R4 | B5 | R5 | B6 | R6 | B7 | R7 | B8 | R8 | B9 | R9 | B10

QCIF(1/16) Mode (Operating clock = MCLK, PLL off)

Register bit configurations :

Sensor Control A : CIF Mode, Bayer Sub-sampling, 1/16 Sub-sampling Mode

Output Format : 8bit Output, Y First, Cb(Blue) First

MCLK

HSYNC

QCIF Mode Video Clock & Output Data

HSYNC

YCbCr 4:2:2 ,8bit Output Data

CLK

Y[7:0] | × | × | Y0 | Cb 01 | Y1 | Cr 01 | × | × | × | × | Y4 | Cb 45 | Y5 | Cr 45 | × | × | × | × | YB | Cb B9 | Y9 | Cr B9 | ×

YCbCr 4:2:2 ,16bit Output Data

CLK

Y[7:0] | × | × | Y0 | Y1 | Y4 | Y5 | YB | Y9

C | × | × | Cb0 | Cr0 | Cb1 | Cr1 | Cb2 | Cr2 | Cb3 | Cr3 | Cb4 | Cr4 | Cb5

YCbCr 4:4:4 Output Data

CLK

Y[7:0] | × | × | Y0 | Y1 | × | × | YB | Y9 | × | × | Y16 | Y17 | ×

C[7:0] | × | × | Cb0 | Cr0 | Cb1 | Cr1 | × | × | × | × | Cb4 | Cr4 | Cb5 | Cr5 | × | × | × | × | CbB | CrB | Cb9 | Cr9 | ×

RGB 5:6:5, 8bit Output Data

CLK

Y[7:0] | × | × | RG0 | GB0 | RG1 | GB1 | × | × | × | × | RG4 | GB4 | RG5 | GB5 | × | × | × | × | RGB | GBB | RG9 | GB9 | ×

RGB 5:6:5, 16bit Output Data

CLK

Y[7:0] | × | × | RG0 | RG1 | RG2 | RG3 | RG4 | RG5

C[7:0] | × | × | GB0 | GB1 | GB2 | GB3 | GB4 | GB5

RGB 4:4:4 Output Data

CLK

Y[7:0] | × | × | G0 | G1 | × | × | × | × | RG4 | RG5 | × | × | × | × | RGB | RG9 | ×

C[7:0] | × | × | B0 | R0 | B1 | R1 | × | × | × | × | B4 | R4 | B5 | R5 | × | × | × | × | BB | RB | B9 | R9 | ×

Bayer Data Format (Operating clock = MCLK, PLL off)

Output Format is controlled by configuring Sensor Control C(SCTRC) and Output Format(OUTFMT) register. Configurable options are specified again for your reference.

8bit/16bit raw or gamma-corrected Bayer output

When Bayer output mode is selected, Window Width x Window Height raw image data is produced with the following sequence. After VSYNC goes low state, the first HSYNC line of a frame is activated with B pixel data appearing first when both of Column Start Address and Row Start Address are even.

MCLK

HSYNC

8bit Bus Bayer Mode Video Clock & 8bit Output Data (Even)

CLK

Y[7:0] | x | B0 | G0 | B1 | G1 | B2 | G2 | B3 | G3 | B4 | G4 | B5 |

| B0[10:3] | G0[10:3] |

8bit Bus Bayer VGA Mode Video Clock & 8bit Output Data (Even)

| x | B0 | G0 | B1 | G1 | B2 | G2 |

8bit Bus Bayer QVGA Mode Video Clock & 8bit Output Data (Even)

| x | B0 | G0 | B1 |

8bit Bus Bayer Mode Video Clock & 11bit Output Data

CLK

Y[7:0] | x | B0 | G0 | B1 | G1 | B2 | G2 | B3 | G3 | B4 | G4 | B5 |

| B0[10:3] | B0[2:0] |

16bit Bus Bayer Mode Video Clock & 11bit Output Data

Y[7:0] | x | B0[10:3] | G0 | B1 | G1 | B2 | G2 | B3 | G3 | B4 | G4 | B5 |

C[7:0] | x | B0[2:0] | G0 | B1 | G1 | B2 | G2 | B3 | G3 | B4 | G4 | B5 |
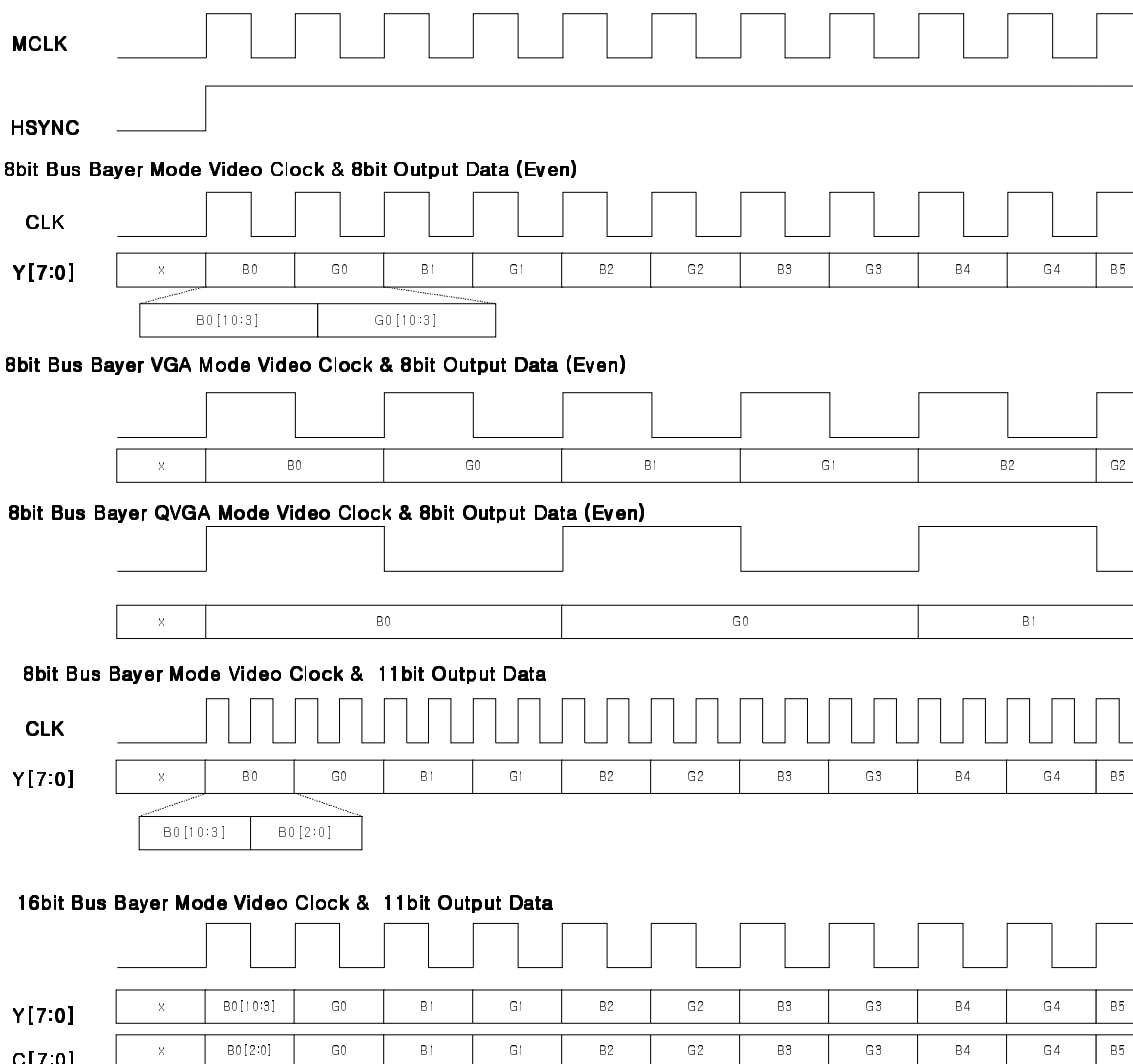
Window mode and image size

Mode	Width	Height
Full(SXGA)	1280	960
1/4(VGA)	640	480
1/16(QVGA)	320	240
4CIF	704	576
CIF	352	288
QCIF	176	144

※ **Note:** The 'Width' means the number of VCLK during HSYNC is active high and the 'Height' means the number of HSYNC during VSYNC is active low.

I2C Chip Interface

The serial bus interface consists of the SDA(serial data) and SCK(serial clock) pins. HV7161SP sensor can operate only as a slave. The SCK only controls the serial interface. However, MCLK should be supplied and RESET should be high signal during controlling the serial interface. The Start condition is that logic transition (High to Low) on the SDA pin while the SCK pin is at high state. The Stop condition is that logic transition (Low to High) on the SDA pin while the SCK pin is at high state. To generate Acknowledge signal, the Sensor drives the SDA low when the SCK pin is at high state. Every byte consists of 8 bits. Each byte transferred on the bus must be followed by an Acknowledge. The most significant bit of the byte should always be transmitted first.
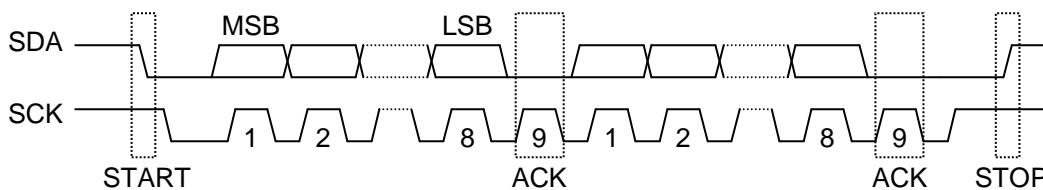
Register Write Sequences

One Byte Write

S	22H	A	01H	A	03H	A	P
*1	*2	*3	*4	*5	*6	*7	*8
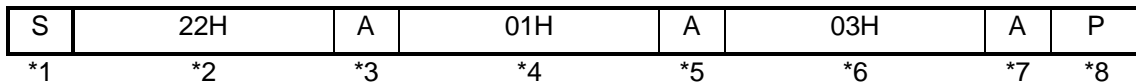
Set "Sensor Control A" register into Window mode

*1. Drive: I2C start condition

*2. Drive: 22H(001_0001 + 0) [device address + R/W bit]

*3. Read: acknowledge from sensor

*4. Drive: 01H [sub-address]

*5. Read: acknowledge from sensor

*6. Drive: 03H [Video Mode : SXGA]

*7. Read: acknowledge from sensor

*8. Drive: I2C stop condition

Multiple Byte Write using Auto Address Increment

S	22H	A	76H	A	70H	A	70H	A	P
*1	*2	*3	*4	*5	*6	*7	*8	*9	*10
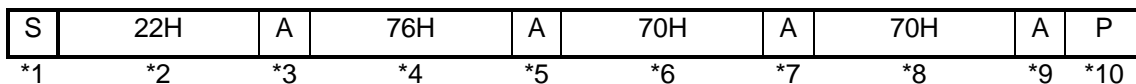
Set "LuTarget1, LuTarget2" register as 70H, 70H with auto address increment

*1. Drive: I2C start condition

*2. Drive: 22H(001_0001 + 0) [device address + R/W bit]

*3. Read: acknowledge from sensor

*4. Drive: 76H [sub-address]
*5. Read: acknowledge from sensor
*6. Drive: 70H [LuTarget1]
*7. Read: acknowledge from sensor
*8. Drive: 70H [LuTarget2]
*9. Read: acknowledge from sensor
*10. Drive: I2C stop condition

Register Read Sequence

S	22H	A	50H	A	S	23H	A	Data of 50H	A	P
*1	*2	*3	*4	*5	*6	*7	*8	*9	*10	*11

Read "Gamma Slope 6" register from HV7161SP

*1. Drive: I2C start condition
*2. Drive: 22H(001_0001 + 0) [device address + R/W bit(be careful. R/W=0)]
*3. Read: acknowledge from sensor
*4. Drive: 50H [sub-address]
*5. Read: acknowledge from sensor
*6. Drive: I^{2}C start condition
*7. Drive: 23H(001_0001 + 1) [device address + R/W bit(be careful. R/W=1)]
*8. Read: acknowledge from sensor
*9. Read: Read "Gamma Slope 6" from sensor
*10. Drive: acknowledge to sensor. If there is more data bytes to read, SDA should be driven to low and data read states(*9, *10) is repeated. Otherwise SDA should be driven to high to prepare for the read transaction end.
*11. Drive: I2C stop condition

AC/DC Characteristics

Absolute Maximum Ratings

Symbol	Parameter	Units	Min.	Max.
Vpp:ph	I/O and pixel block supply voltage	Volts	-0.3	3.62
Vpp:p	Internal analog and digital supply voltage	Volts	-0.3	2.5
Vipp	Input signal voltage	Volts	-0.3	3.3
Top	Operating Temperature	°C	-10	50
Tst	Storage Temperature	°C	-30	80

※ Caution: Stresses exceeding the absolute maximum ratings may induce failure.

DC Operating Conditions

Symbol	Parameter	Units	Min.	Typ.	Max.	Load[pF]
Vdd:ph	I/O and pixel block supply voltage	Volt	2.3	2.5 to 2.8	2.9	
Vdd:p	Internal analog an digital operation supply voltage	Volt	1.6	1.8	2.0	
Vih	Input voltage logic "1"	Volt	2.0			30[pF]
Vil	Input voltage logic "0"	Volt			0.8	30[pF]
Voh	Output voltage logic "1"	Volt	2.4			30[pF]
Vol	Output voltage logic "0"	Volt			0.4	30[pF]
Iih	Input High Current	uA	-10		10	30[pF]
Iil	Input Low Current	uA	-10		10	30[pF]
Ta	Ambient operating temperature	°C	-10	25	50	

AC Operating Conditions

Symbol	Parameter	Max Operation Frequency	Units	Notes
MCLK	Main clock frequency	21	MHz	1,2
SCK	I^2C clock frequency	400	KHz	3

1. MCLK may be divided by internal clock division logic for easy integration with high speed video codec system.
2. Frame Rate : 15 frames/sec at 21Mhz, HBLANK = 208, VBLANK = 8
3. SCK is driven by host processor. For the detail serial bus timing, refer to I2C chip interface section

Output AC Characteristics

All output timing delays are measured with output load 30[pF]. Output delay includes the internal clock path delay and output driving delay that changes in respect to the output load, the operating environment, and a board design. Due to the variable valid time delay of the output, video output signals Y[7:0], C[7:0], HSYNC, and VSYNC may be latched in the negative edge of VCLK for the stable data transfer between the image sensor and video codec.

6ns
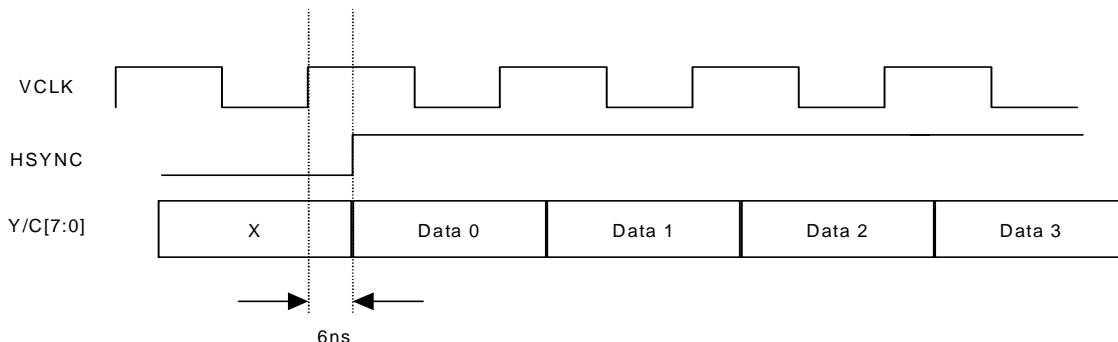
I2C Bus Timing
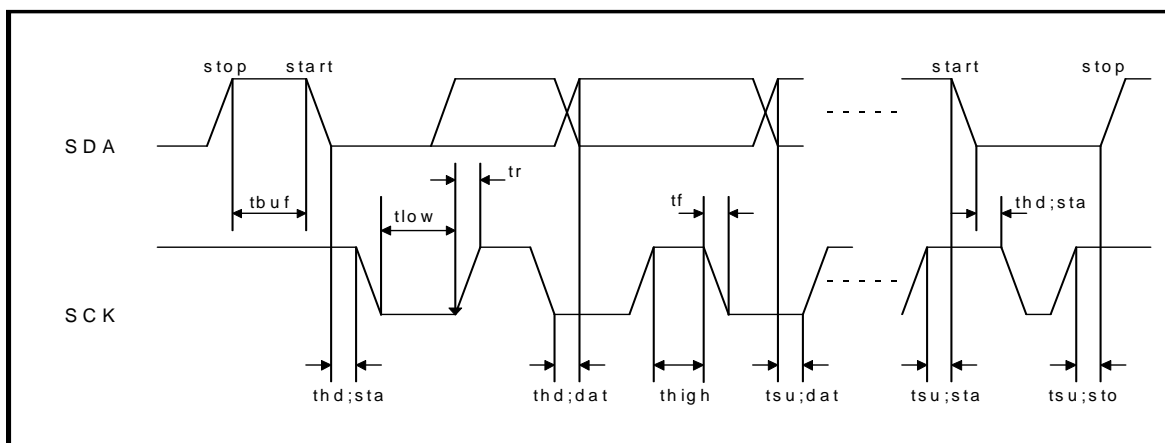
Parameter	Symbol	Min.	Max.	Unit
SCK clock frequency	f_{sck}	0	400	KHz
Time that I^{2}C bus must be free before a new transmission can start	t_{buf}	1.2	-	us
Hold time for a START	$t_{hd};s_{ta}$	1.0	-	us
LOW period of SCK	t_{low}	1.2	-	us
HIGH period of SCK	t_{high}	1.0	-	us
Setup time for START	$t_{su};s_{ta}$	1.2	-	us
Data hold time	$t_{hd};d_{at}$	0.1	-	us
Data setup time	$t_{su};d_{at}$	250	-	ns
Rise time of both SDA and SCK	t_r	-	300	ns
Fall time of both SDA and SCK	t_f	-	300	ns
Setup time for STOP	$t_{su};s_{to}$	1.2	-	us
Capacitive load of SCK/SDA	C_b	-	-	pf

Electro-Optical Characteristics

Parameter	Units	Min.	Typ.	Max.	Note
G Sensitivity	mV / lux·sec		1700		
Dark Signal	Code		2.13		0 ~ 255
Saturation	Code		190		0 ~ 255
Dynamic range	dB		48		
SNR	dB			40	
Power Consumption (25℃) [1]	mW	51	73	95	

Note 1). Others except power consumption are tested under below electro-optical test condition, and the power consumption is tested under default operating condition at MCLK 25MHz and PLL off.

Electro-Optical Test Condition (Temperature = 50℃)

| Parameter	Description
G Sensitivity	preamp gain = 2x, R/G/B gain = 1x, 30lux, integration time @ 128code
Dark Signal	preamp gain = 2x, R/G/B gain = 1x, 1/10sec, 0lux
Saturation	preamp gain = 1x, R/G/B gain = 1x, 1/10sec, 100lux
Dynamic range	(Temperature = 30℃)
SNR	(Temperature = 30℃)
DC and AC conditions	Internal 1.8V and 2.6V, and I/O 2.6V @ MCLK 25Mhz, PLL off

- Color temperature of light source: 3200K / IR cut-off filter (CM-500S, 1mm thickness) is used.

Typical Application

U1
HV7161SP_CLCC48
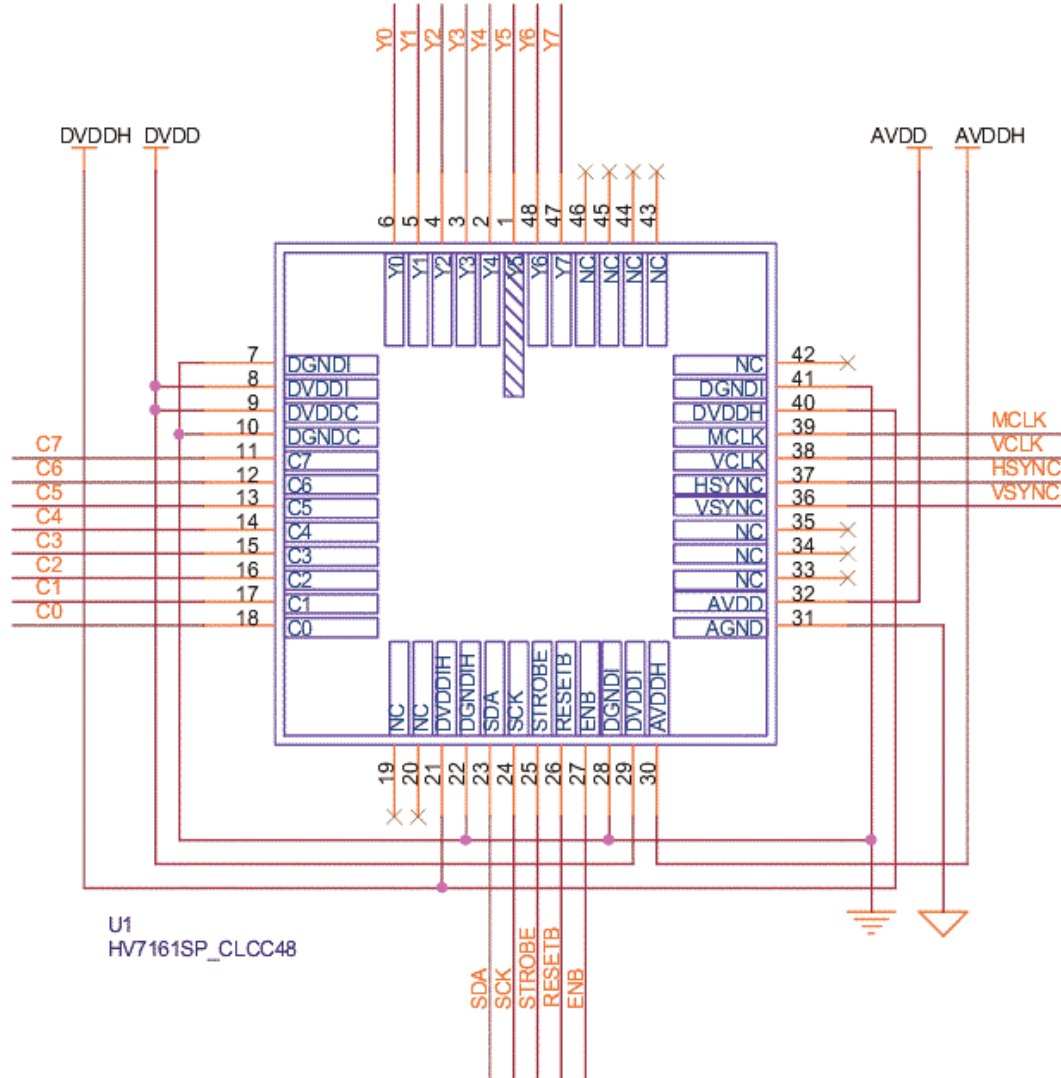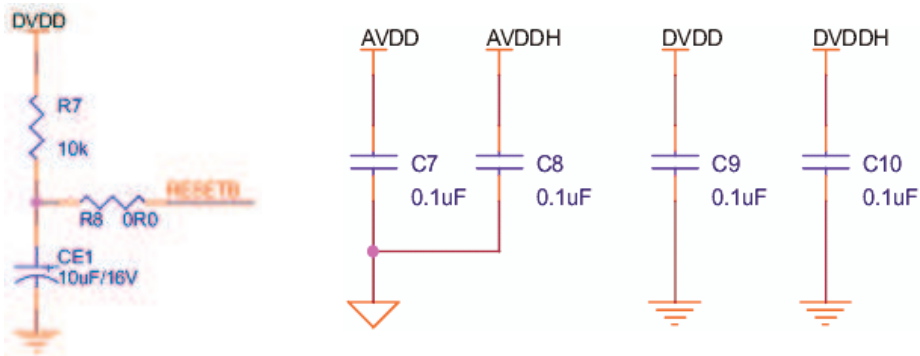
CLCC Package Specification

MagnaChip Semiconductor Ltd.
System IC SP Div.

* Contact Point *

CIS Marketing Team

15Floor, MagnaChip Youngdong Bldg. 891 Daechi-Dong Kangnam-Gu Seoul 135-738 Republic of Korea

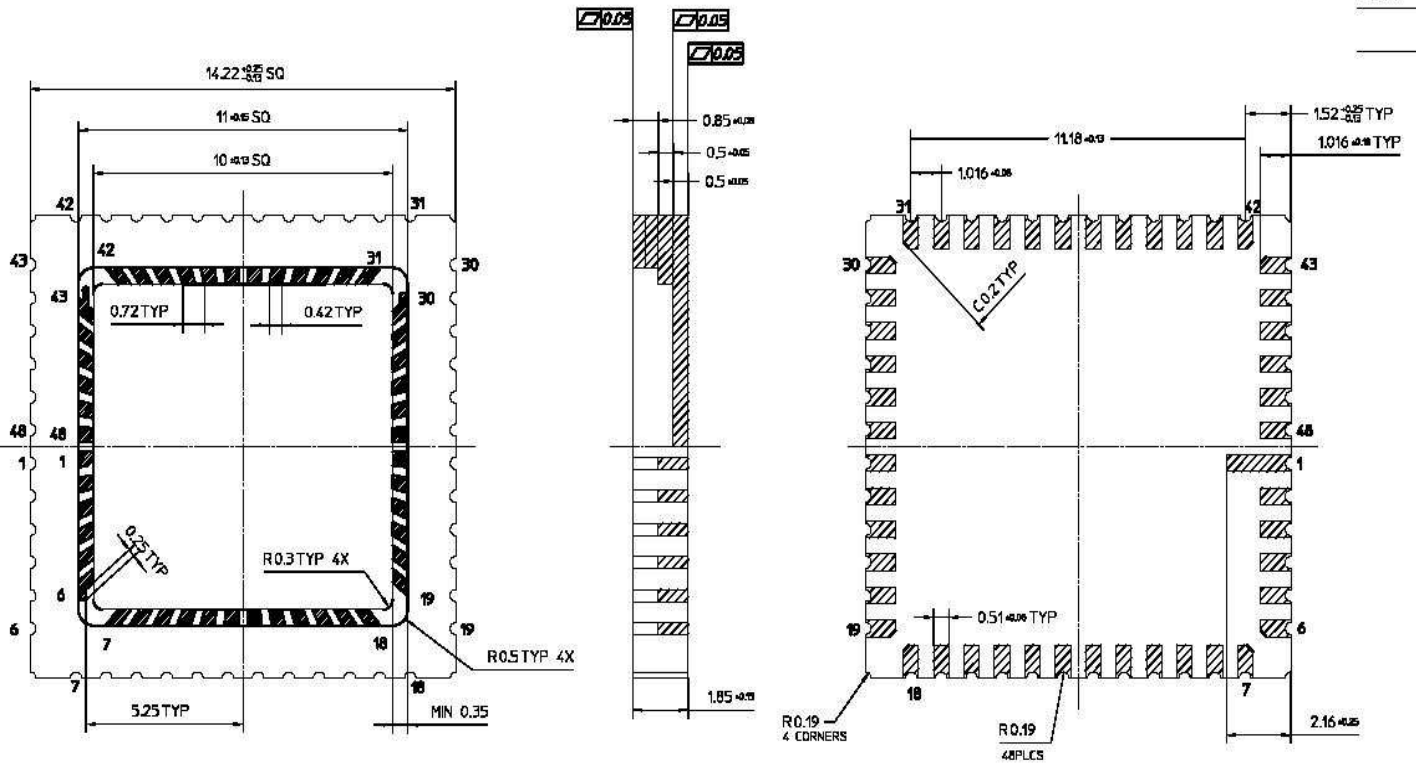Tel: 82-2-3459-5579

Fax: 82-2-3459-5580

E-mail : suyeon.moon@MagnaChip.com

This document has a general product description and is subject to change without notice. MagnaChip Semiconductor Ltd. does not assume any responsibility for use of circuits described and no patent licenses are implied.