FAIRCHILD SEMICONDUCTOR™

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FIN1019
3.3V LVDS High Speed Differential Driver/Receiver (Preliminary)

General Description

This driver and receiver pair are designed for high speed interconnects utilizing Low Voltage Differential Signaling (LVDS) technology. The driver translates LVTTL signals to LVDS levels with a typical differential output swing of 350mV and the receiver translates LVDS signals, with a typical differential input threshold of 100mV, into LVTTL levels. LVDS technology provides low EMI at ultra low power dissipation even at high frequencies. This device is ideal for high speed clock or data transfer.

Features

- Greater than 400Mbs data rate
- 3.3V power supply operation
- 0.5ns maximum differential pulse skew
- 2.5ns maximum propagation delay
- Low power dissipation
- Power OFF protection
- 100mV receiver input sensitivity
- Fail safe protection open-circuit, shorted and terminated conditions
- Meets or exceeds the TIA/EIA-644 LVDS standard
- Flow-through pinout simplifies PCB layout
- 14-Lead SOIC and TSSOP packages save space

Ordering Code:

Order Number	Package Number	Package Description
FIN1019M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
FIN1019MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

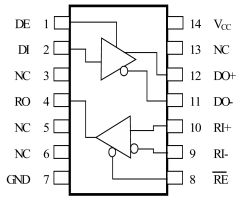
Function Table

Inputs			Outputs
RI+	**RI–**	**$\overline{RE}$**	**RO**
L	H	L	L
H	L	L	H
X	X	H	Z
Fail Safe Condition		L	H

DI	**DE**	**DO+**	**DO–**
L	H	L	H
H	H	H	L
X	L	Z	Z
Open–Circuit or Z	H	L	H

H = HIGH Logic Level L = LOW Logic Level X = Don't Care
Z = High Impedance Fail Safe = Open, Shorted, Terminated

Connection Diagram



Pin Descriptions

Pin Name	Description
DI	LVTTL Data Input
DO+	Non-inverting LVDS Output
DO–	Inverting LVDS Output
DE	Driver Enable (LVTTL, Active HIGH)
RI+	Non-Inverting LVDS Input
RI–	Inverting LVDS Input
RO	LVTTL Receiver Output
$\overline{RE}$	Receiver Enable (LVTTL, Active LOW)
V_{CC}	Power Supply
GND	Ground

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +4.6V
LVTTL DC Input Voltage (DI, DE, $\overline{RE}$)	−0.5V to +6V
LVDS DC Input Voltage (RI+, RI−)	−0.5V to 4.7V
LVTTL DC Output Voltage (RO)	−0.5V to +6V
LVDS DC Output Voltage (DO+, DO−)	−0.5V to 4.7V
LVDS Driver Short Circuit Current (I_{OSD})	Continuous
LVTTL DC Output Current (I_O)	16 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Max Junction Temperature (T_J)	150°C
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C
ESD (Human Body Model)	≥ 2000V
ESD (Machine Model)	≥ 200V

Recommended Operating Conditions

Supply Voltage (V_{CC})	3.0V to 3.6V
Input Voltage (V_{IN})	0 to V_{CC}
Magnitude of Differential Voltage ($\|V_{ID}\|$)	100 mV to V_{CC}
Common-Mode Input Voltage (V_{IC})	0.05V to 2.35V
Operating Temperature (T_A)	−40°C to +85°C

Note 1: The "Absolute Maximum Ratings": are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature and output/input loading variables. Fairchild does not recommend operation of circuits outside databook specification.

DC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ (Note 2)	Max	Units
LVDS Differential Driver Characteristics						
V_{OD}	Output Differential Voltage	R_L = 100Ω, See Figure 1	250	350	450	mV
ΔV_{OD}	V_{OD} Magnitude Change from Differential LOW-to-HIGH				25	mV
V_{OS}	Offset Voltage		1.125	1.25	1.375	V
ΔV_{OS}	Offset Magnitude Change from Differential LOW-to-HIGH				25	mV
I_{OZD}	Disabled Output Leakage Current	V_{OUT} = V_{CC} or GND, DE = 0V			±20	µA
I_{OFF}	Power Off Output Current	V_{CC} = 0V, V_{OUT} = 0V or 3.6V			±20	µA
I_{OS}	Short Circuit Output Current	V_{OUT} = 0V, DE = V_{CC}			−8	mA
		V_{OD} = 0V, DE = V_{CC}			±6	
LVTTL Driver Characteristics						
V_{OH}	Output HIGH Voltage	I_{OH} = −100 µA, $\overline{RE}$ = 0V, See Figure 6 and Table 1	V_{CC} −0.2			V
		I_{OH} = −8 mA, $\overline{RE}$ = 0V, V_{ID} = 400 mV V_{ID} = 400 mV, V_{IC} = 1.2V, see Figure 6	2.4			
V_{OL}	Output LOW Voltage	I_{OL} = 100 µA, $\overline{RE}$ = 0V, V_{ID} = −400 mV See Figure 6 and Table 1			0.2	V
		I_{OL} = −8 mA, $\overline{RE}$ = 0V, V_{ID} = −400 mV V_{ID} = −400 mV, V_{IC} = 1.2V, see Figure 6			0.5	
I_{OZ}	Disabled Output Leakage Current	V_{OUT} = V_{CC} or GND, $\overline{RE}$ = V_{CC}			±20	µA
LVDS Receiver Characteristics						
V_{TH}	Differential Input Threshold HIGH	See Figure 6 and Table 1			100	mV
V_{TL}	Differential Input Threshold LOW	See Figure 6 and Table 1	−100			mV
I_{IN}	Input Current	V_{IN} = 0V or V_{CC}			±20	µA
$I_{I(OFF)}$	Power-OFF Input Current	V_{CC} = 0V, V_{IN} = 0V or 3.6V			±20	µA
LVTTL Driver and Control Signals Characteristics						
V_{IH}	Input HIGH Voltage		2.0		V_{CC}	V
V_{IL}	Input LOW Voltage		GND		0.8	V
I_{IN}	Input Current	V_{IN} = 0V or V_{CC}			±20	µA
$I_{I(OFF)}$	Power-OFF Input Current	V_{CC} = 0V, V_{IN} = 0V or 3.6V			±20	µA
V_{IK}	Input Clamp Voltage	I_{IK} = −18 mA	−1.5			V

DC Electrical Characteristics (Continued)

Device Characteristics						
I_{CC}	Power Supply Current	Driver Enabled, Driver Load: R_L = 100 Ω Receiver Disabled, No Receiver Load			14	mA
		Driver Enabled, Driver Load: RL = 100 Ω, Receiver Enabled, (RI+ = 1V and RI− = 1.4V) or (RI+ = 1.4V and RO− = 1V)			20	mA
		Driver Disabled, Receiver Enabled, (RI+ = 1V and RI− = 1.4V) or (RI+ = 1.4V and RI− = 1V)			13.5	mA
		Driver Disabled, Receiver Disabled			9	mA
C_{IN}	Input Capacitance	Any LVTTL or LVDS Input		3		pF
C_{OUT}	Output Capacitance	Any LVTTL or LVDS Output		5		pF

Note 2: All typical values are at T_A = 25°C and with V_{CC} = 3.3V.

AC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ (Note 3)	Max	Units
Driver Timing Characteristics						
t_{PLHD}	Differential Propagation Delay LOW-to-HIGH	R_L = 100 Ω, C_L = 10 pF, See Figure 2 and Figure 3	0.5		1.5	ns
t_{PHLD}	Differential Propagation Delay HIGH-to-LOW		0.5		1.5	ns
t_{TLHD}	Differential Output Rise Time (20% to 80%)		0.4		1.0	ns
t_{THLD}	Differential Output Fall Time (80% to 20%)		0.4		1.0	ns
$t_{SK(P)}$	Pulse Skew $\|t_{PLH} - t_{PHL}\|$				0.5	ns
$t_{SK(PP)}$	Part-to-Part Skew (Note 4)	R_L = 100Ω, C_L = 10 pF, See Figure 4 and Figure 5			1.0	ns
t_{ZHD}	Differential Output Enable Time from Z to HIGH				5.0	ns
t_{ZLD}	Differential Output Enable Time from Z to LOW				5.0	ns
t_{HZD}	Differential Output Disable Time from HIGH to Z				5.0	ns
t_{LZD}	Differential Output Disable Time from LOW to Z				5.0	ns
Receiver Timing Characteristics						
t_{PLH}	Propagation Delay LOW-to-HIGH	$\|V_{ID}\|$ = 400 mV, C_L = 10 pF, See Figure 6 and Figure 7	1.0		2.5	ns
t_{PHL}	Propagation Delay HIGH-to-LOW		1.0		2.5	ns
t_{TLH}	Output Rise time (20% to 80%)			0.5		ns
t_{THL}	Output Fall time (80% to 20%)			0.5		ns
$t_{SK(P)}$	Pulse Skew | $t_{PLH} - t_{PHL}$ |				0.5	ns
$t_{SK(PP)}$	Part-to-Part Skew (Note 4)				1.0	ns
t_{ZH}	LVTTL Output Enable Time from Z to HIGH	R_L = 500 Ω, C_L = 10 pF, See Figure 8			5.0	ns
t_{ZL}	LVTTL Output Enable Time from Z to LOW				5.0	ns
t_{HZ}	LVTTL Output Disable Time from HIGH to Z				5.0	ns
t_{LZ}	LVTTL Output Disable Time from LOW to Z				5.0	ns

Note 3: All typical values are at T_A = 25°C and with V_{CC} = 5V.

Note 4: $t_{SK(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices switching in the same direction (either LOW-to-HIGH or HIGH-to-LOW) when both devices operate with the same supply voltage, same temperature, and have identical test circuits.

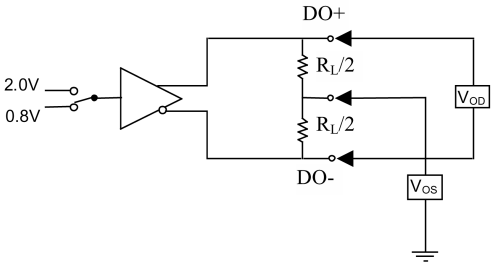
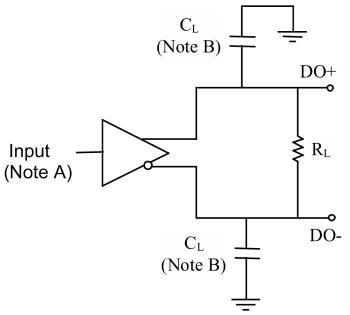


FIGURE 1. Differential Driver DC Test Circuit



Note A: Input pulses have frequency = 10 MHz, t_R or t_F = 1 ns

Note B: C_L includes all probe and jig capacitances

FIGURE 2. Differential Driver Propagation Delay and Transition Time Test Circuit

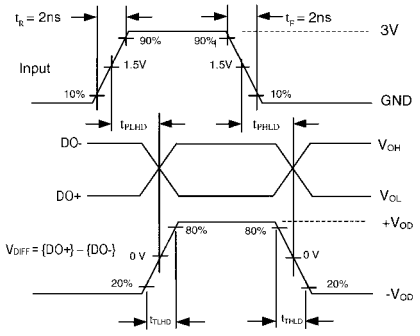
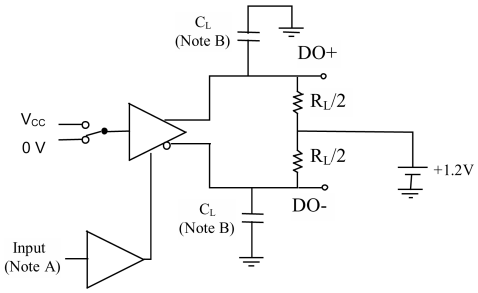


FIGURE 3. AC Waveforms for Differential Driver



Note B: Input pulses have the frequency = 10 MHz, t_R or t_F = 1 ns

Note A: C_L includes all probe and jig capacitances

FIGURE 4. Differential Driver Enable and Disable Test Circuit

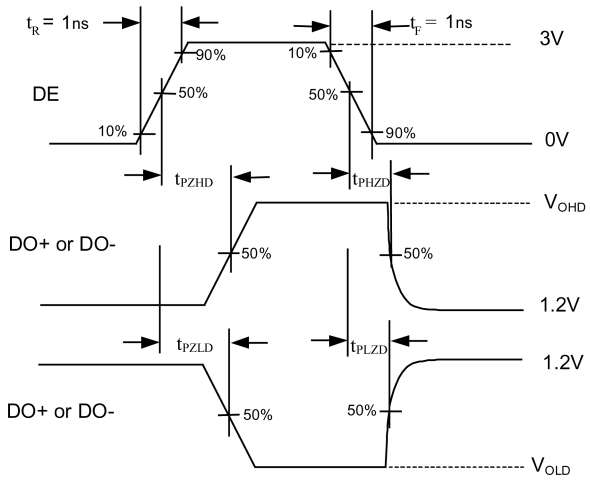
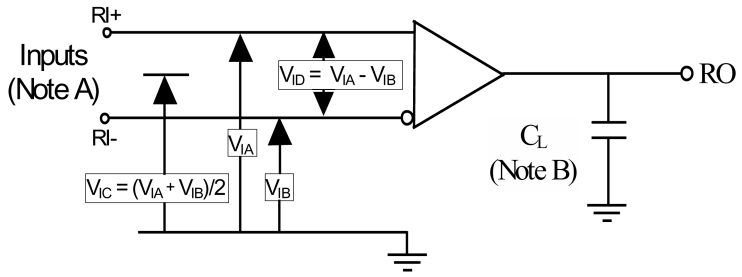


FIGURE 5. Enable and Disable AC Waveforms



Note A: Input pulses have frequency = 10 MHz, t_R or t_F = 1ns

Note B: C_L includes all probe and jig capacitance

FIGURE 6. Differential Receiver Voltage Definitions and Propagation Delay and Transition Time Test Circuit

TABLE 1. Receiver Minimum and Maximum Input Threshold Test Voltages

Applied Voltages (V)		Resulting Differential Input Voltage (mV)	Resulting Common Mode Input Voltage (V)
V_{IA}	V_{IB}	V_{ID}	V_{IC}
1.25	1.15	100	1.2
1.15	1.25	−100	1.2
2.4	2.3	100	2.35
2.3	2.4	−100	2.35
0.1	0	100	0.05
0	0.1	−100	0.05
1.5	0.9	600	1.2
0.9	1.5	−600	1.2
2.4	1.8	600	2.1
1.8	2.4	−600	2.1
0.6	0	600	0.3
0	0.6	−600	0.3

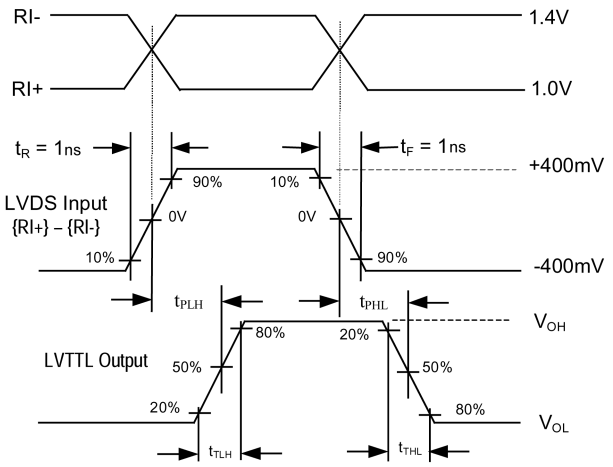
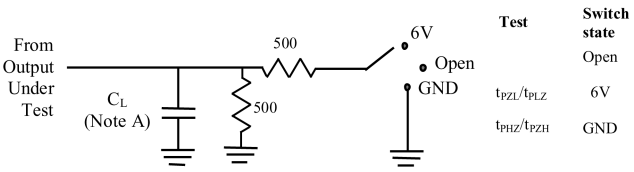


FIGURE 7. LVDS Input to LVTTL Output AC Waveforms

Test Circuit for LVTTL Outputs



Voltage Waveforms Enable and Disable Times

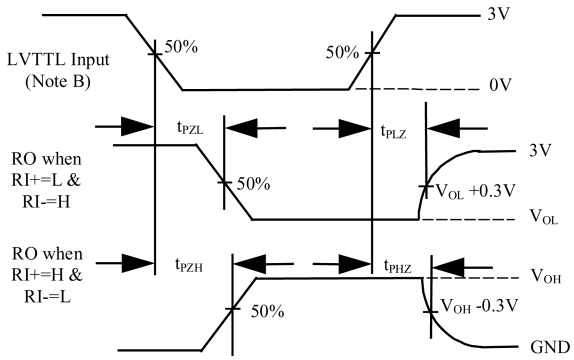
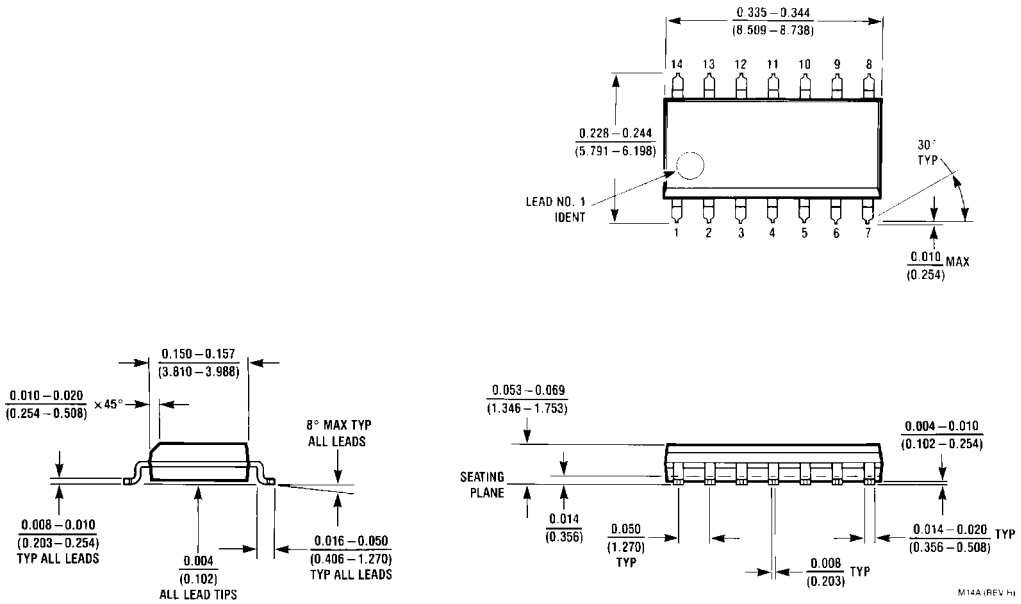


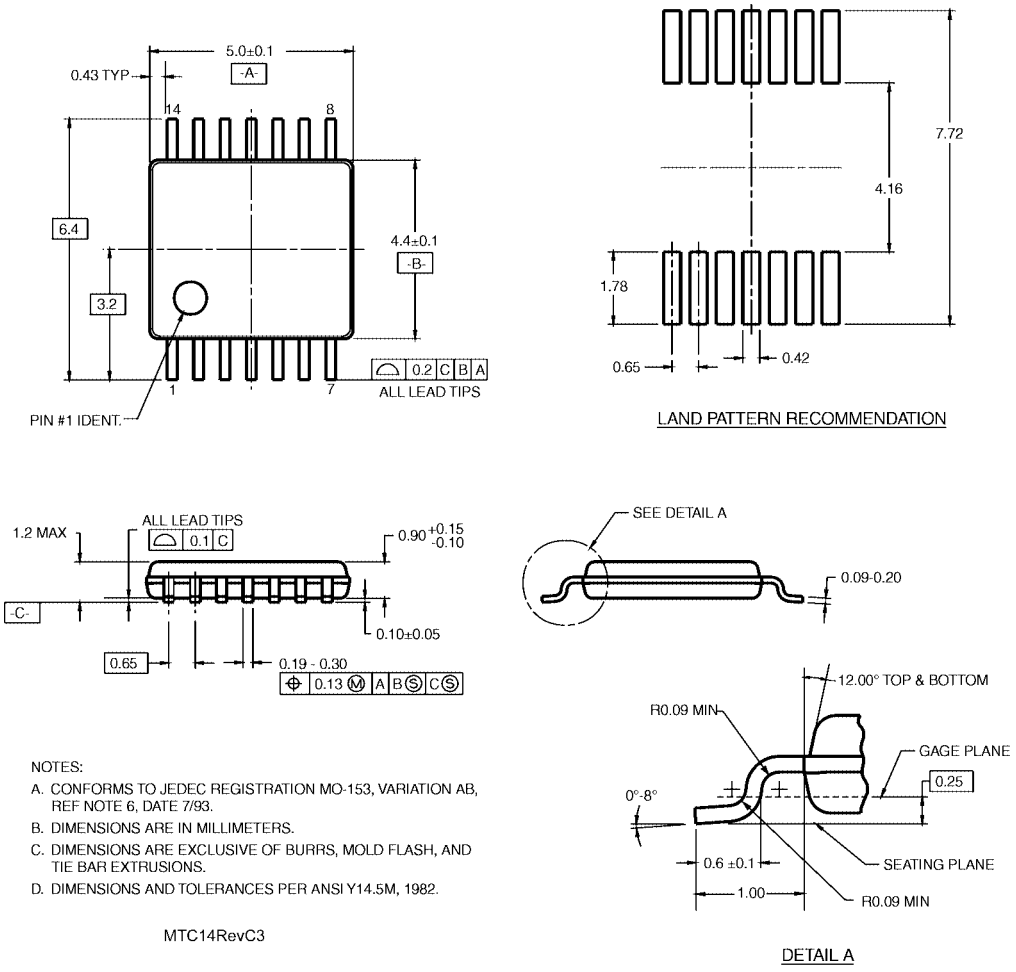
FIGURE 8. LVTTL Outputs Test Circuit and AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC14RevC3

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14

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