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P-Channel 100-V (D-S) MOSFET

PRODU	PRODUCT SUMMARY				
V _{DS} (V)	R_{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)		
- 100	0.120 at V _{GS} = - 10 V	- 19	16.5 nC		
- 100	0.160 at V _{GS} = - 4.5V	- 15.7	10.5 110		

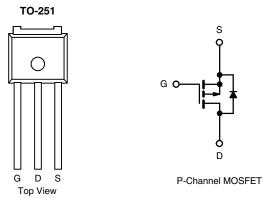
FEATURES

- Halogen-free Option Available
- TrenchFET[®] Power MOSFET
- UIS and R_g Tested



APPLICATIONS

• Active Clamp in Intermediate DC/DC Power Supplies



Parameter	Symbol	Limit	Unit		
Drain-Source Voltage		V _{DS}	- 100	V	
Gate-Source Voltage		V _{GS}	± 20	v	
	T _C = 25 °C		- 19.0		
Continuous Drain Current ($T_{I} = 150 \ ^{\circ}C$)	T _C = 70 °C		- 12.6		
Continuous Drain Current (1) = 150°C)	T _A = 25 °C	I _D	- 15 ^{a, b}		
	T _A = 70 °C		- 10 ^{a, b}		
Pulsed Drain Current		I _{DM}	- 20	— A	
Continuous Source Drain Diado Current	T _C = 25 °C	L.	- 13.2		
Continuous Source-Drain Diode Current	T _A = 25 °C	Is	- 3.0 ^{a, b}		
Avalanche Current		I _{AS}	15		
Single-Pulse Avalanche Energy	L = 0.1 mH	E _{AS}	11.25	mJ	
	T _C = 25 °C		52		
Mauinung Dauran Diasia atian	T _C = 70 °C	в	33	w	
Maximum Power Dissipation	T _A = 25 °C	P _D	3.7 ^{a, b}		
	T _A = 70 °C		2.4		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 50 to 150		
Soldering Recommendations (Peak Temperature)			260		

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. t = 10 s.

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THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, b}	t ≤ 10 s	R _{thJA}	26	33	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	1.9	2.4	C/W

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. Maximum under Steady State conditins is 81 °C/W.

Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static			•			•	
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	- 100			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$			- 100		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = - 250 μA		- 5.0			
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -250 \ \mu A$	- 1		- 3	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA	
Zana Cata Valtana Duain Cumant	1	V _{DS} = - 100 V, V _{GS} = 0 V			- 1		
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = -100 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 55 ^{\circ}\text{C}$			- 10	μΑ	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge -5 \text{ V}, \text{ V}_{GS} = -10 \text{ V}$	- 10			Α	
	Passa	V _{GS} = - 10 V, I _D = - 4 A	0.108		0.120	0	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 4.5 V, I _D = - 3 A		0.119	0.160	Ω	
Forward Transconductance ^a	9 _{fs}	V _{DS} = - 15 V, I _D = 4 A		25		S	
Dynamic ^b	•		•	•	•	•	
Input Capacitance	C _{iss}			1480			
Output Capacitance	C _{oss}	V _{DS} = - 50 V, V _{GS} = 0 V, f = 1 MHz		80		pF	
Reverse Transfer Capacitance	C _{rss}			60			
Tatal Cata Charge		$V_{DS} = -50 \text{ V}, V_{GS} = -10 \text{ V}, I_{D} = -4 \text{ A}$		35	55		
Total Gate Charge	Q_g		16.5	25	nC		
Gate-Source Charge	Q _{gs}	Q_{gs} $V_{DS} = -50$ V, $V_{GS} = -4.5$ V, $I_D = -4$ A		4.7			
Gate-Drain Charge	Q _{gd}			8			
Gate Resistance	R _g	f = 1 MHz		5.3	8	Ω	
Turn-On Delay Time	t _{d(on)}			30	45		
Rise Time	t _r	V_{DD} = - 50 V, R_L = 12.5 Ω		110	165	-	
Turn-Off DelayTime	t _{d(off)}	${ m I}_{ m D}\cong$ - 4 A, ${ m V}_{ m GEN}$ = - 4.5 V, ${ m R}_{ m g}$ = 1 Ω		51	80		
Fall Time	t _f			40	60		
Turn-On Delay Time	t _{d(on)}			11	18	ns	
Rise Time	t _r	V_{DD} = - 50 V, R_L = 12.5 Ω		13	20		
Turn-Off DelayTime	t _{d(off)}	$I_D \cong$ - 4 A, V_{GEN} = - 10 V, R_g = 1 Ω		42	65		
Fall Time	t _f			10	15		
Drain-Source Body Diode Characterist	ics						
Continuous Source-Drain Diode Current	۱ _S	T _C = 25 °C			- 19	^	
Pulse Diode Forward Current ^a	I _{SM}				- 20	A	
Body Diode Voltage V_{SD} $I_S = -3 \text{ A}$		I _S = - 3 A		- 0.8	- 1.2	V	
Body Diode Reverse Recovery Time	t _{rr}			46	70	ns	
Body Diode Reverse Recovery Charge	Q _{rr}	I _F = - 4 A, dl/dt = 100 A/μs, T _{.1} = 25 °C		97	150	nC	
Reverse Recovery Fall Time	t _a	$r_{\rm F} = -4$ A, u/ul = 100 A/µs, $r_{\rm J} = 25$ °C		36			
Reverse Recovery Rise Time	t _b			10		ns	

Notes:

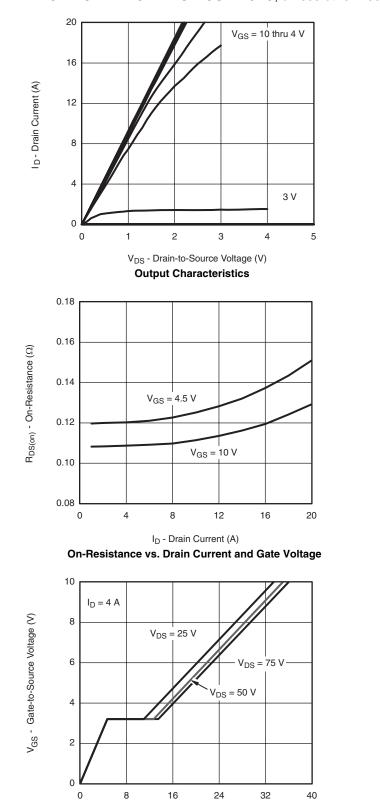
a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



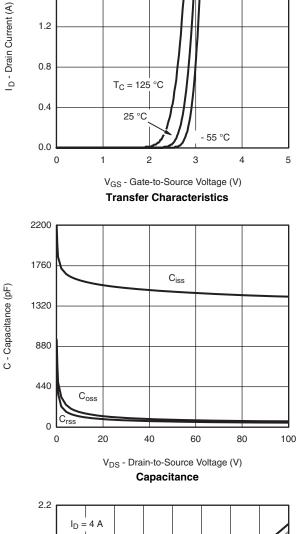
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Qg - Total Gate Charge (nC)

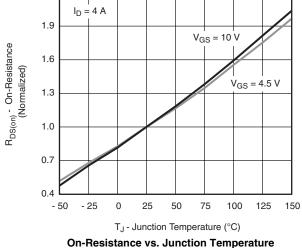
Gate Charge

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



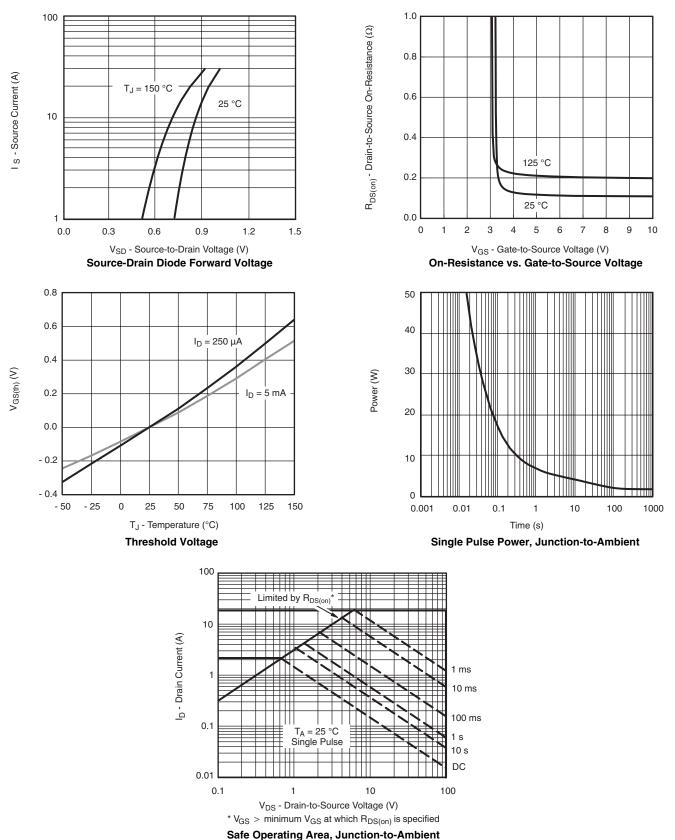
2.0

1.6



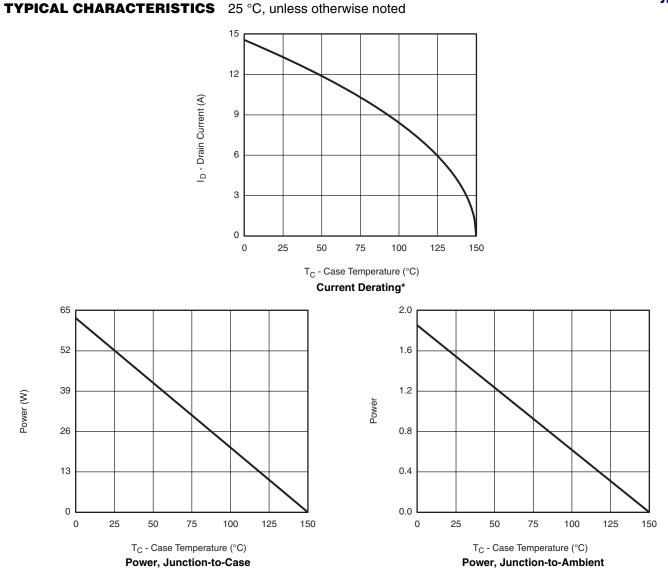
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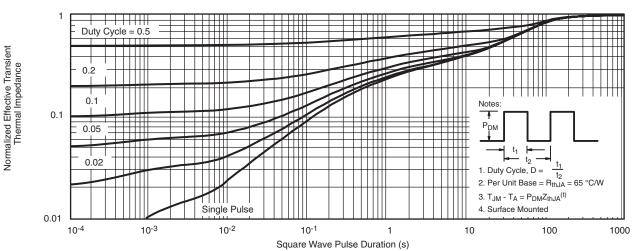
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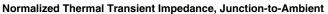


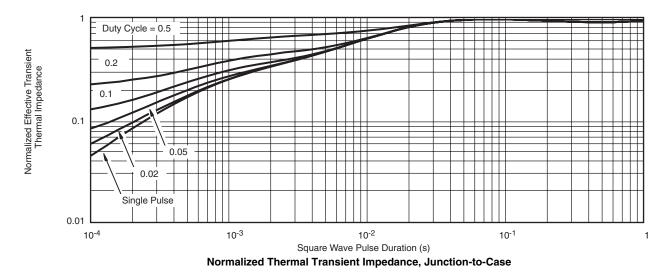
* The power dissipation PD is based on T_{J(max)} = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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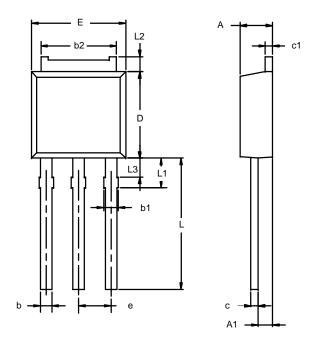






Package Information Áwww.din-tek.jp

TO-251AA (DPAK)



Note: Dimension L3 is for reference only.

	MILLIN	IETERS	INCHES		
Dim	Min	Max	Min	Max	
Α	2.21	2.38	0.087	0.094	
A1	0.89	1.14	0.035	0.045	
b	0.71	0.89	0.028	0.035	
b1	0.76	1.14	0.030	0.045	
b2	5.23	5.43	0.206	0.214	
С	0.46	0.58	0.018	0.023	
c1	0.46	0.58	0.018	0.023	
D	5.97	6.22	0.235	0.245	
Е	6.48	6.73	0.255	0.265	
е	2.28 BSC		0.090 BSC		
L	8.89	9.53	0.350	0.375	
L1	1.91	2.28	0.075	0.090	
L2	0.89	1.27	0.035	0.050	
L3	1.15	1.52	0.045	0.060	
	3946—Rev. E		0.045	0.	



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