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Motorola Reliability Report for the LCX Product Family

Introduction/Statement of Purpose

Motorola Reliability and Quality Assurance

Motorola has a long standing reputation for manufacturing products of excellent Quality and Reliability since the introduction of the first car radio in 1928. This has helped Motorola to become one of the largest corporations exclusively devoted to electronics.

In today's semiconductor marketplace, two important elements for the success of a company are its quality and reliability systems. They are interrelated, reliability being quality extended over the expected life of a product. For any manufacturer to remain in business, its products must meet or exceed basic quality and reliability standards and customer needs.

At Motorola, the most stringent and demanding definitions of quality and reliability are used.

Quality

- Reduction of variability around a target so that conformance to customer requirements and expectations can be achieved in a cost–effective way
- The probability that a device (equipment, parts) will have performance characteristics within specified limits
- Fitness for use

Reliability

- Quality in time and environment
- The probability that our semiconductor devices, which initially have satisfactory performance, will continue to perform their intended function for a given time in usage environments

At Motorola, our Reliability and Quality Assurance Program is designed to generate ongoing data for both reliability and quality for the various product families. Both reliability and quality monitors are performed on the different major categories of semiconductor products. These monitors are designed to test the product's design and material as well as to identify and eliminate potential failure mechanisms to ensure reliable device performance in a "real world" application. Thus, the primary purpose of the program is to identify trends from generated data, so if need be, corrective action(s) can be taken toward improving performance. In addition, this reliability and quality data can be utilized by our customers for failure rate predictions.

It is the explicit purpose of this communication to inform the customer of our LCX qualification results. In addition, we have provided a general definition of our reliability and quality assurance program.

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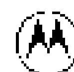

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LCX Device Description

The LCX logic family, the first low voltage CMOS family with 5V tolerant inputs and outputs, is manufactured on the H4C “plus” 75% CMOS (double layer metal) process at MOS 6. The LCX family emphasizes low power, low switching noise, and fast switching speeds. It will be assembled in the qualified 20 ld. SOIC package and 20 ld. TSSOP package. The H4C “plus” 75% CMOS process in MOS 6 was qualified using the LCX logic family’s E76S maskset.

LCX Processing Information

PROCESSING SUMMARY — H4C “plus,” 75% CMOS (Double Layer Metal)

General	
Process Type	CMOS on EPI
Effective Channel Length	Min. target=0.65µm
Process Complexity	Single Poly, Double Metal
Gate Processing	
Gate Oxide Thickness	150Å
Gate Terminal	Phosphorous Doped Polysilicon (POCL)
N+ Source Drain Dopant	Phosphorous & Arsenic
P+ Source Drain Dopant	Boron (BF2)
Metallization Processing	
Metal Composition	AlSiCu w/TiN Barrier (M1) AlSiCu (M2)
Passivation Processing	
Passivation Type	Double Layer, Nitride over PSG Oxide
Electrical Characteristics	
Field Threshold Voltage	>12V
Punchthrough Voltage	>12V
Gate Oxide Breakdown	>14V

LCX Qualification Introduction

LCX Qualification consisted of intrinsic and extrinsic reliability testing. Intrinsic reliability concerns device degradation issues and is assessed via electromigration, hot carrier injection and dielectric breakdown measures. Extrinsic reliability addresses both processing and packaging related issues and utilizes several tests: high temperature bias, temperature cycling, pressure temperature humidity, thermal shock, temperature humidity bias, surface mount preconditioning, physical dimensions, solderability and marking permanency. (Included below are definitions of the aforementioned terms.)

INTRINSIC RELIABILITY

Electromigration

Electromigration is the movement of metal in the direction of electron flow. This is accelerated by high current densities and temperatures which result in metal void and/or collection (hillock) formations, and ultimately shorts. Design rules specify minimum metal widths and maximum current densities to circumvent electromigration issues.

Hot Carrier Injection (HCI)

Hot carrier injection is the result of electron scattering and subsequent trapping in the gate oxide of MOS devices. Scattering is a function of electron velocity and thus electric fields and temperature. Ultimately, carrier mobility and transconductance are reduced causing threshold voltage shifts. Processing conditions are set to minimize hot carrier generation rates and gate trapping efficiencies.

Dielectric Breakdown

Dielectric breakdown results in the formation of a conductive path connecting once–isolated conducting layers. High voltage induced charge injection and trapping accelerates this breakdown. Dielectric integrity is maximized via uniform depositional thickness, and dielectric quality is achieved through minimizing impurity, charge, and defect levels.

EXTRINSIC RELIABILITY

High Temperature Bias (HTB)

High temperature bias (HTB) testing is performed to accelerate failure mechanisms which are activated through the application of elevated temperatures and the use of biased operating conditions. The temperature and voltage conditions used in the stress are dependent on the product under stress. However, the typical ambient temperature is 145°C with the static bias applied equal to or greater than the data sheet nominal value.

Temperature Cycling (MIL–STD–833D–1010C)

Temperature cycle testing accelerates the effects of thermal expansion mismatch among the different components within a specific die and packaging system. This test is typically performed per MIL–STD–883D Method 1010C with the minimum and maximum temperatures being –65°C and +150°C, respectively. During temperature cycle testing, devices are inserted into a cycling system and held at the cold dwell temperature for at least ten minutes. Following this cold dwell, the devices are heated to the hot dwell where they remain for another ten minute minimum time period. The system employs a circulating air environment to assure rapid stabilization at the specified temperature. The dwell at each extreme, plus the two transition times of five minutes each (one up to the hot dwell temperature, another down to the cold dwell temperature), constitute one cycle.

Thermal Shock (MIL–STD–833D–1010C)

The objective of thermal shock testing is the same as that for temperature cycle testing, that is, to emphasize differences in expansion coefficients for components of the packaging system. However, thermal shock provides additional stress, in that the device is exposed to a sudden change in temperature due to a maximum transfer time of ten seconds, as well as the increased thermal conductivity of a liquid ambient. This test is typically performed per MIL–STD–883D Method 1011C with minimum and maximum temperatures being –65 °C to +150 °C, respectively. Devices are placed in a bath and cooled to minimum specified temperature. After being held in the cold chamber for five minutes minimum, the devices are transferred to an adjacent chamber at the maximum specified temperature for an equivalent time. Two five minute dwells plus two ten second transitions constitute one cycle.

Temperature Humidity Bias (THB Motorola Std)

This stress is performed to accelerate the effects of moisture penetration, with the dominant effect being corrosion. Conditions employed during this test are a temperature of 85°C, humidity of 85% RH, and a nominal bias level.

Pressure Temperature Humidity (PTH Motorola Std)

This stress is performed to accelerate the effects of moisture penetration, with the dominant effect being corrosion. This test detects similar failure mechanisms as THB but at a greatly accelerated rate. Conditions employed during this test are a temperature of 121°C, pressure of 15psig or greater, humidity of 100% RH, unbiased.

Surface Mount Preconditioning (Motorola Std)

Preconditioning tests are performed to simulate the customer board mount process where surface mount parts are subjected to a high temperature for a short duration. These tests detect mold compound delamination from the die and leadframe which can result in reliability failures. The dominant failure mechanism is corrosion, but other

stress–related problems could also occur like fractured wirebonds, passivation cracks, smeared metal on die, etc.

The conditions typically used are 245°C for IR reflow and 260°C for solder immersion. For small pitch packages, a 260°C oil immersion is substituted for the 260°C solder to avoid solder bridging of the leads.

Physical Dimensions (MIL–STD–883D–2016)

The purpose of this test is to verify the external dimensions of the device are in accordance with the case outline specification. This test is typically performed per MIL–STD–883D Method 2016.

Solderability (MIL–STD–883D–2003)

The purpose of this test is to determine the solderability of all terminations which are normally joined by a soldering operation. This test is typically performed per MIL–STD–883D Method 2003. The test verifies the ability of these terminations to be wetted or coated by solder, and to predict suitable fillet when dip soldered. An accelerated aging test is included in this method which simulates a minimum of six months natural aging under a combination of various storage conditions that have a deleterious effect on the solderability.

Marking Permanency (Motorola Std)

The purpose of this test is to verify the device markings will not become illegible when subjected to solvents, and the solvents will not cause any mechanical, electrical, damage or deterioration, of the materials or finishes. This test is typically performed per Motorola standard.

Process Qualification Information

PROCESS QUALIFICATION SUMMARY

The H4C "plus" 75% CMOS (double layer metal) process qualification consisted of intrinsic reliability testing (Electromigration, Hot Carrier Injection, and Dielectric Breakdown) and extrinsic reliability testing (High Temperature Bias, Temperature Cycling, and Pressure Temperature Humidity), the results of which follow.

Intrinsic Reliability

- Electromigration . . . . No significant degradation
- HCI . . . . No significant degradation
- Dielectric Breakdown . . . . No significant degradation

Extrinsic Reliability

- HTB . . . . Zero failures
- Temperature Cycling . . . . Zero failures
- PTH . . . . Zero failures

INTRINSIC RELIABILITY RESULTS

DEVICE QUALIFICATION

Electromigration

Electromigration evaluation of MOS 6 metals used in the H4C "plus" 75% CMOS (double layer metal) process revealed an acceptable metallization process for a minimum lifetime of 10 years at 100°C with $\leq$ .01% cumulative failures.

Hot Carrier Injection

Hot carrier injection testing resulted in less than a 10% change in transconductance over the lifetime of the transistor.

Worst case HCI occurs at cold temperature, so Low Temperature Bias was performed at –10°C as shown below. Zero process related rejects occurred after 504 hours of op–life at –10°C.

LOW TEMPERATURE BIAS (–10°C, 3.6V BIAS)

Lot #	Sample Size	40 Hours	250 Hours	504 Hours
S37201.4	72	0 Rejects	0 Rejects	0 Rejects

Dielectric Breakdown

The current conduction and QBD data taken in MOS 6 was used to calculate an intrinsic gate oxide lifetime of 1364 years. This estimated lifetime greatly exceeds the expected lifetime of the device.

EXTRINSIC RELIABILITY RESULTS/DATA

PROCESS QUALIFICATION

The reliability testing consisted of High Temperature Bias (145°C, 3.6V bias), Temperature Cycling (–65°C to 150°C), and PTH (121°C, 15PSIG, & 100% RH). Samples from three wafer lots; S37201.4, S41657.2, and S37744.1 were tested as specified above. Wafer lot # S37201.4 was a nominal lot.

Wafer lot # S41657.2 was a metal and dielectric split lot. The metal and dielectric layers were run at the maximum and minimum thickness specifications in order to account for worst and best case step coverage.

Wafer lot # S37744.1 was a Vt and Leff split lot. The Vt and Leff were run at minimum and maximum specifications in order to account for worst and best case leakage, worst and best case speeds, and worst case translation window. Zero process related rejects occurred after 504 hours of op–life, 600 temp cycles, and 240 hours of PTH.

HIGH TEMPERATURE BIAS (145°C, 3.6V BIAS)

Lot #	Sample Size	40 Hours	250 Hours	504 Hours
S37201.4	84	0 Rejects	0 Rejects	0 Rejects
S41657.2	304	0 Rejects	0 Rejects	0 Rejects
S37744.1	225	0 Rejects	0 Rejects	0 Rejects

FIT = 14.5; Stress temp = 145°C; Equiv temp = 55°C; Activation energy = 0.7eV; Confidence level = 60%; Device hours = 308,952.

TEMPERATURE CYCLE (–65°C TO 150°C)

Lot #	Sample Size	100 Cycles	600 Cycles
S37201.4	76	0 Rejects	0 Rejects
S41657.2	286	0 Rejects	0 Rejects
S37744.1	227	0 Rejects	0 Rejects

PRESSURE TEMPERATURE HUMIDITY (121°C, 15 PSIG, 100% RH)

Lot #	Sample Size	96 Hours	240 Hours
S37201.4	43	0 Rejects	0 Rejects
S41657.2	168	0 Rejects	0 Rejects
S37744.1	223	0 Rejects	0 Rejects

The H4C "plus" 75% CMOS (double layer metal) process in MOS 6 has been qualified and approved based on the results of the above intrinsic and extrinsic reliability results.

Package Qualification

MC74LCX244 is being offered in both 16ld SOIC and 20ld TSSOP packaging. Both are currently qualified packages. As the TSSOP package is a newer technology, relevant qualification data has been included in this report. All reliability tests have passed successfully, including preconditioning tests used to simulate customer board mount processes (see below). Furthermore, based on reliability results, drypack is not required for this package type.

Included below is general information concerning the TSSOP package and results relating to the AIZU TSSOP qualification.

Package Qualification Summary

TSSOP leads	Op Life	Temperature Cycle	Thermal Shock	THB	Surface Mount Preconditioning	Solderability	Marking Permanency	Physical Dimension
14	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
16	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
20	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS

Summary Package Information

- Package Material — Hitachi CEL 9200N
- Leadframe Material — Copper
- Plating — 80/20 tin/lead solder plate
- Die Attach Epoxy — Sumitomo CRM 1033B
- Wire Bond Material — 1.0 mil gold
- Wire Bond Method — Thermosonic Ball
- Theta JA (20 ld TSSOP) — 140 Deg C/W
- 14–/16–Lead Flag Size — 83 x 93 mils
- 20–Lead Flag Size — 83 x 120 and 110 x 120 mils

The Aizu package dimensions are as follows:

Package	Width	Length	Pitch	Total Mounting Height
14/16-Lead	4.4mm	5.0mm	6.5mm	1.1mm
20-Lead	4.4mm	6.5mm	6.5mm	1.1mm

Qualification data is based on devices from the Metal Gate, High Speed, and Fact families with various die sizes as listed below:

Lot #	Lead Count	Device	Die Size
1	14	MC14066B	64 x 64 mils
2	14	MC74ACT08	41 x 45
3	16	MC74HC76	72 x 83
4	16	MC74HC175	68 x 73
5	16	MC74ACT163	63 x 50
6	20	MC74HC244A	74 x 74
7	20	MC74AC245	69 x 81
8	20	MC74ACT534	68 x 67
9	20	MC74HCT245A	82 x 104

Package Qualification Results

HTB T_A = 125°C, Nominal Bias

Lot #	Leads	168 Hours	504 Hours	1000 Hours
1	14 ld	0/45	0/45	0/45
6	20 ld	0/45	0/45	0/45
7	20 ld	0/45	0/45	0/45

TEMPERATURE CYCLE (MIL–STD–883, Method 1010C)
–65 to +150°C

Lot #	Leads	600 Hours	1000 Hours
1	14 ld	0/45	0/45
2	14 ld	0/76	0/76
3	16 ld	0/45	0/45
4	16 ld	0/45	0/45
5	16 ld	0/74	0/74
6	20 ld	0/45	0/45
7	20 ld	0/45	0/45
8	20 ld	0/73	0/73
9	20 ld	0/45	0/45

THERMAL SHOCK (MIL–STD–883, Method 1011C)
–65 to +150°C

Lot #	Leads	300 Cycles	500 Cycles	1000 Cycles
1	14 ld	0/22	0/22	0/22
3	16 ld	0/22	0/22	0/22
4	16 ld	0/22	0/22	0/22
6	20 ld	0/22	0/22	0/22
7	20 ld	0/22	0/22	0/22

THB — 85°C/85% R.H., Nominal Bias

Lot #	Leads	168 Hours	504 Hours	1000 Hours
1	14 ld	0/45	0/45	0/45
3	16 ld	0/45	0/45	0/45
4	16 ld	0/45	0/45	0/45
6	20 ld	0/45	0/45	0/45
7	20 ld	0/45	0/45	0/45

Preconditioning tests:

IR Reflow preconditioning is performed to simulate the customer board mount process where surface mount parts are subjected to IR temperatures of 245°C max.

All preconditioned lots received 30x external visual for package cracks. No cracks were present for any of the preconditioned lots.

IR reflow preconditioning — 24 hrs 85/85 + 2 cycles IR reflow at 240°C + PTH (121°C, 100%RH, 15psig)

Lot #	Leads	96 Hours	192 Hours	288 Hours
1	14 ld	0/45	0/45	0/45
3	16 ld	0/45	0/45	0/45
4	16 ld	0/45	0/45	0/45
6	20 ld	0/45	0/45	0/45
7	20 ld	0/45	0/45	0/45
9	20 ld	0/45	0/45	0/45

IR reflow preconditioning — 168 hrs 85/85 + 3 cycles IR reflow at 245°C + PTH (121°C, 100%RH, 15psig)

Lot #	Leads	96 Hours
2	14 ld	0/41
5	16 ld	0/40
8	20 ld	0/41
9	20 ld	0/45

IR reflow preconditioning — 168 hrs 85/85 + 3 cycles IR reflow at 245°C + Temp cycle (–65 to +150°C)

Lot #	Leads	100 Cycles	600 Cycles	1000 Cycles
2	14 ld	0/71	0/71	0/71
5	16 ld	0/73	0/73	0/73
8	20 ld	0/72	0/72	0/72
9	20 ld	0/76	0/76	0/76

Solder immersion preconditioning:

Solder immersion is performed to simulate the customer backside board assembly process where surface mount parts are subjected to a 260°C wave solder. Based on the following data, the 14/16/20 TSSOP can be backside board mounted.

Solder Preconditioning — 168 hrs 85/85 + 10 second oil/solder immersion at 260°C + PTH (121°C, 100%RH, 15psig)

Lot #	Leads	48 Hours	96 Hours
2	14 ld	0/20	0/20
5	16 ld	0/21	0/21
8	20 ld	0/25	0/25
9	20 ld	0/45	0/45

Solder Preconditioning — 168 hrs 85/85 + 10 second oil/solder immersion at 260°C + Temp cycle (–65 to +150°C)

Lot #	Leads	100 Cycles	600 Cycles	1000 Cycles
2	14 ld	0/16	0/16	0/16
5	16 ld	0/21	0/21	0/21
8	20 ld	0/22	0/22	0/22
9	20 ld	0/76	0/76	—

Solderability (Motorola Standard)

Lot #	Leads	8 Hour Steam Age Results	2 Hour Bake at 175°C Results
2	14 ld	0/3	0/3
5	16 ld	0/3	0/3
8	20 ld	0/3	0/3

Marking Legibility (Motorola Standard)

Lot #	Leads	Results
2	14 ld	0/11
5	16 ld	0/11
8	20 ld	0/11

Physical Dimensions (Case Outline)

Lot #	Leads	Results
2	14 ld	0/3
5	16 ld	0/3
8	20 ld	0/3

Terminal Strength (Motorola Standard)

A. Tensile Pull–Out Strength — 100g, 10 sec.

Lot #	Leads	Results
4	16 ld	0/11

B. Bending Test — 50g, 2 Times

Lot #	Leads	Results
4	16 ld	0/11

Salt Water Spray — T_A = 35°C, 5% NaCl solution, 24 Hours

Lot #	Leads	Results
3	16 ld	0/11
6	20 ld	0/11
7	20 ld	0/11

X–Ray for Wire Sweep and Internal Voids (Motorola Standard)

Lot #	Leads	Results
2	14 ld	0/5
3	16 ld	0/5
4	16 ld	0/5
5	16 ld	0/5
8	20 ld	0/5

Thermal Considerations

Reliability of Plastic Packages

Although today's plastic packages are as reliable as ceramic packages under most environmental conditions, as the junction temperature increases a failure mode unique to plastic packages becomes a significant factor in the long term reliability of the device.

Modern plastic package assembly utilizes gold wire bonded to aluminum bonding pads throughout the electronics industry. As the temperature of the silicon (junction temperature) increases, an intermetallic compound forms between the gold and aluminum interface. This intermetallic formation results in a significant increase in the impedance of the wire bond and can lead to performance failure of the affected pin. With this relationship between intermetallic formation and junction temperature established, it is incumbent on the designer to ensure that the junction temperature for which a device will operate is consistent with the long term reliability goals of the system.

Reliability studies were performed at elevated ambient temperatures (125°C) from which an Arrhenius Equation (Eq 1), relating junction temperature to bond failure, was established. The application of this equation yields the values in Table 1. This table relates the junction temperature of a device in a plastic package to the continuous operating time before 0.1% bond failure (1 failure per 1000 bonds).

$$T = 6.376 \times 10^{-9} e^{\left[\frac{11554.267}{273.15 + T_J}\right]} \qquad \text{(Eq 1)}$$

Where:
T = Time to 0.1% bond failure

Table 1. Tj vs Time to 0.1% Bond Failure

Junction Temp. (°C)	Time (hours)	Time (yrs.)
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.1
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

Thermal Management

As in any system, proper thermal management is essential to establish the appropriate trade-off between performance, density, reliability and cost. In particular, the designer should be aware of the reliability implication of continuously operating semiconductor devices at high junction temperatures.

The increasing popularity of surface mount devices (SMD) is putting a greater emphasis on the need for better thermal management of a system. This is due to the fact that SMD packages generally require less board space than their through hole counterparts so that designs incorporating SMD technologies have a higher thermal density. To optimize the thermal management of a system it is imperative that the user understand all of the variables which contribute to the junction temperature of the device.

The variables involved in determining the junction temperature of a device are both supplier and user defined. The supplier, through lead frame design, mold compounds, die size and die attach, can positively impact the thermal resistance and the junction temperature of a device. Motorola continually experiments with new package designs and assembly techniques in an attempt to further enhance the thermal performance of its products.

It can be argued that the user has the greatest control of the variables which commonly impact the thermal performance of a device. Depending on the environment in which an IC is placed, the user could control over 75% of the current that flows through the device. Ambient temperature, air flow and related cooling techniques are the obvious user controlled variables, however, PCB substrate material, layout density, size of the air-gap between the board and the package, amount of exposed copper interconnect, use of thermally-conductive epoxies and number of boards in a box and output loading can all have significant impacts on the thermal performance of a system.

PCB substrates all have different thermal characteristics, these characteristics should be considered when exploring the PCB alternatives. The user should also account for the different power dissipations of the different devices in his system and space them on the PCB accordingly. In this way, the heat load is spread across a larger area and “hot spots” do not appear in the layout. Copper interconnect traces act as heat radiators, therefore, significant thermal dissipation can be achieved through the addition of interconnect traces on the top layer of the board. Finally, the use of thermally conductive epoxies can accelerate the transfer of heat from the device to the PCB where it can more easily be passed to the ambient.

The advent of SMD packaging and the industry push towards smaller, denser designs makes it incumbent on the designer to provide for the removal of thermal energy from the system. Users should be aware that they control many of the variables which impact the junction temperatures and, thus, to some extent, the long term reliability of their designs.

Calculating Junction Temperature

The following equation can be used to estimate the junction temperature of a device in a given environment:

$$T_J = T_A + P_D \Theta_{JA}$$

where:

T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
Θ_{JA} = Avg Pkg Thermal Resistance (Junction Ambient)

$$P_D = V_{CC}\left[\overset{\mathbf{1}}{C_P V_{CC} \sum_{i=1}^{s} F_{OUT_i}}\right] + V_{CC}\,[\overset{\mathbf{2}}{\Delta I_{CC} n}]$$

$$+ (V_{CC} - V_{OH})\left[\overset{\mathbf{3}}{(V_{OH} - V_{OL}) \sum_{i=1}^{s} C_{L_i} F_{OUT_i}} + \overset{\mathbf{4}}{\sum_{i=1}^{h} \frac{V_{OH}}{R_{D_i}}}\right]$$

$$+ (V_{OL})\left[\overset{\mathbf{5}}{(V_{OH} - V_{OL}) \sum_{i=1}^{s} C_{L_i} F_{OUT_i}} + \overset{\mathbf{6}}{\sum_{i=1}^{l} \frac{(V_{CC} - V_{OL})}{R_{U_i}}}\right]$$

Power Dissipation Equation

The power dissipation equation is made up of five major factors controlled by the user which contribute to increased power dissipation:

1. Frequency of operation (output switching frequency)
2. Input voltage levels
3. Output loading (capacitive and resistive)
4. V_{CC} level
5. Duty cycle

Each of these five factors are addressed in the estimating equation except duty cycle. Duty cycle can be addressed by “weighting” the power dissipation equation terms appropriately.

The first current term is I_{CCD}, with the device unloaded. It is caused by the internal switching of the device. Static I_{CC} is so small for LCX, that when estimating power dissipation, it is ignored.

$$C_P V_{CC} \sum_{i=1}^{s} F_{out_i}$$

This term represents the I_{CC} current with absolutely no load. This measurement is taken without the output pins connected to the board. The C_P for a device is calculated by:

$$C_P = \frac{I_{CC}(@50MHz) - I_{CC}(@1MHz)}{V_{CC}(49MHz)s}$$

“s” is the number of outputs switching. C_P may vary slightly from part to part within a product family.

The next term is from current due to holding the CMOS inputs at V_{CC}–0.6V rather than at the rail voltages. This term becomes insignificant as load and frequency increase.

$$\Delta I_{CC} n$$

ΔI_{CC} is the through current when holding the input High of a device to V_{CC}–0.6V. This value is typically 300µA or less. “n” is the number of inputs held at this level.

The third term is current through the upper structure of the device. It is caused by the external capacitive load and the output frequency. If a capacitive load exists then this term can become very significant.

$$(V_{OH} - V_{OL}) \sum_{i=1}^{s} C_{L_i} F_{OUT_i}$$

V_{OH}–V_{OL} is the voltage swing of the output. C_L is the output load (this could vary from output to output). F_{OUT} is the output frequency which can also vary from output to output.

The fourth term stems from current through the upper structure due to an external resistive load to ground.

As the output frequency increases, the measured current approaches that of static High outputs.

$$\sum_{i=1}^{h} \frac{V_{OH}}{R_{D_i}}$$

R_D is an external pull–down resistor. A different value load could be applied to each output.

The fifth current term is determined by the output capacitive load and the output frequency on the lower structure of the device. If this load exists than this term is also significant.

$$(V_{OH} - V_{OL}) \sum_{i=1}^{s} C_{L_i} F_{OUT_i}$$

All variables are the same as with the third term with the exception that this is current flowing through the lower structure of the IC. This current is not I_{CC}, but rather current that is “sinked” from an external source.

The final term is due to an external load connected to V_{CC}. This term includes both switching and static Low outputs.

$$\sum_{i=1}^{l} \frac{(V_{CC} - V_{OL})}{R_{U_i}}$$

As with term five, this is current that flows through the lower structure of the IC. This current too is not I_{CC}.

Example of Thermal Calculations

Junction temperature can be estimated using the following equation:

$$T_J = (\Theta_{JA} \times P_D) + T_A$$

where:

T_J = Junction Temperature (°C)
Θ_{JA} = Thermal Resistance (Junction–to–Ambient)
P_D = Power Dissipation at a T_J
T_A = Ambient Temperature (°C)

Example of LCX T_J Calculation

1. Calculate Current Consumption:

For example, the LCX244's C_P is 25pF. Let V_{CC} = 3V; operating temperature = 85°C; F_{OUT} = 50MHz; for 4 outputs switching; hold 2 inputs LOW and 2 inputs HIGH (at V_{CC} – 0.6V); C_L = 100pF; 500Ω pull–down; no pull–up.

$$\overset{\mathbf{1}}{\left[25pF \times 3V \sum_{i=1}^{4} 50MHz\right]} + \overset{\mathbf{2}}{0.3mA(2)}$$

=15mA + 0.6mA = 15.6mA

These unloaded terms contribute only 10% of the total I_{CC} current.

$$\overset{\mathbf{3}}{(2.8V - 0.2V) \sum_{i=1}^{4} 100pF(50MHz)} + \overset{\mathbf{4}}{\sum_{i=1}^{6} \frac{2.8V}{500\Omega}}$$

= 52mA + 33.6mA = 85.6mA

In this example, terms three and four contribute over 55% of the total I_{CC} current. This part of I_{CC} is entirely due to external loading.

$$\overset{\mathbf{5}}{(2.8V - 0.2V) \sum_{i=1}^{4} 100pF(50MHz)} + \overset{\mathbf{6}}{\sum_{i=1}^{6} \frac{3V - 0.2V}{\infty}}$$

= 52mA + 0 = 52mA

These terms are not I_{CC} currents, but rather currents "sinked" by the lower structure of the device. The total current from all terms is 153.2mA.

2. Finding PD (V x I)

When calculating the total power dissipation of the device, the first two terms are multiplied by V_{CC}, which in this example is

3V(15.6mA) = 46.8mW

The third and fourth terms are multiplied by the voltage drop across the upper structure of the device, V_{CC}–V_{OH}. This is approximately 0.2V.

0.2V(85.6mA) = 17.1mW

The fifth and sixth terms are multiplied by the voltage drop across the lower structure of the device, V_{OL}.

0.2V(52mA) = 10.4mW

The total estimated power dissipation of an LCX 244 with 4 outputs switching, at 85°C, with V_{CC}=3V, with 2 outputs held static Low, and 2 inputs at 2.4V with 100pF capacitive loads, 500Ω pull–downs, and 50MHz switching frequency is:

74.3 mW

3. Θ_{JA} Value

The θ_{JA} for a 20–pin TSSOP is approximately 140°C/W.

4. Final Calculations for T_J for the LCX244

$T_J = (P_D \times \Theta_{JA}) + T_A$ = (0.0743W × 140°C/W) + 85°C = 95.4°C. LCX runs cool — well below the point for reliability worries. Using the Arrhenius Equation (Eq 1 on page 11), the time to 0.1% bond failures is approximately 30 years.

System Considerations

The manner in which an IC package is mounted and positioned in its surrounding environment will have significant effects on operating junction temperatures. These conditions are under the control of the system designer and are worthy of serious consideration in PC board layout and system ventilation and airflow.

Forced–air cooling will significantly reduce Θ_{JA}. Air flow parallel to the long dimension of the package is generally a few percent more effective than air flow perpendicular to the long dimension of the package. In actual board layouts, other components can provide air flow blocking and flow turbulence, which may reflect the net reduction of Θ_{JA} of a specific component.

External heat sinks applied to an IC package can improve thermal resistance by increasing heat flow to the ambient environment. Heat sink performance will vary by size, material, design, and system air flow. Heat sinks can provide a substantial improvement.

Package mounting can affect thermal resistance. Surface mount packages dissipate significant amounts of heat through the leads. Improving heat flow from package leads to ambient will decrease thermal resistance.

- *Metal (copper) traces* on PC boards conduct heat away from the package and dissipate it to the ambient; thus the larger the trace area the lower the thermal resistance.
- *Package stand–off* has a small effect on Θ_{JA}. Boards with higher thermal conductivity (ceramic) may show the most pronounced benefit.
- The use of *thermally conductive adhesive* under SO packages can lower thermal resistance by providing a direct heat flow path from the package to board. Naturally high thermal conductivity board material and/or cool board temperatures amplify this effect.
- *High thermal conductive board material* will decrease thermal resistance. A change in board material from epoxy laminate to ceramic will help reduce thermal resistance.

Conclusion

Thermal management remains a major concern of producers and users of IC's. An increase in Θ_{JA} is the major trade–off one must accept for package miniaturization. When the user considers all of the variables that affect the IC junction temperature, he is then prepared to take maximum advantage of the tools, materials and data that are available.

References

1. "High Performance ECL Data – ECLinPS and ECLinPS Lite," Motorola, pp. 4–32.
2. "Thermal Considerations for Advanced Logic Families; AN241," Philips Semiconductors

Reliability Audit Program Summary

The Motorola Logic Reliability Audit Program (RAP) is designed to monitor the ability of Logic products to exceed minimum acceptable reliability standards. Mesa Reliability Engineering has overall responsibility for RAP, including updating requirements, interpreting results, offshore administration, and monthly reporting.

Testing

RAP is a system of mechanical, environmental, and electrical tests performed periodically on randomly selected samples of standard products. Each sample receives minimum standard tests covering all wafer fab sites, assembly sites, and packages. Within each family, devices are chosen to represent the range of die sizes and functional complexity.

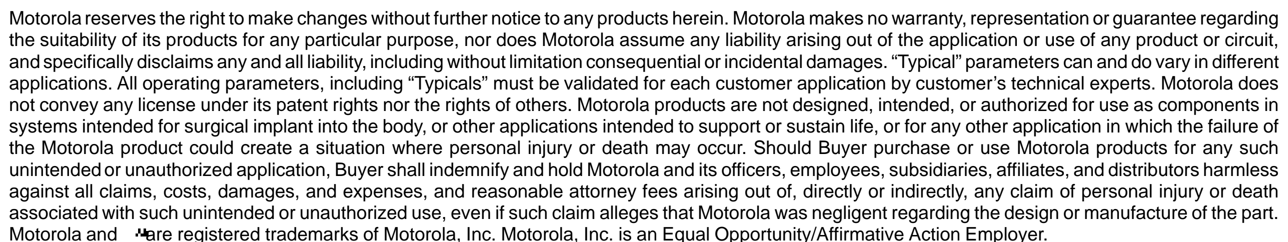
In addition to standard tests, each package type also receives special pre–conditioning tests, the frequency of which is intended to sample every package type and assembly site once per month.

Reliability tests are run at three sites: Mesa, Arizona (LICD); Manila, Philippines (MPI); and Taipei, Taiwan (METL). Following mechanical and electrical testing, devices receive standard static and functional electrical tests using conditions and limits per applicable device specifications.

Failures

All failed devices require recorded data. Failure data and failure verification information accompany all rejects to a product analysis lab where root cause failure analysis is performed on all occurrences observed at that site. All information regarding failed units is logged into a tracking database.

A review is called if any sample has a failure. The findings are analyzed relative to past performance to determine if customers are at risk for abnormally high failure rates. Customer notification may then be required and, if needed, is prepared and distributed. Following the completion of testing and data review, the local reliability engineering group enters all data into the Reliability Audit Program Database.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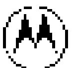

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