

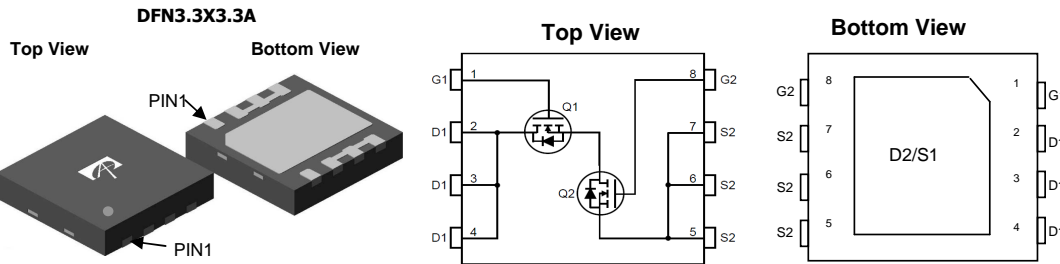
General Description

The AON7902 is designed to provide a high efficiency synchronous buck power stage with optimal layout and board space utilization. It includes two specialized MOSFETs in a dual Power DFN3.3x3.3A package. The Q1 "High Side" MOSFET is designed to minimize switching losses. The Q2 "Low Side" MOSFET use advance trench technology with a monolithically integrated Schottky to provide excellent $R_{DS(ON)}$ and low gate charge. The AON7902 is well suited for use in compact DC/DC converter applications.

Product Summary

| | Q1 | Q2 |
|------------------------------------|---------------|----------------|
| V_{DS} | 30V | 30V |
| I_D (at $V_{GS}=10V$) | 27A | 40A |
| $R_{DS(ON)}$ (at $V_{GS}=10V$) | <21m Ω | <6.2m Ω |
| $R_{DS(ON)}$ (at $V_{GS} = 4.5V$) | <28m Ω | <7.4m Ω |

100% UIS Tested
 100% Rg Tested



Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

| Parameter | Symbol | Max Q1 | Max Q2 | Units |
|---|------------------|------------------|----------|------------|
| Drain-Source Voltage | V_{DS} | 30 | | V |
| Gate-Source Voltage | V_{GS} | ± 20 | ± 12 | V |
| Continuous Drain Current ^C | I_D | 24 | 40 | A |
| Current ^C | | $T_C=25^\circ C$ | 15 | |
| Pulsed Drain Current ^C | I_{DM} | 90 | 150 | |
| Continuous Drain Current | I_{DSM} | 8 | 13 | A |
| Current | | $T_A=25^\circ C$ | 6 | |
| Avalanche Current ^C | I_{AS}, I_{AR} | 22 | 36 | A |
| Avalanche Energy $L=0.1mH$ ^C | E_{AS}, E_{AR} | 24 | 65 | mJ |
| Power Dissipation ^B | P_D | 17 | 50 | W |
| | | $T_C=25^\circ C$ | 7 | |
| Power Dissipation ^A | P_{DSM} | 1.8 | 1.8 | W |
| | | $T_A=25^\circ C$ | 1.1 | |
| Junction and Storage Temperature Range | T_J, T_{STG} | -55 to 150 | | $^\circ C$ |

Thermal Characteristics

| Parameter | Symbol | Typ Q1 | Typ Q2 | Max Q1 | Max Q2 | Units |
|---|-----------------|--------------|--------|--------|--------|--------------|
| Maximum Junction-to-Ambient ^A | $R_{\theta JA}$ | 27 | 27 | 35 | 35 | $^\circ C/W$ |
| Maximum Junction-to-Ambient ^{AD} | | Steady-State | 60 | 60 | 72 | |
| Maximum Junction-to-Case | $R_{\theta JC}$ | 6 | 2 | 7.5 | 2.5 | $^\circ C/W$ |

Q1 Electrical Characteristics (T_J=25°C unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-----------------------------|---------------------------------------|---|-----|----------|----------|-------|
| STATIC PARAMETERS | | | | | | |
| BV _{DSS} | Drain-Source Breakdown Voltage | I _D =250μA, V _{GS} =0V | 30 | | | V |
| I _{DSS} | Zero Gate Voltage Drain Current | V _{DS} =30V, V _{GS} =0V T _J =55°C | | | 1 5 | μA |
| I _{GSS} | Gate-Body leakage current | V _{DS} =0V, V _{GS} = ±20V | | | 100 | nA |
| V _{GS(th)} | Gate Threshold Voltage | V _{DS} =V _{GS} , I _D =250μA | 1.3 | 1.8 | 2.3 | V |
| I _{D(ON)} | On state drain current | V _{GS} =10V, V _{DS} =5V | 90 | | | A |
| R _{DS(ON)} | Static Drain-Source On-Resistance | V _{GS} =10V, I _D =8A T _J =125°C | | 17 24 | 21 29 | mΩ |
| | | V _{GS} =4.5V, I _D =4A | | 22 | 28 | |
| g _{FS} | Forward Transconductance | V _{DS} =5V, I _D =8A | | 33 | | S |
| V _{SD} | Diode Forward Voltage | I _S =1A, V _{GS} =0V | | 0.7 | | V |
| I _S | Maximum Body-Diode Continuous Current | | | | 20 | A |
| DYNAMIC PARAMETERS | | | | | | |
| C _{iss} | Input Capacitance | V _{GS} =0V, V _{DS} =15V, f=1MHz | 470 | 590 | 710 | pF |
| C _{oss} | Output Capacitance | | 250 | 360 | 470 | pF |
| C _{riss} | Reverse Transfer Capacitance | | 13 | 23 | 40 | pF |
| R _g | Gate resistance | V _{GS} =0V, V _{DS} =0V, f=1MHz | 0.7 | 1.5 | 2.3 | Ω |
| SWITCHING PARAMETERS | | | | | | |
| Q _{g(10V)} | Total Gate Charge | V _{GS} =10V, V _{DS} =15V, I _D =8A | 7 | 9 | 11.0 | nC |
| Q _{g(4.5V)} | Total Gate Charge | | 3 | 4 | 5.0 | nC |
| Q _{gs} | Gate Source Charge | | | 1.5 | | nC |
| Q _{gd} | Gate Drain Charge | | | 1.5 | | nC |
| t _{D(on)} | Turn-On DelayTime | V _{GS} =10V, V _{DS} =15V, R _L =1.8Ω, R _{GEN} =3Ω | | 6 | | ns |
| t _r | Turn-On Rise Time | | | 3 | | ns |
| t _{D(off)} | Turn-Off DelayTime | | | 18 | | ns |
| t _f | Turn-Off Fall Time | | | 3 | | ns |
| t _{rr} | Body Diode Reverse Recovery Time | I _F =8A, dI/dt=500A/μs | 8 | 11 | 14 | ns |
| Q _{rr} | Body Diode Reverse Recovery Charge | I _F =8A, dI/dt=500A/μs | 15 | 19 | 23 | nC |

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150°C. The SOA curve provides a single pulse rating g.

G. The maximum current rating is limited by package.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.

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Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

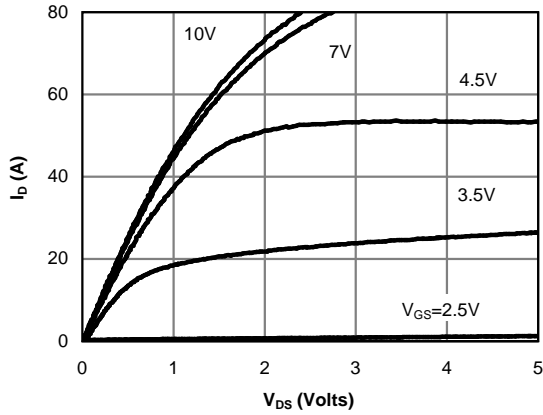


Fig 1: On-Region Characteristics (Note E)

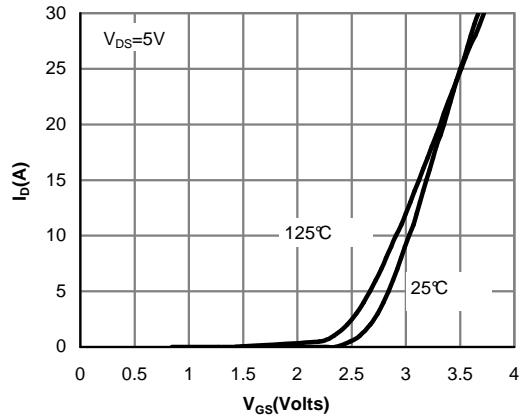


Figure 2: Transfer Characteristics (Note E)

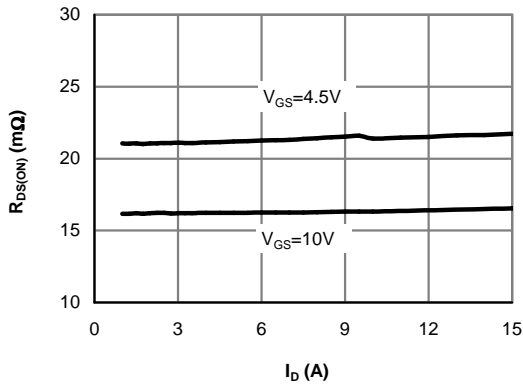


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

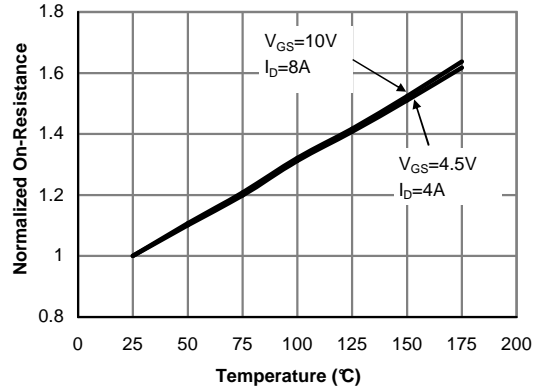


Figure 4: On-Resistance vs. Junction Temperature (Note E)

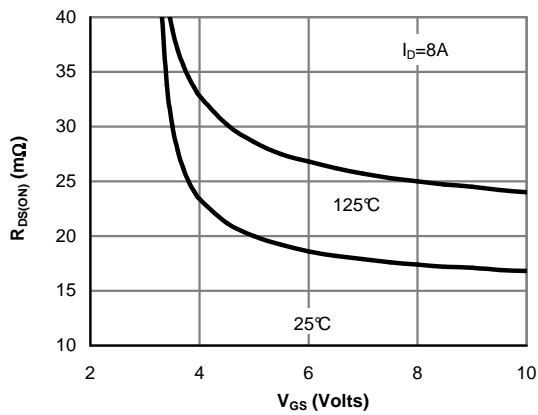


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

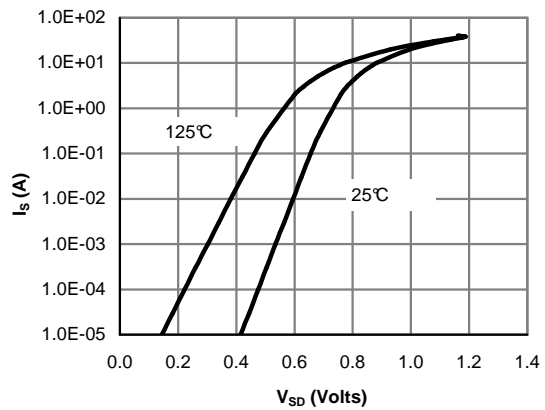


Figure 6: Body-Diode Characteristics (Note E)

Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

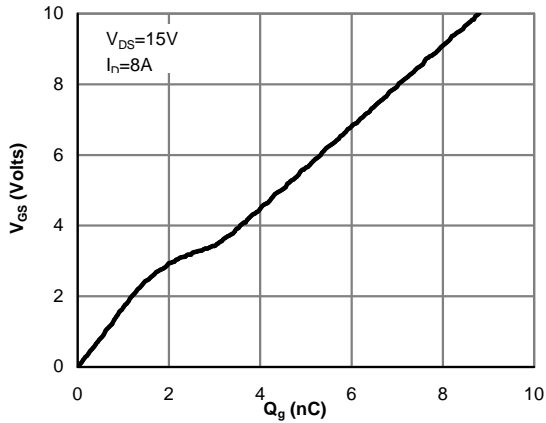


Figure 7: Gate-Charge Characteristics

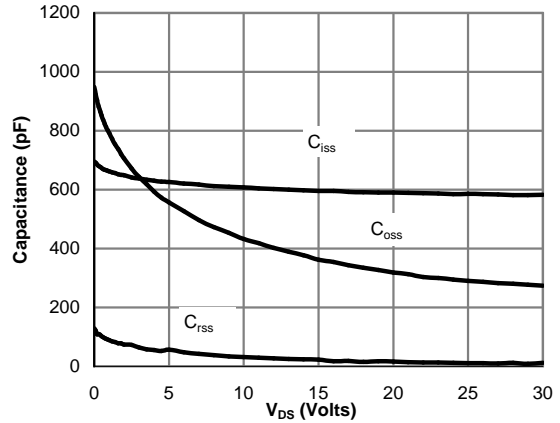


Figure 8: Capacitance Characteristics

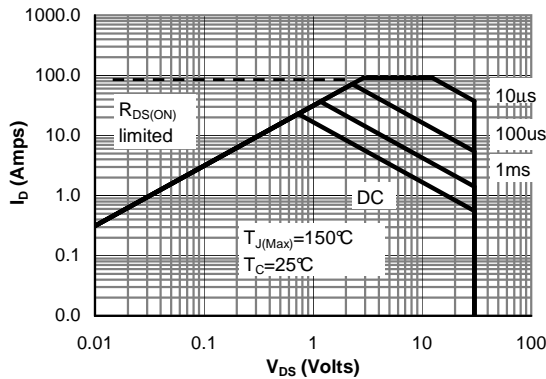


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

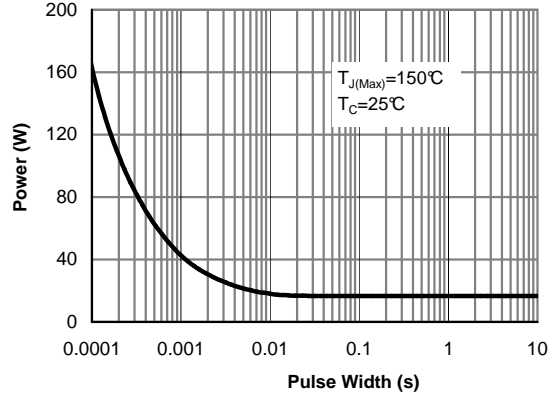


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

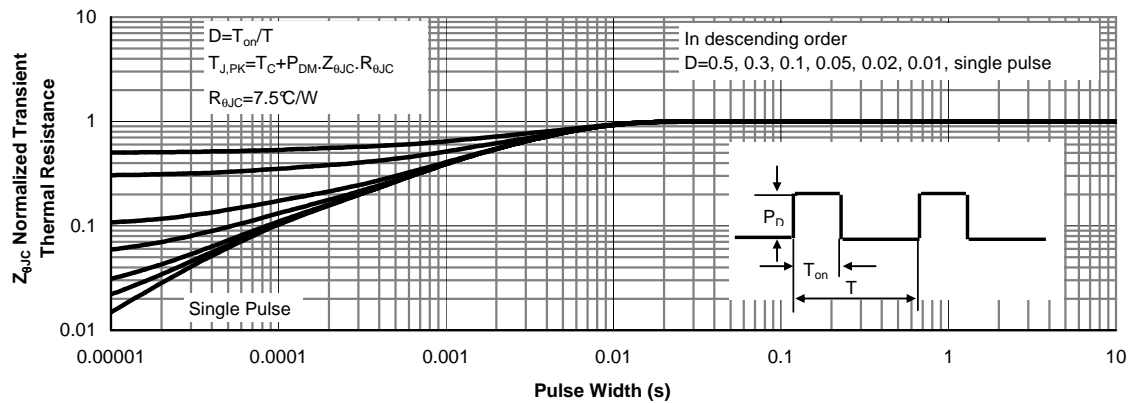


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

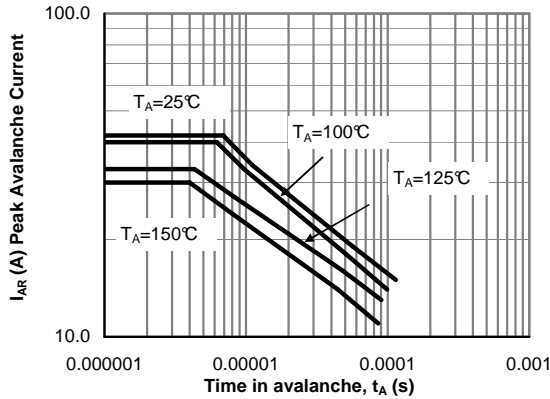


Figure 12: Single Pulse Avalanche capability (Note C)

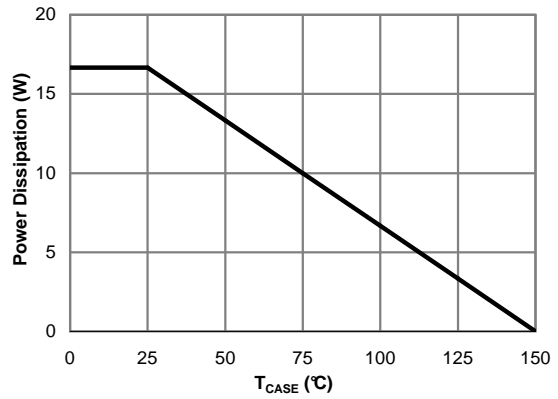


Figure 13: Power De-rating (Note F)

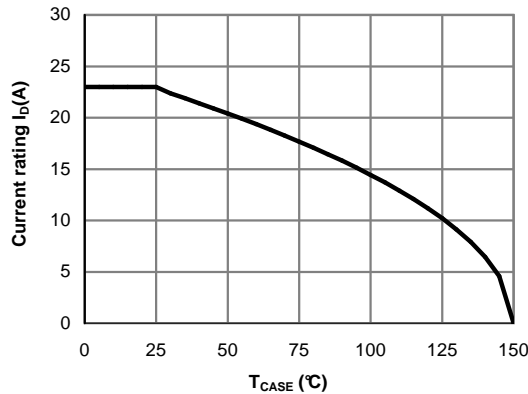


Figure 14: Current De-rating (Note F)

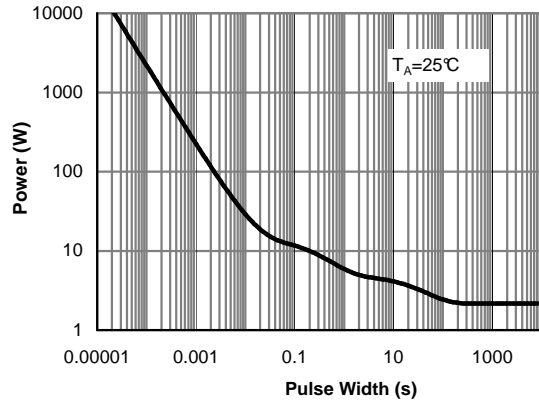


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

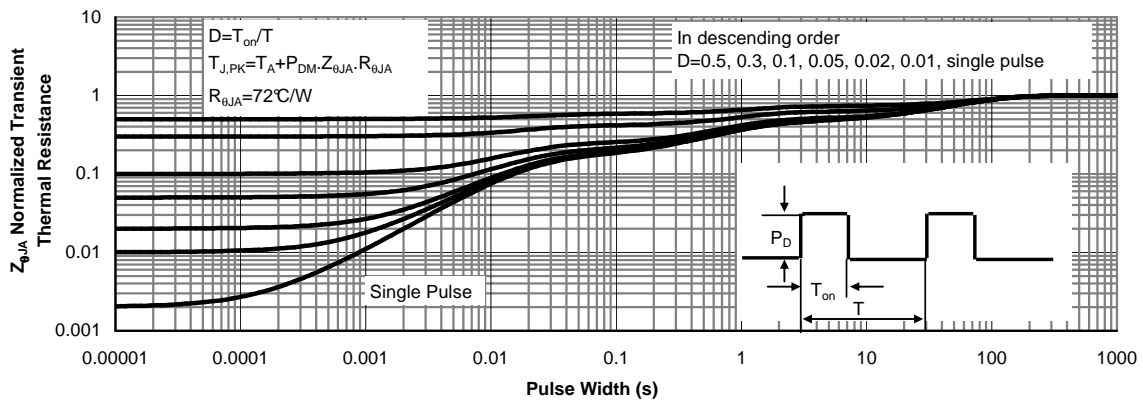


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

Q2 Electrical Characteristics (T_J=25°C unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-----------------------------|--|---|------|------------|------------|-------|
| STATIC PARAMETERS | | | | | | |
| BV _{DSS} | Drain-Source Breakdown Voltage | I _D =10mA, V _{GS} =0V | 30 | | | V |
| I _{DSS} | Zero Gate Voltage Drain Current | V _{DS} =30V, V _{GS} =0V T _J =55°C | | | 0.5 500 | mA |
| I _{GSS} | Gate-Body leakage current | V _{DS} =0V, V _{GS} = ±12V | | | 100 | nA |
| V _{GS(th)} | Gate Threshold Voltage | V _{DS} =V _{GS} , I _D =250μA | 1.1 | 1.6 | 2.1 | V |
| I _{D(ON)} | On state drain current | V _{GS} =10V, V _{DS} =5V | 150 | | | A |
| R _{DS(ON)} | Static Drain-Source On-Resistance | V _{GS} =10V, I _D =13A T _J =125°C | | 5.1 7.4 | 6.2 9 | mΩ |
| | | V _{GS} =4.5V, I _D =10A | | 5.7 | 7.4 | mΩ |
| g _{FS} | Forward Transconductance | V _{DS} =5V, I _D =13A | | 50 | | S |
| V _{SD} | Diode Forward Voltage | I _S =1A, V _{GS} =0V | | 0.4 | 0.7 | V |
| I _S | Maximum Body-Diode Continuous Current ⁶ | | | | 40 | A |
| DYNAMIC PARAMETERS | | | | | | |
| C _{iss} | Input Capacitance | V _{GS} =0V, V _{DS} =15V, f=1MHz | 2800 | 3500 | 4200 | pF |
| C _{oss} | Output Capacitance | | 360 | 520 | 680 | pF |
| C _{riss} | Reverse Transfer Capacitance | | 150 | 260 | 450 | pF |
| R _g | Gate resistance | V _{GS} =0V, V _{DS} =0V, f=1MHz | 0.6 | 1.2 | 1.8 | Ω |
| SWITCHING PARAMETERS | | | | | | |
| Q _{g(4.5V)} | Total Gate Charge | V _{GS} =10V, V _{DS} =15V, I _D =13A | 22 | 28 | 34 | nC |
| Q _{gs} | Gate Source Charge | | | | 9 | nC |
| Q _{gd} | Gate Drain Charge | | | | 11 | nC |
| t _{D(on)} | Turn-On DelayTime | V _{GS} =10V, V _{DS} =15V, R _L =1.2Ω, R _{GEN} =3Ω | | 8 | | ns |
| t _r | Turn-On Rise Time | | | 5 | | ns |
| t _{D(off)} | Turn-Off DelayTime | | | 50 | | ns |
| t _f | Turn-Off Fall Time | | | 8 | | ns |
| t _{rr} | Body Diode Reverse Recovery Time | I _F =13A, dI/dt=500A/μs | 10 | 13 | 16 | ns |
| Q _{rr} | Body Diode Reverse Recovery Charge | I _F =13A, dI/dt=500A/μs | 16 | 21 | 26 | nC |

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150°C. The SOA curve provides a single pulse rating g.

G. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.

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Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

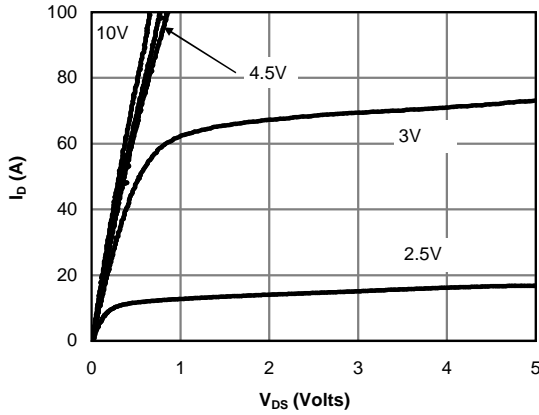


Fig 1: On-Region Characteristics (Note E)

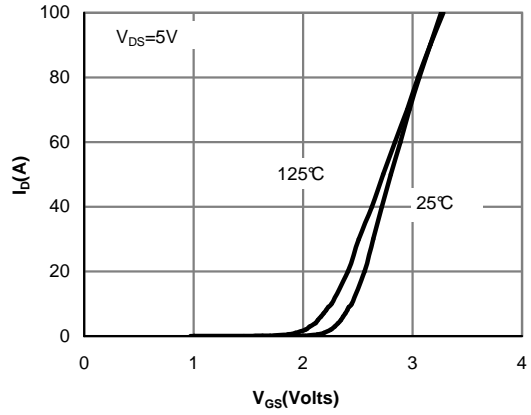


Figure 2: Transfer Characteristics (Note E)

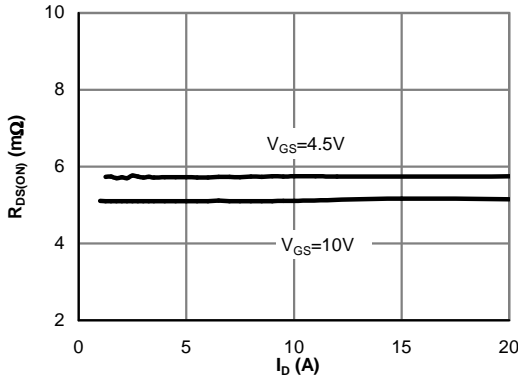


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

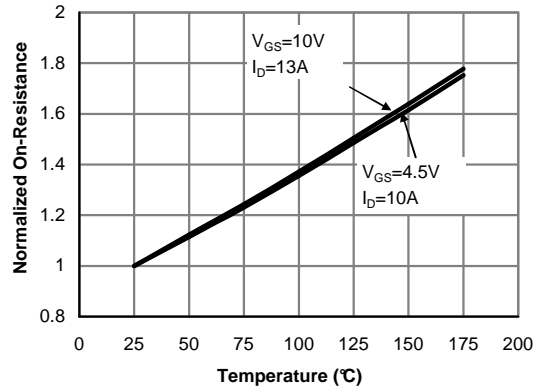


Figure 4: On-Resistance vs. Junction Temperature (Note E)

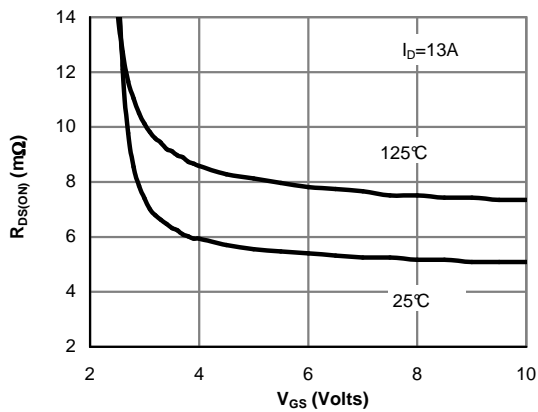


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

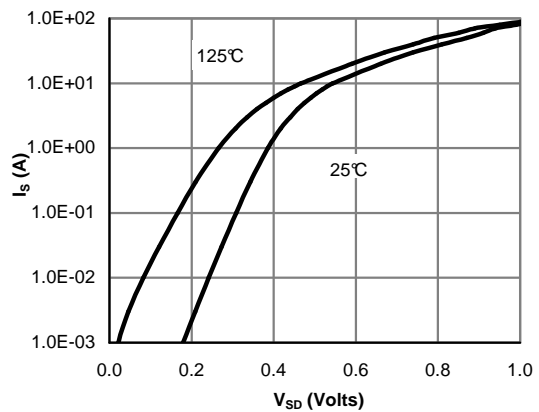


Figure 6: Body-Diode Characteristics (Note E)

Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

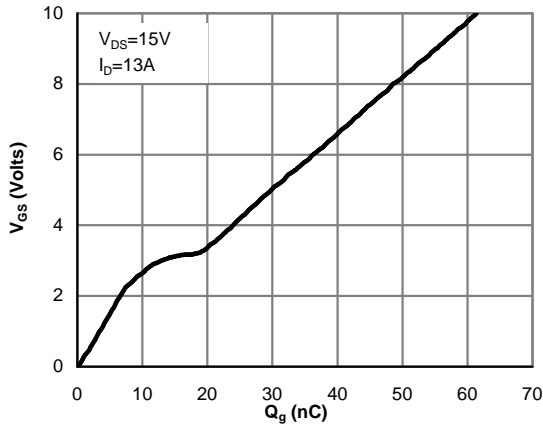


Figure 7: Gate-Charge Characteristics

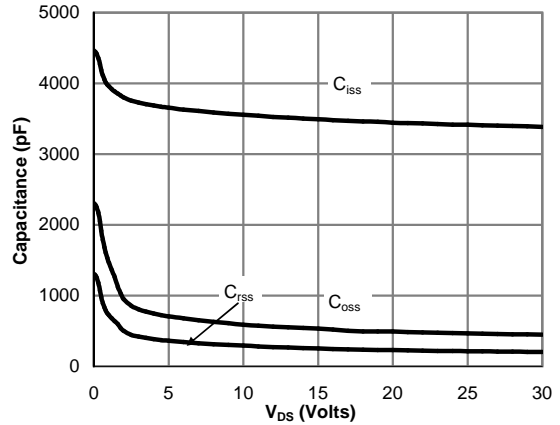


Figure 8: Capacitance Characteristics

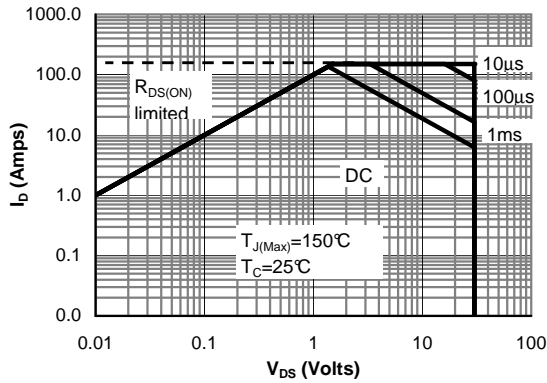


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

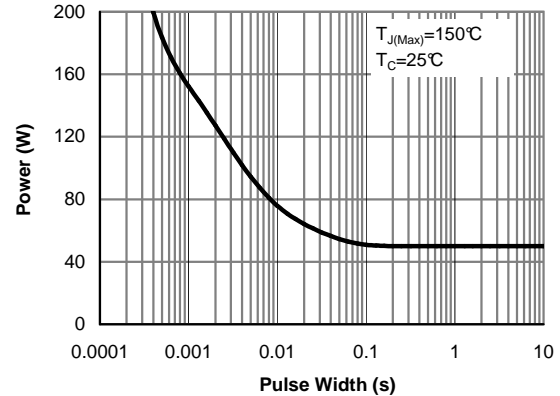


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

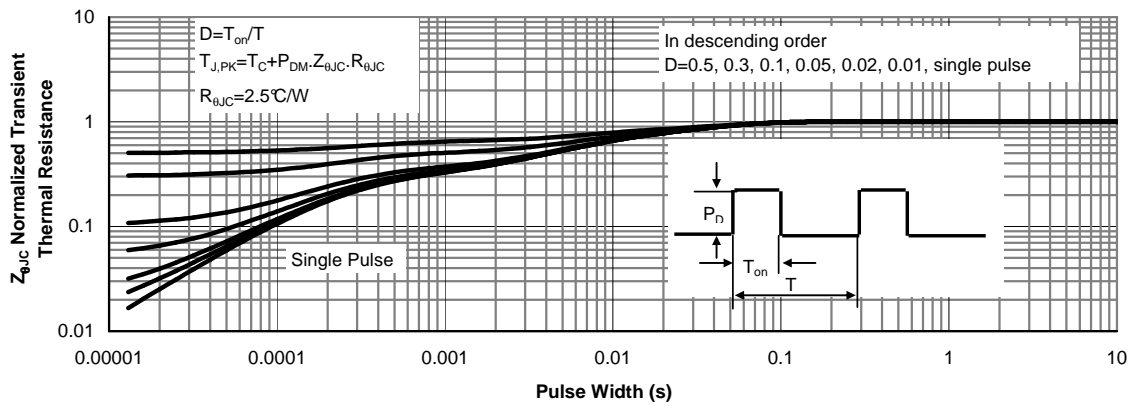


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

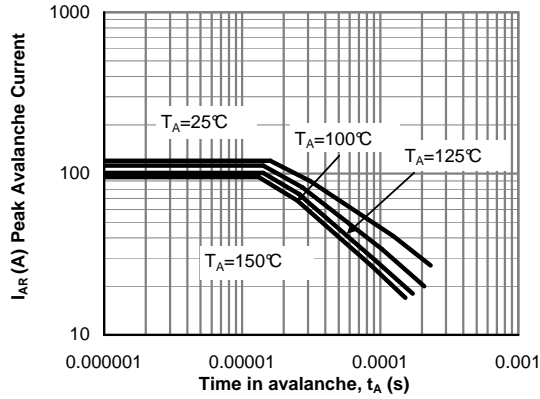


Figure 12: Single Pulse Avalanche capability (Note C)

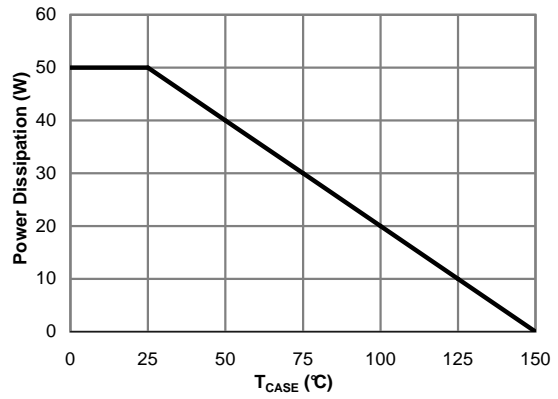


Figure 13: Power De-rating (Note F)

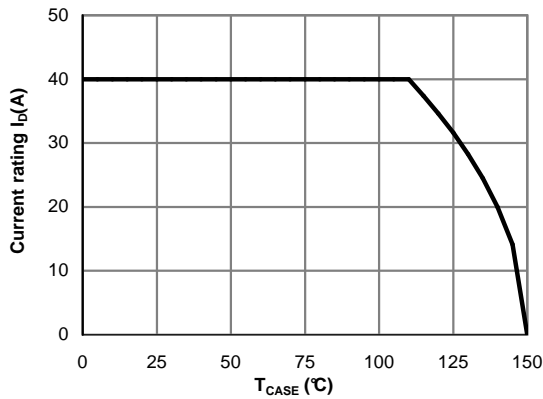


Figure 14: Current De-rating (Note F)

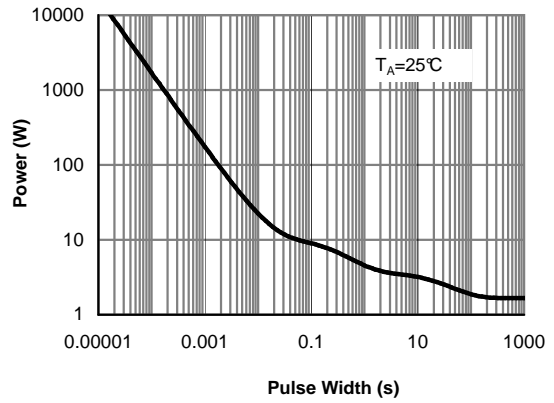


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note G)

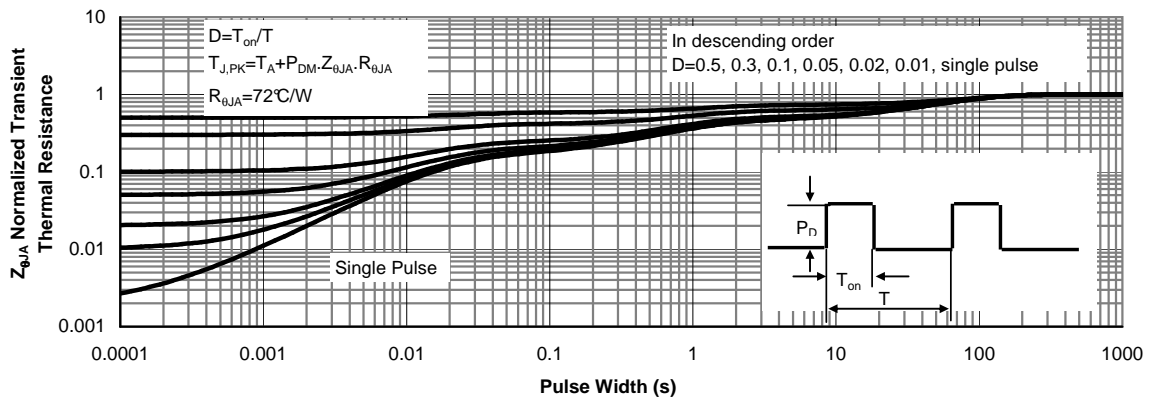


Figure 16: Normalized Maximum Transient Thermal Impedance (Note G)

Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

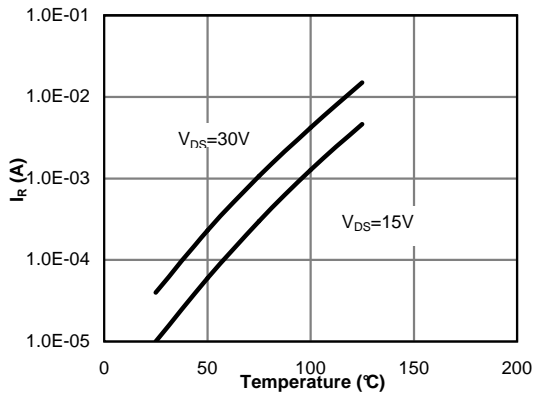


Figure 17: Diode Reverse Leakage Current vs. Junction Temperature

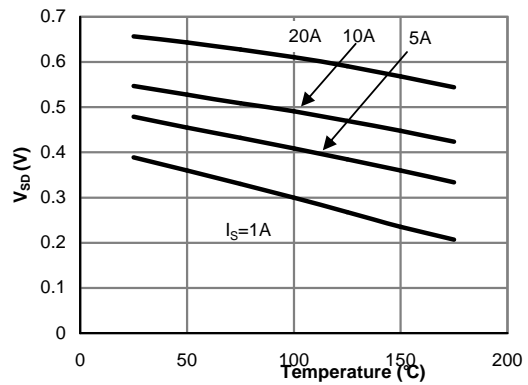


Figure 18: Diode Forward Voltage vs. Junction Temperature

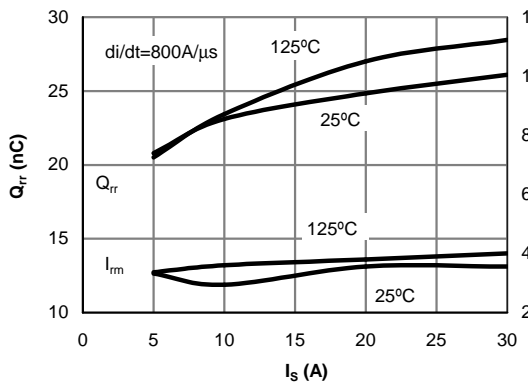


Figure 18: Diode Reverse Recovery Charge and Peak Current vs. Conduction Current

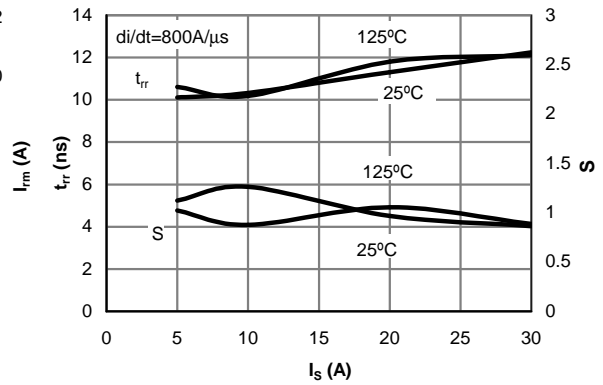


Figure 19: Diode Reverse Recovery Time and Softness Factor vs. Conduction Current

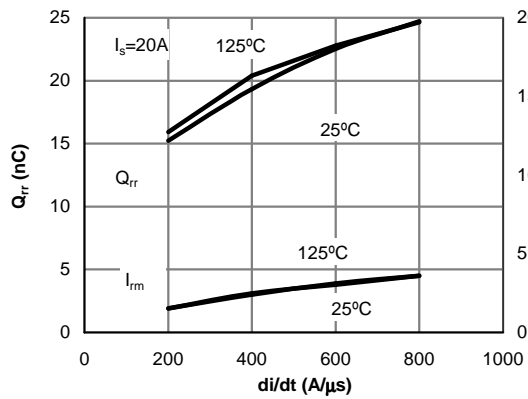


Figure 20: Diode Reverse Recovery Charge and Peak Current vs. di/dt

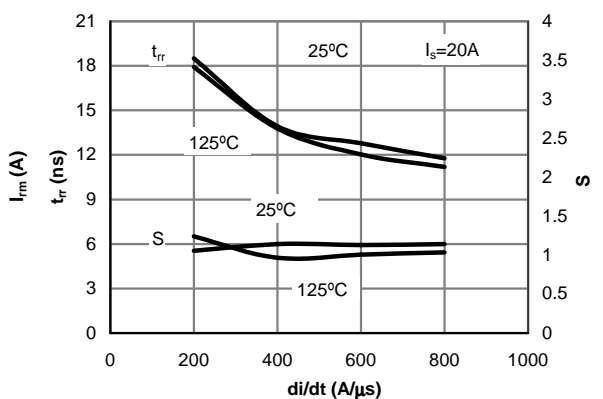
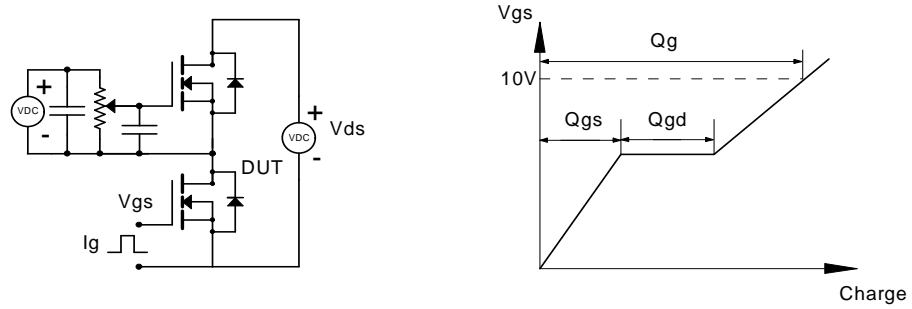
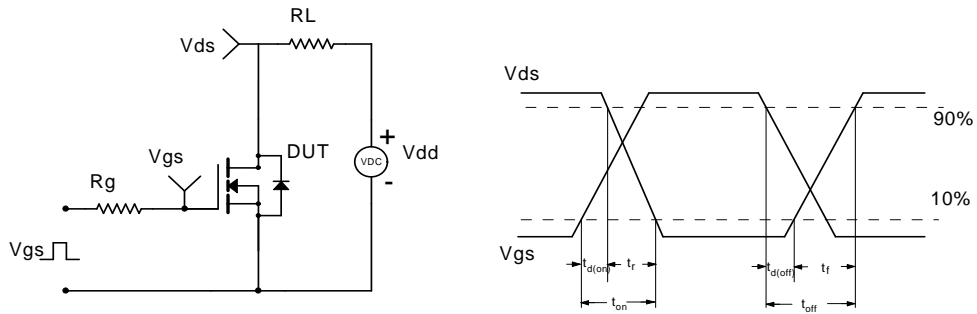


Figure 21: Diode Reverse Recovery Time and Softness Factor vs. di/dt

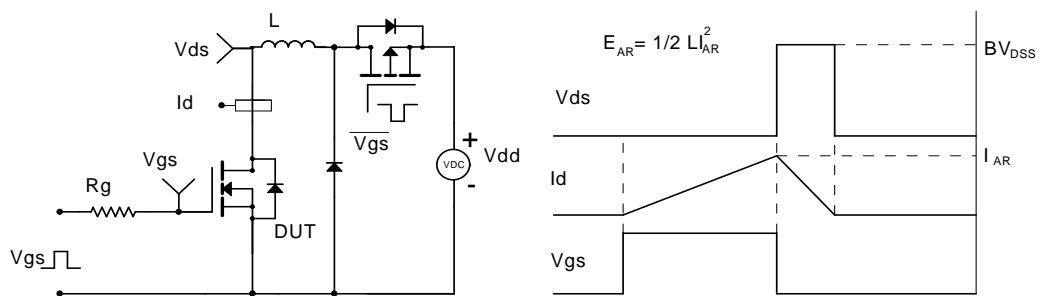
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

