REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET	15	16	17	18	19	20	21												
REV STATUS OF SHEETS				REV															
				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
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REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS, 12 X 10-BIT MATRIX MULTIPLIER, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-93260
A	67268	

SHEET 1 OF 21

DESC FORM 193
JUL 91

5962-E357-94

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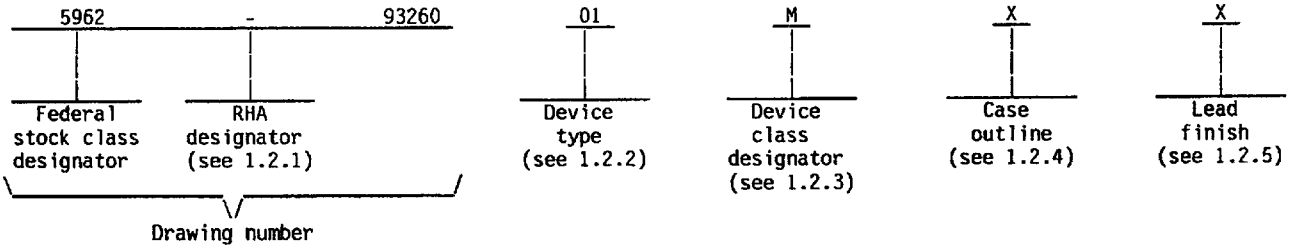
9004708 0007221 439

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Speed
01	LF2250	12 x 10-Bit matrix multiplier	25 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA3-P121	121	Pin grid array

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/2/3/4/

Storage temperature range	-65°C to +150°C
V_{CC} supply voltage with respect to ground range	-0.5 V dc to +7.0 V dc
Input signal with respect to ground range	-0.5 V dc to V_{CC} + 0.5 V dc
Signal applied to high impedance output range	-0.5 V dc to V_{CC} + 0.5 V dc
Output current into low outputs	25 mA
Latch-up current	>400 mA
Power dissipation	1.67 W
Lead temperature (soldering, 10 seconds)	300°C
Junction temperature (T_J)	175°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage range	4.50 V dc ≤ V_{CC} ≤ 5.50 V dc
Operating ambient temperature range	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 5/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Maximum rating indicate stress specification only. Functional operation of these products at values beyond those indicated in operation condition table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.
3/ The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, convention precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.
4/ This devices provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at -0.6 V and V_{CC} +0.6 V. The devices can withstand indefinite operation with inputs in the range of -0.5 V to +7.0 V. Devices operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.
5/ Values will be added when they become available.

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Data modes. The data modes shall be as specified on figure 2.

3.2.4 Block diagrams. The block diagrams shall be as specified on figure 3.

3.2.5 Format diagrams. The input and output format diagrams shall be as specified on figure 4.

3.2.6 Latency equation. The latency equation shall be as specified on figure 5.

3.2.7 Switching waveforms. The switching waveforms shall be as specified on figure 6.

3.2.8 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-I-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Devices type	Limits		Units
					Min	Max	
Output high voltage	V_{OH}	V_{CC} = Min., I_{OH} = -2.0 mA	1,2,3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = Min., I_{OL} = 4.0 mA				0.4	V
Input high voltage	V_{IH}				2.0	V_{CC}	V
Input low voltage	V_{IL}	2/			0.0	0.8	V
Input current	I_{IX}	$GND \le V_{IN} \le V_{CC}$ 3/	2			±10	µA
Output leakage current	I_{OZ}	3/				±40	µA
V_{CC} current, dynamic	I_{CC1}	4/ 5/	1,2,3			160	mA
V_{CC} current, quiescent	I_{CC2}	6/				12	mA
Input capacitance	C_{IN}	T_A = +25°C, f = 1 MHz See 4.4.1c	4			10	pF
Output capacitance	C_{OUT}	T_A = +25°C, f = 1 MHz See 4.4.1c				10	pF
Functional test		See 4.4.1b	7,8				
Cycle time	t_{CYC}	7/ 8/	9,10,11		25		ns
Clock pulse width, LOW	t_{PWL}	7/ 8/			10		ns
Clock pulse width, HIGH	t_{PWH}	7/ 8/			10		ns
Input set-up time	t_S	7/ 8/			9		ns
Input hold time	t_H	7/ 8/			0		ns
Output delay	t_D	7/ 8/				20	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

1/ All testing shall be performed using worst-case test conditions unless otherwise specified.

2/ This devices provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at -0.6 V and V_{CC} +0.6 V. The devices can withstand indefinite operation with inputs in the range of -0.5 V to +7.0 V. Devices operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

3/ These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

4/ Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

5/ Tested with all outputs changing every cycle and no load, at a 20 MHz clock rate.

6/ Tested with all inputs within 0.1 V of V_{CC} or ground, no load.

7/ AC specification are tested with input transition times less than 3 ns, output reference levels of 1.5V (except t_{ENA}/t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current source of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For t_{ENABLE} and $t_{DISABLE}$ measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high speed output capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result,care must be exercised in the testing of the devices. The following measures are recommended:

a. A 0.1 μF ceramic capacitor should be installed between V_{CC} and ground leads as close to the Devices Under Test (DUT) as possible. Similar capacitors should be installed between devices V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain request DUT input levels relative to the DUT ground pin.

8/ Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Set-up time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

Device type	01	Device type	01	Device type	01	Device type	01	Device type	01
Case outline	X	Case outline	X	Case outline	X	Case outline	X	Case outline	X
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
A1	XC_7	B13	B_2	E13	A_8	K1	YC_3	M7	KC_6
A2	XC_9	C1	XC_1	F1	Y_7	K2	ZC_0	M8	KC_9
A3	XC_{10}	C2	XC_2	F2	YC_8	K3	ZC_3	M9	KB_2
A4	$MODE_0$	C3	XC_6	F3	V_{CC}	K11	KA_4	M10	KB_5
A5	C_{11}	C4	V_{CC}	F11	A_7	K12	KA_7	M11	KB_9
A6	C_8	C5	GND	F12	A_6	K13	KA_9	M12	KA_2
A7	C_7	C6	C_{10}	F13	A_5	L1	ZC_1	M13	KA_3
A8	C_5	C7	GND	G1	Y_5	L2	ZC_4	N1	ZC_5
A9	C_3	C8	V_{CC}	G2	Y_6	L3	ZC_6	N2	ZC_8
A10	C_1	C9	C_0	G3	GND	L4	GND	N3	ZC_{10}
A11	B_{10}	C10	B_8	G11	A_3	L5	KC_0	N4	KC_1
A12	B_7	C11	B_5	G12	A_2	L6	GND	N5	KC_3
A13	B_4	C12	B_3	G13	A_4	L7	V_{CC}	N6	KC_5
B1	XC_4	C13	B_1	H1	Y_4	L8	KB_0	N7	KC_7
B2	XC_5	D1	YC_{11}	H2	YC_0	L9	KB_4	N8	KC_8
B3	XC_8	D2	XC_0	H3	V_{CC}	L10	KB_8	N9	KB_1
B4	XC_{11}	D3	XC_3	H11	GND	L11	KA_1	N10	KB_3
B5	$MODE_1$	D4	NC (PIN)	H12	A_0	L12	KA_5	N11	KB_6
B6	C_9	D11	CLK	H13	A_1	L13	KA_6	N12	KB_7
B7	C_6	D12	B_0	J1	YC_1	M1	ZC_2	N13	KA_0
B8	C_4	D13	A_{10}	J2	YC_2	M2	ZC_7	---	---
B9	C_2	E1	YC_9	J3	GND	M3	ZC_9	---	---
B10	B_{11}	E2	YC_{10}	J11	KA_8	M4	ZC_{11}	---	---
B11	B_9	E3	GND	J12	CWE_1	M5	KC_2	---	---
B12	B_6	E11	A_{11}	J13	CWE_0	M6	KC_4	---	---
---	---	E12	9	---	---	---	---	---	---

NOTE: NC = No connect

FIGURE 1. Terminal connections.

Mode selection

Mode 1-0	Operating mode
00	3 x 3 Matrix multiplier
01	9-Tap FIR filter
10	3 x 3 Convolver
11	4 x 2 Convolver

Data port formatting

Pin names											
$Mode_{1-0}$	A_{11-0}	B_{11-0}	C_{11-0}	KA_{9-0}	KB_{9-0}	KC_{9-0}	XC_{11-0}	YC_{11-8}	Y_{7-4}	YC_{3-0}	ZC_{11-0}
00	A_{11-0}	B_{11-0}	C_{11-0}	KA_{9-0}	KB_{9-0}	KC_{9-0}	X_{11-0}	Y_{11-8}	Y_{7-4}	Y_{3-0}	Z_{11-0}
01	A_{11-0}	A_{11-0}	NC	KA_{9-0}	KB_{9-0}	KC_{9-0}	$CASIN_{15-4}$	$CASIN_{3-0}$	NC	$CASOUT_{3-0}$	$CASOUT_{15-4}$
10	A_{11-0}	B_{11-0}	C_{11-0}	KA_{9-0}	KB_{9-0}	KC_{9-0}	$CASIN_{15-4}$	$CASIN_{3-0}$	NC	$CASOUT_{3-0}$	$CASOUT_{15-4}$
11	A_{11-0}	B_{11-0}	NC	KA_{9-0}	KB_{9-0}	KC_{9-0}	$CASIN_{15-4}$	$CASIN_{3-0}$	NC	$CASOUT_{3-0}$	$CASOUT_{15-4}$

Coefficient inputs

Input port	Register available
KA	KA_1, KA_2, KA_3
KB	KB_1, KB_2, KB_3
KC	KC_1, KC_2, KC_3

Coefficient registers update

CWE_{1-0}	Coefficient set
00	Hold all register
01	KA_1, KB_1, KC_1
10	KA_2, KB_2, KC_2
11	KA_3, KB_3, KC_3

FIGURE 2. Data modes.

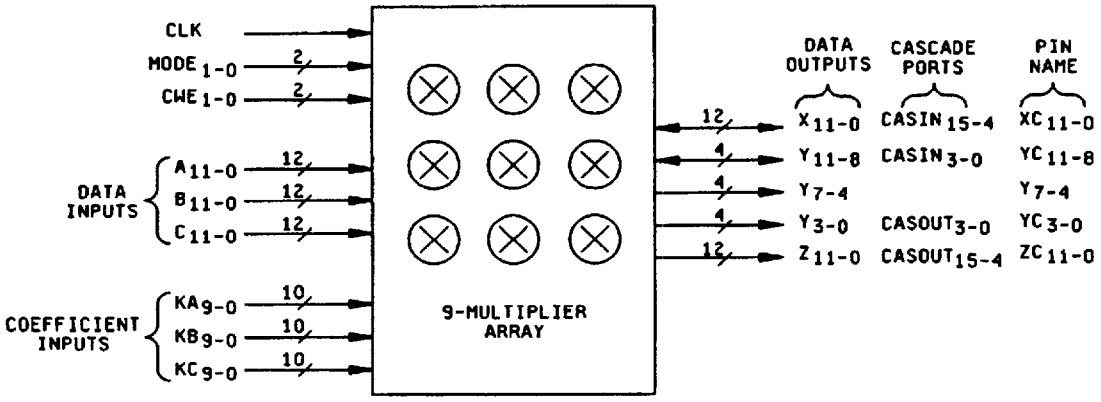
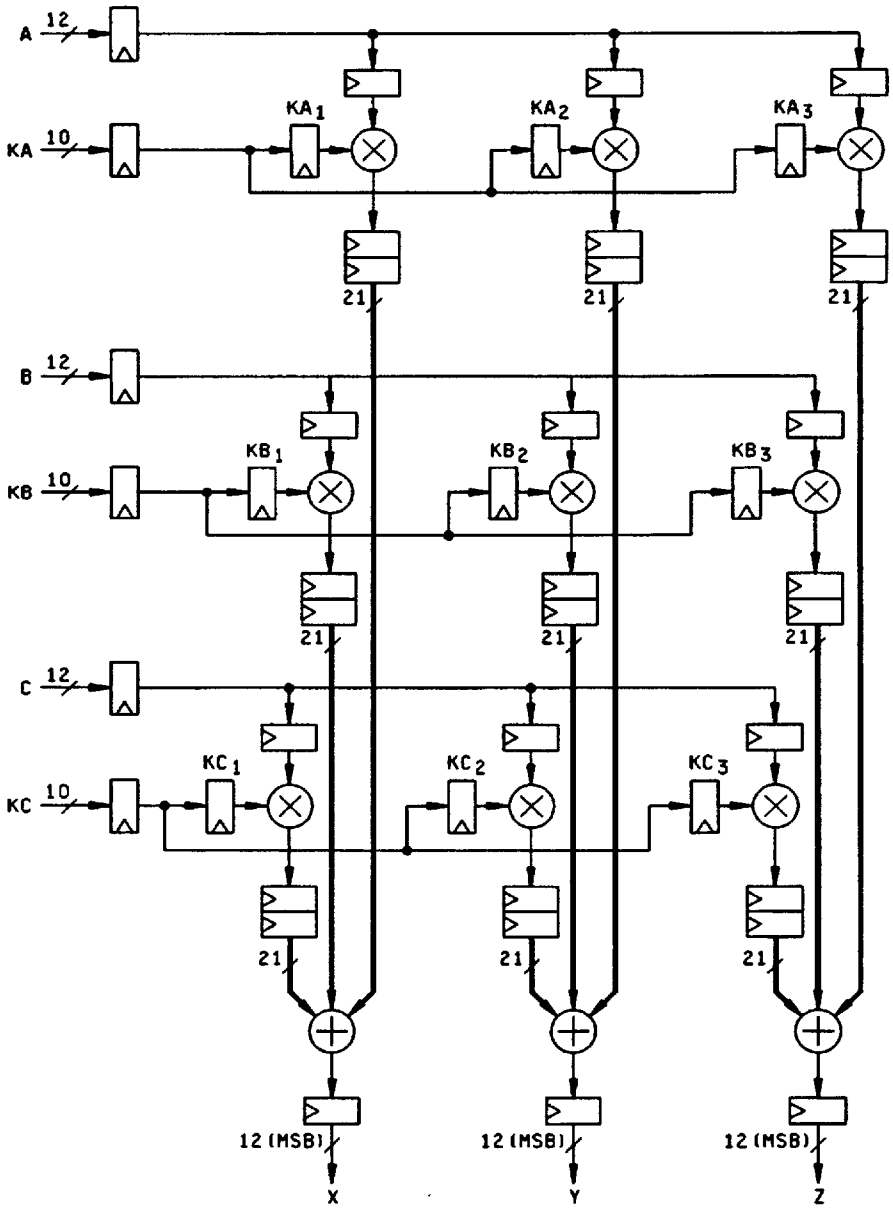
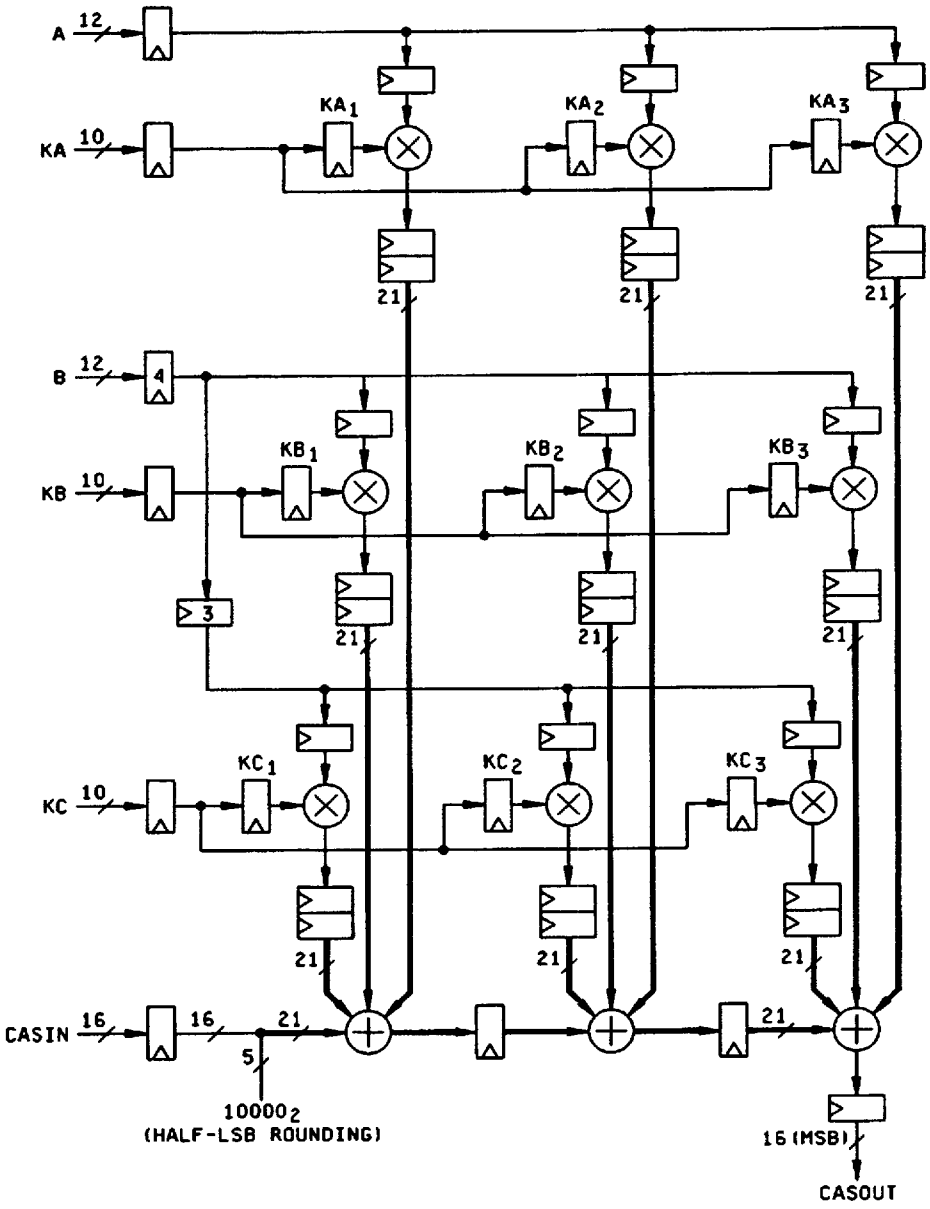


FIGURE 3. Block diagrams.



3 x 3 Matrix multiplier (mode 00)

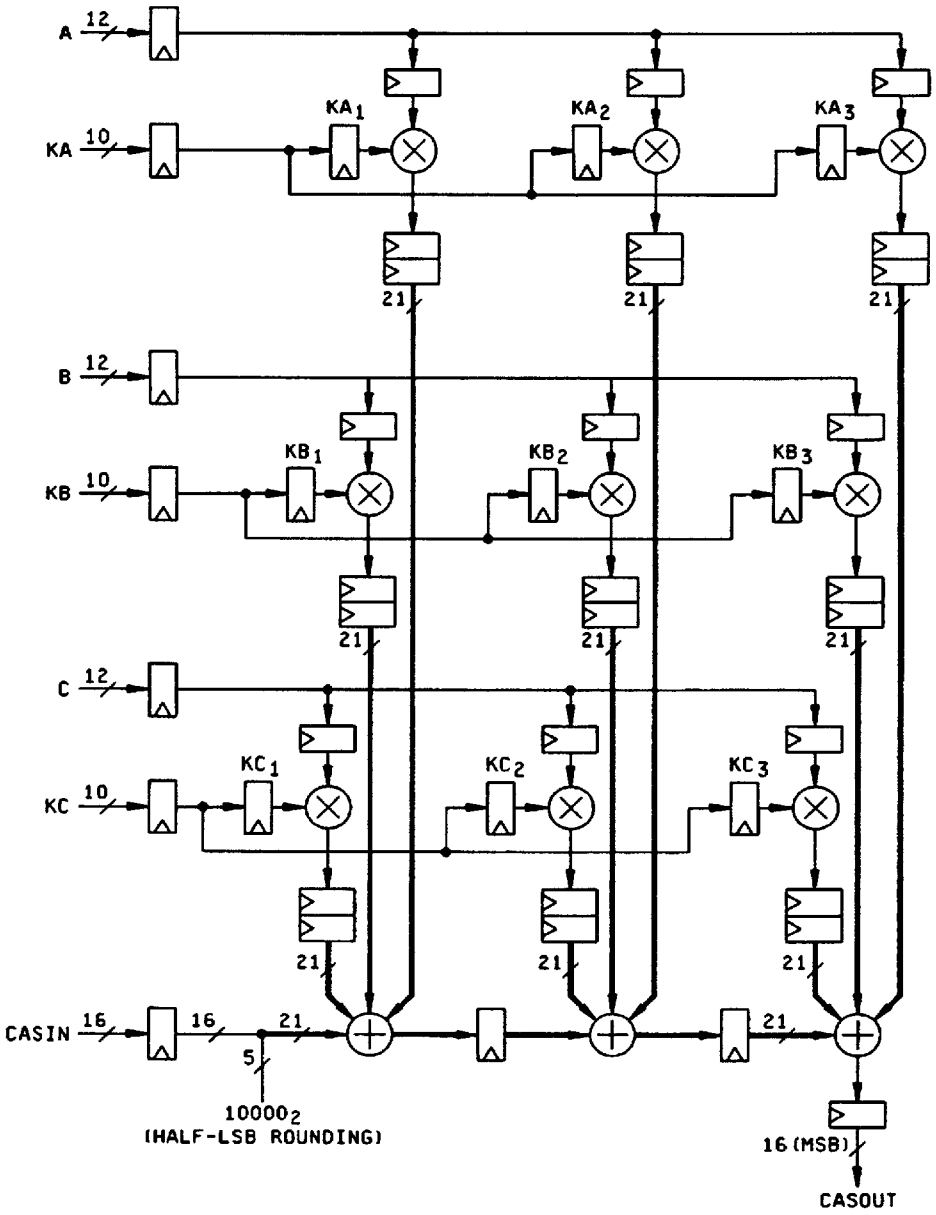
FIGURE 3. Block diagrams - Continued.



Note: Numbers in registers indicate number of pipeline delays

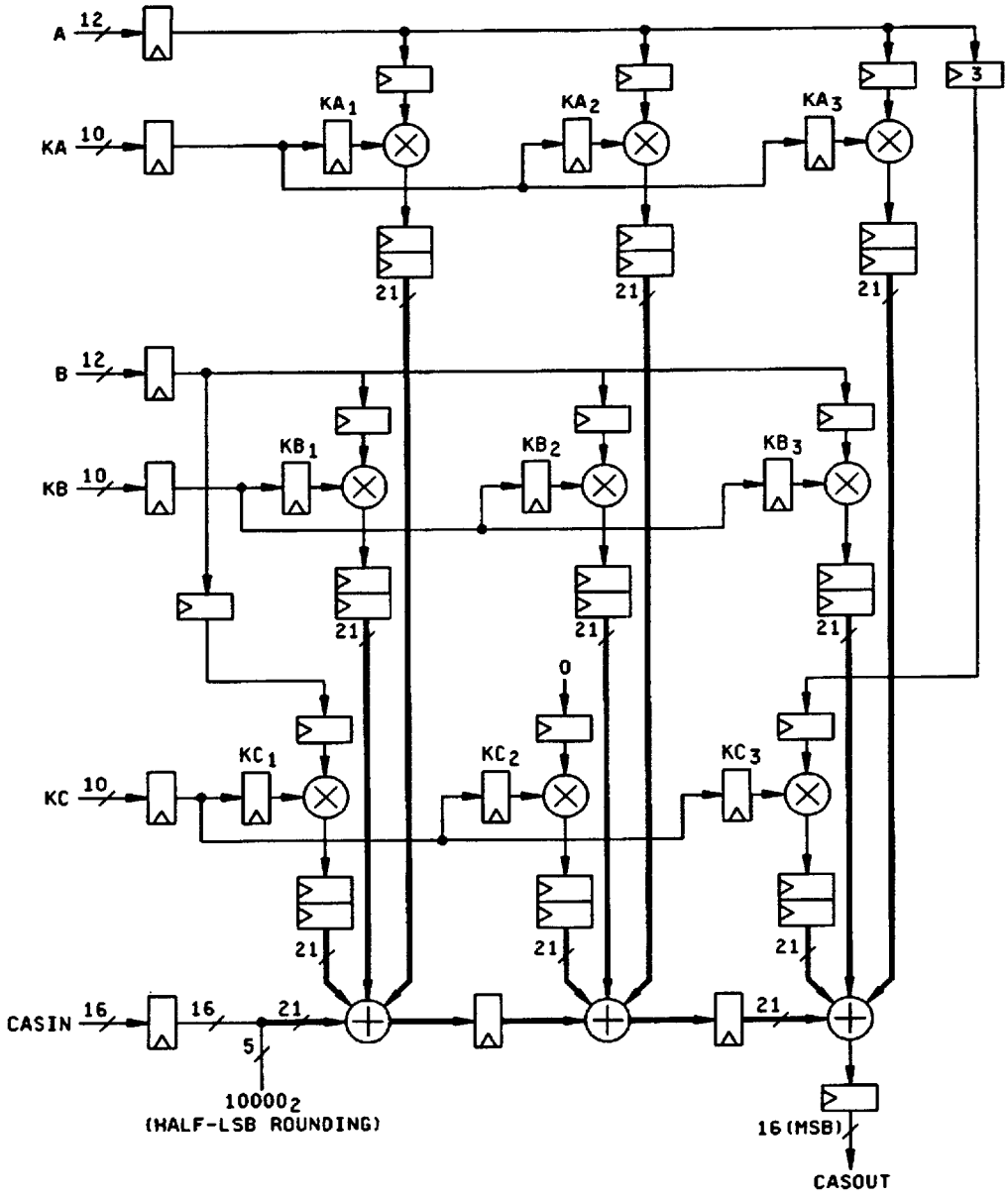
9-Tap FIR filter (mode 01)

FIGURE 3. Block diagrams - Continued.



3 x 3-Pixel convolver (mode 10)

FIGURE 3. Block diagrams - Continued.



Note: Numbers in registers indicate number of pipeline delays

4 x 2-Pixel convolver (mode 11)

FIGURE 3. Block diagrams - Continued.

Input formats

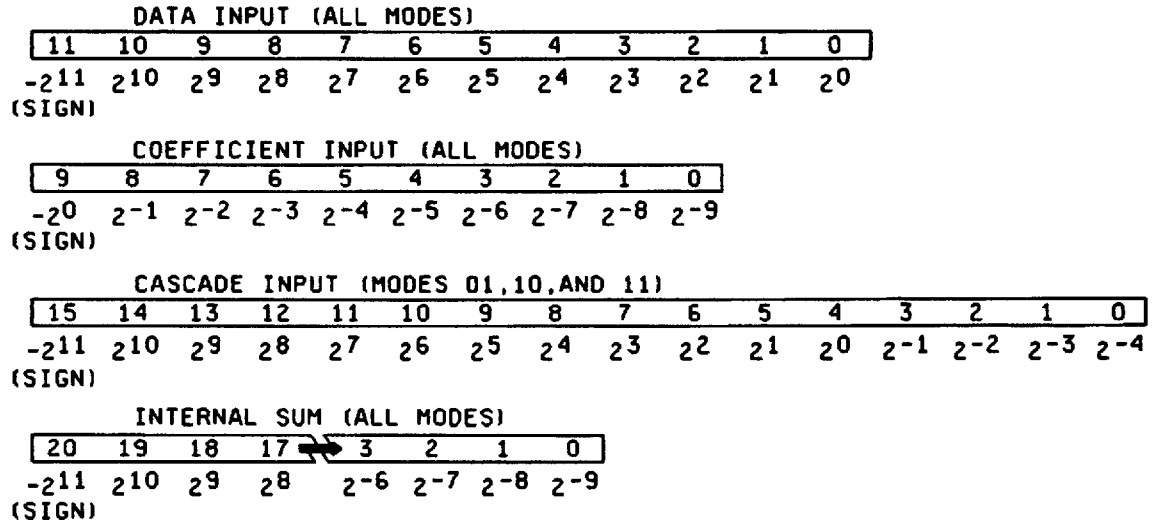


FIGURE 4. Format diagrams.

RESULT (MODES 00)

11	10	9	8	7	6	5	4	3	2	1	0
-2^{11} (SIGN)	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

CASCADE OUT (MODES 01,10,AND 11)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{11} (SIGN)	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}

FIGURE 4. Format diagrams - Continued.

-------- 3 x 3 Matrix Multiplier --- Mode 00 -------

X(n+4) = A(n)KA1(n) + B(n)KB1(n) + C(n)KC1(n)

Y(n+4) = A(n)KA2(n) + B(n)KB2(n) + C(n)KC2(n)

Z(n+4) = A(n)KA3(n) + B(n)KB3(n) + C(n)KC3(n)

-------- 9-Tap FIR Filter --- Mode 01 -------

CASOUT(n+12) = A(n+8)KA3(n+8) + A(n+7)KA2(n+7) + A(n+6)KA1(n+6)
+ B(n+5)KB3(n+8) + B(n+4)KB2(n+7) + B(n+3)KB1(n+6)
+ B(n+2)KC3(n+8) + B(n+1)KC2(n+7) + B(n)KC1(n+6)
+ CASIN(n+9)

-------- 3 x 3-Pixel Convolver --- Mode 10 -------

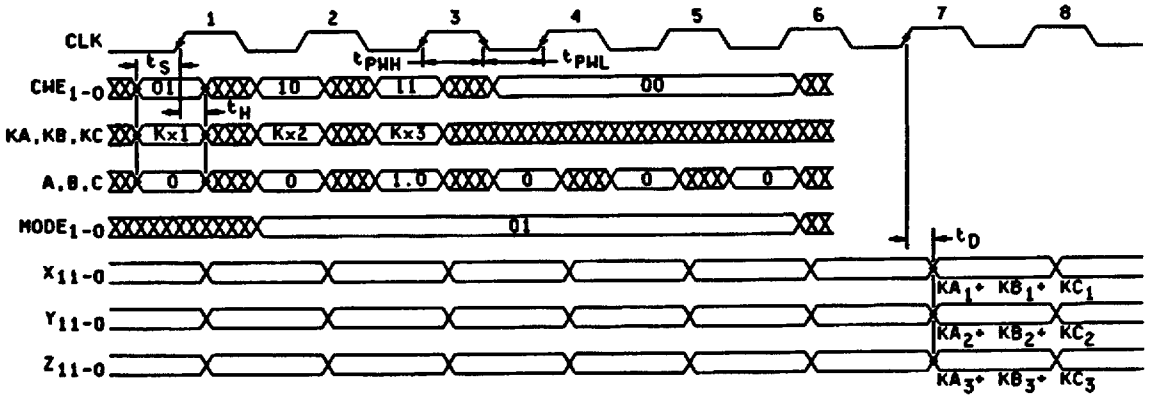
CASOUT(n+6) = A(n+2)KA3(n+2) + A(n+1)KA2(n+1) + A(n)KA1(n)
+ B(n+2)KB3(n+2) + B(n+1)KB2(n+1) + B(n)KB1(n)
+ C(n+2)KC3(n+2) + C(n+1)KC2(n+1) + C(n)KC1(n)
+ CASIN(n+3)

-------- 4 x 2-Pixel Convolver --- Mode 11 -------

CASOUT(n+7) = A(n+3)KA3(n+3) + A(n+2)KA2(n+2) + A(n+1)KA1(n+1)
+ A(n)KC3(n+3) + B(n+3)KB3(n+3) + B(n+2)KB2(n+2)
+ B(n+1)KB1(n+1) + B(n)KC1(n+1)
+ CASIN(n+4)

FIGURE 5. Latency equations.

3 x 3 Matrix multiplier (mode 00)



9-Tap FIR filter (mode 01)

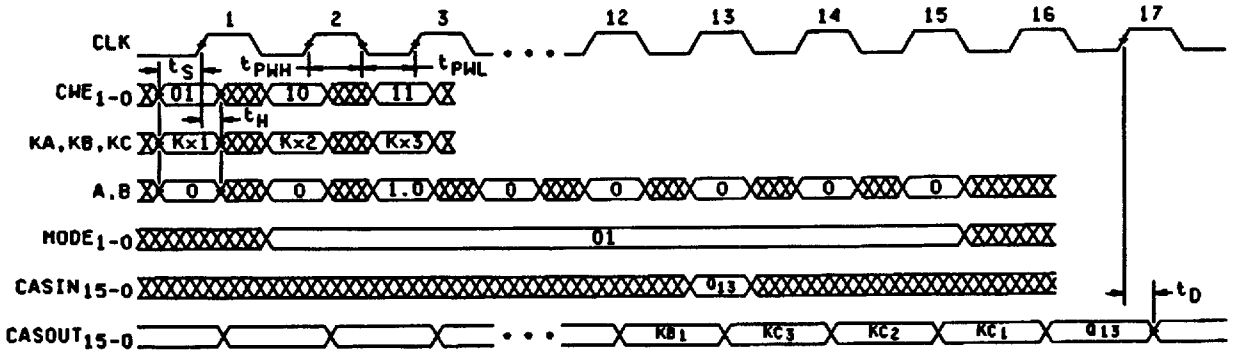


FIGURE 6. Switching waveforms.

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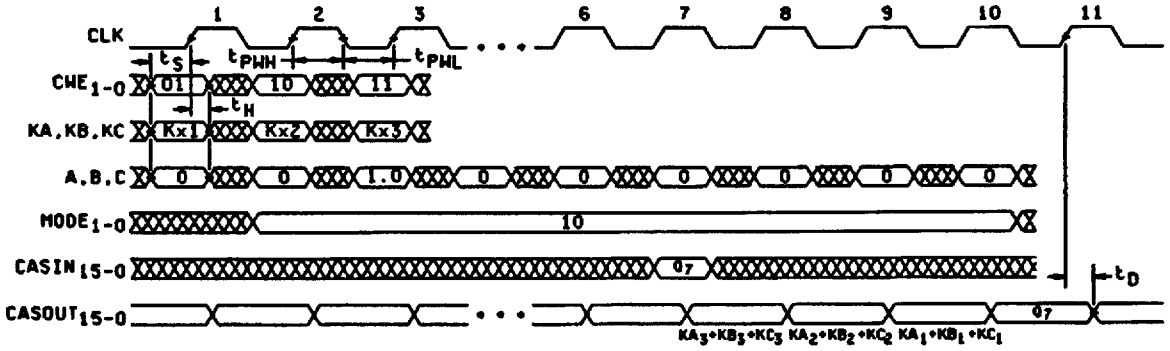
3 x 3-Pixel convolver (mode 10)



4 x 2-Pixel convolver (mode 11)

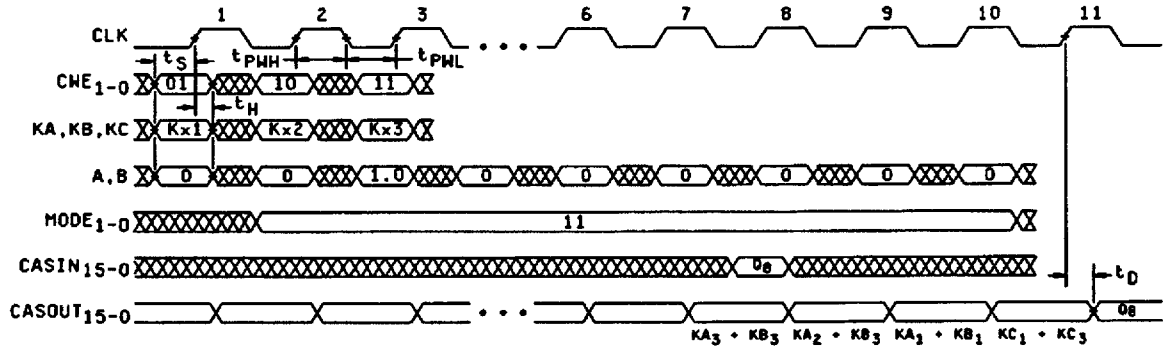


FIGURE 6. Switching waveforms - Continued.

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4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4 (C_{IN}, C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)		1,7,9	1,7,9
Final electrical parameters (see 4.2)	1,2,3,7,8,9,10,11 1/	1,2,3,7,8,9,10,11 1/	1,2,3,7,8,9,10,11 2/
Group A test requirements (see 4.4)	1,2,3,4,7,8,9,10,11	1,2,3,4,7,8,9,10,11	1,2,3,4,7,8,9,10,11
Group C end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9
Group D end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.