Octuple 6-bit DAC with I^{2}C-bus

TDA8444/AT/T

GENERAL DESCRIPTION

The TDA8444/AT/T comprises eight digital-to-analog converters (DSCs), each controlled via the two-wire I^{2}C-bus. The DACs are individually programmed using a 6-bit word to select an output from one of 64 voltage steps. The maximum output voltage of all DACs is set by the input V_{max} and the resolution is approximately $V_{max}/64$. At power-on all DAC outputs are set to their lowest value. The I^{2}C-bus slave receiver has a 7-bit address of which 3 bits are programmable via pins A0, A1 and A2.

FEATURES

- Eight discrete DACs
- I^{2}C-bus slave receiver
- 16-pin DIL package
  16-pin SO package
  20-pin SO package

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	Supply voltage		4.5	12.0	13.2	V
I_{CC}	Supply current	no loads; $V_{max} = V_P$; all data = 00	0	12	15	mA
P_{tot}	Total power dissipation	no loads; $V_{max} = V_P$; all data = 00	–	150	–	mW
V_{max}	Effective range of V_{max} input	$V_P = 12V$	1	–	10.5	V
V_O	DAC output voltage range		0.1	–	V_P–0.5	V
V_{LSB}	Step value of 1 LSB	$V_{max} = v_P$; $I_O = -2mA$	70	160	250	mV

PACKAGE OUTLINES

TDA8444   16-lead DIL; plastic (SOT38)
TDA8444T   16-lead SO; plastic (SOT-162)
TDA8444AT 20-lead SO; (SOT-163)
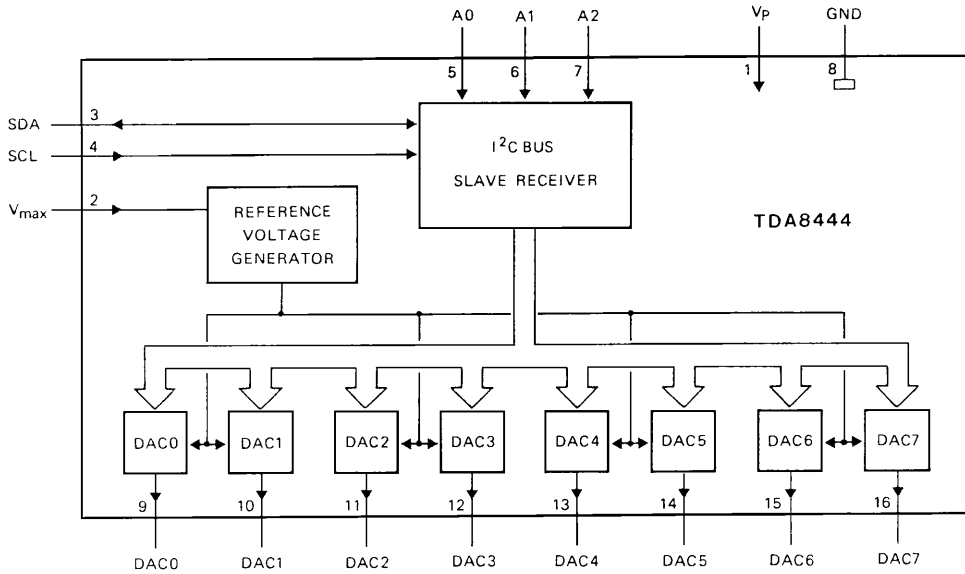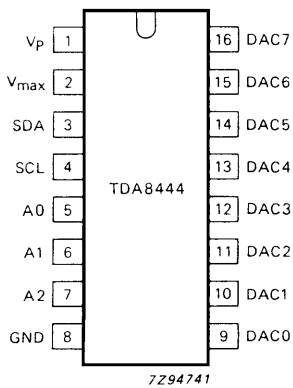
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Fig. 1 Block diagram.

PINNING

Fig. 2 Pinning diagram.

1	Vp	positive supply voltage
2	Vmax	control input for DAC maximum output voltage
3	SDA	I²C-bus serial data input/output
4	SCL	I²C-bus serial data clock
5	A0	programmable address bits for
6	A1	I²C-bus slave receiver
7	A2	
8	GND	ground
9-16	DAC0-7	analogue voltage outputs

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BLOCK DIAGRAM – TDA8444AT (SO-20)

					A0	A1	A2			V_P	GND

SDA — 3

SCL — 4

I²C-BUS SLAVE RECEIVER

TDA8444AT

V_{MAX} — 2

REFERENCE VOLTAGE GENERATOR

DAC0	DAC1	DAC2	DAC3	DAC4	DAC5	DAC6	DAC7
11	13	14	15	16	17	18	20
DAC0	DAC1	DAC2	DAC3	DAC4	DAC5	DAC6	DAC7
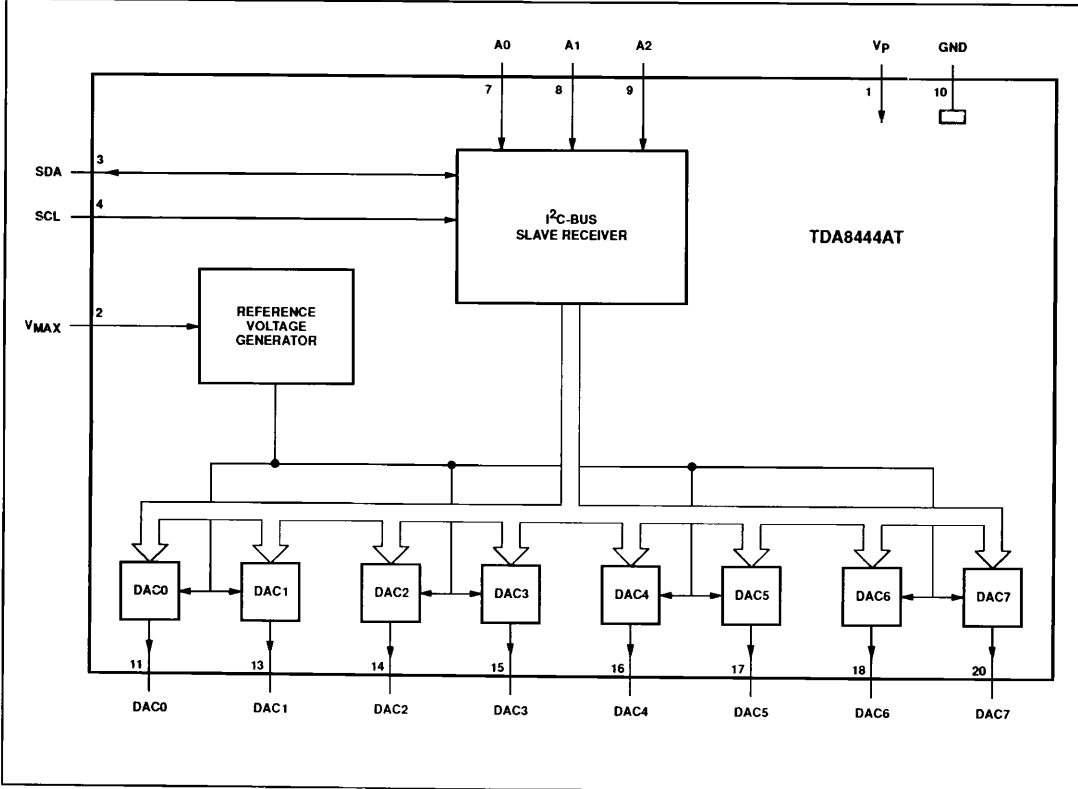
PIN CONFIGURATION AND DESCRIPTION – TDA8444AT (SO-20, SOT-163)

V_P	1		20	DAC7
V_{MAX}	2		19	NC
SDA	3		18	DAC6
SCL	4		17	DAC5
NC	5		16	DAC4
NC	6		15	DAC3
A0	7		14	DAC2
A1	8		13	DAC1
A2	9		12	NC
GND	10		11	DAC0

1	V_p	Positive supply voltage
2	V_{MAX}	Control input for DAC maximum output voltage
3	SDA	I²C bus serial data input/output
4	SCL	I²C bus serial data clock
7	A0	Programmable address bits for I²C bus slave receiver
8	A1	Programmable address bits for I²C bus slave receiver
9	A2	Programmable address bits for I²C bus slave receiver
10	GND	Ground
11, 13-18, 20	DAC0-7	Analog voltage outputs

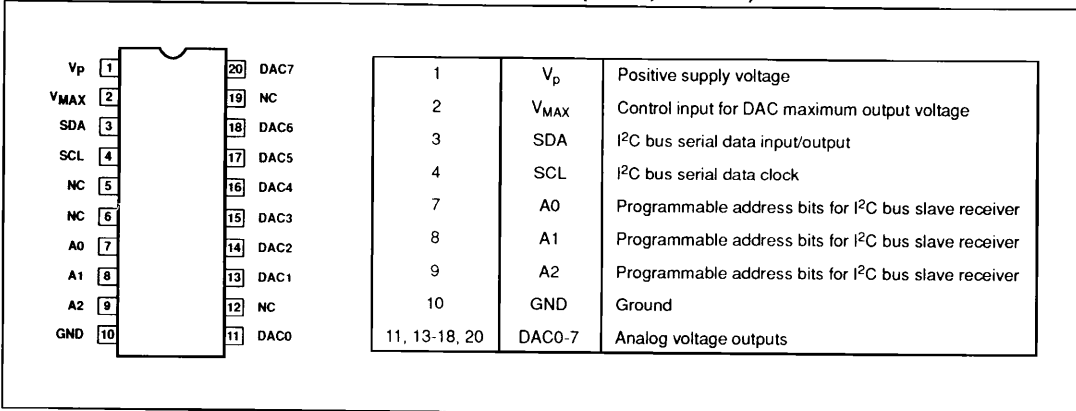# Octuple 6-bit DAC with I²C-bus   TDA8444/AT/T
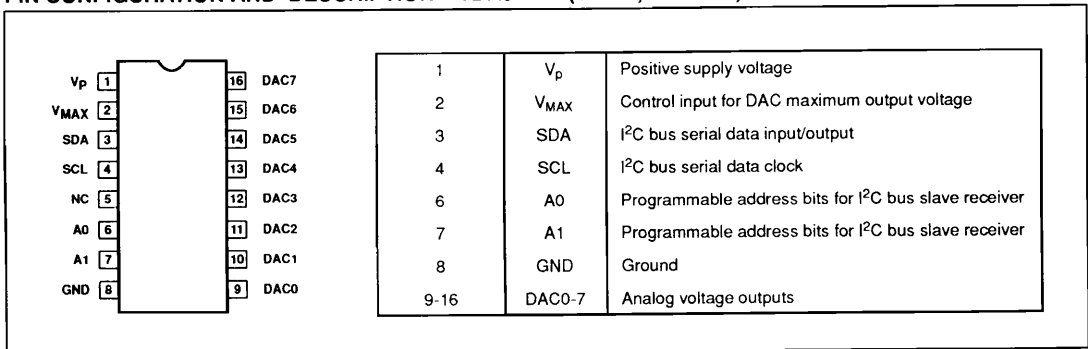
BLOCK DIAGRAM – TDA8444T (SO-16)

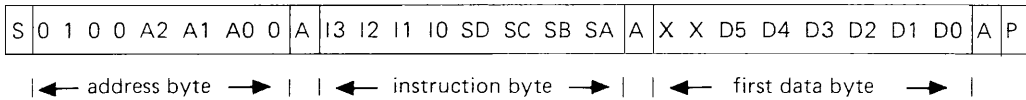## PIN CONFIGURATION AND DESCRIPTION – TDA8444T (SO-16, SOT-162)

1	V$_P$	Positive supply voltage
2	V$_{MAX}$	Control input for DAC maximum output voltage
3	SDA	I²C bus serial data input/output
4	SCL	I²C bus serial data clock
6	A0	Programmable address bits for I²C bus slave receiver
7	A1	Programmable address bits for I²C bus slave receiver
8	GND	Ground
9-16	DAC0-7	Analog voltage outputs

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FUNCTIONAL DESCRIPTION

I²C-bus

The TDA8444 I²C-bus interface is a receive-only slave. Data is accepted from the I²C-bus in the following format:

| S | 0 1 0 0 A2 A1 A0 0 | A | I3 I2 I1 I0 SD SC SB SA | A | X X D5 D4 D3 D2 D1 D0 | A | P |

|◀— address byte —▶| |◀— instruction byte —▶| |◀— first data byte —▶|

Where:

S	= start condition	A2, A1, A0	= programmable address bits
P	= stop condition	I3, I2, I1, I0	= instruction bits
A	= acknowledge	SD, SC, SB, SA	= subaddress bits
X	= don't care	D5, D4, D3, D2, D1, D0	= data bits

Fig. 3 Data format.

Address byte

Valid addresses are 40, 42, 44, 46, 48, 4A, 4C, 4E (hexadec), depending on the programming of bits A2, A1 and A0. With these addresses, up to eight TDA8444 ICs can be operated independently from one I²C-bus. No other addresses are acknowledged by the TDA8444.

Instruction and data bytes

Valid instructions are 00 to 0F and F0 to FF (hexadec); the TDA8444 will not respond to other instruction values.

Instructions 00 to 0F cause auto-incrementing of the subaddress (bits SD to SA) when more than one data byte is sent within one transmission. With auto-incrementing, the first data byte is written into the DAC addressed by bits SD to SA and then the subaddress is automatically incremented by one position for the next data byte in the series.

Auto-incrementation does not occur with instructions F0 to FF. Other than auto-incrementation there is no difference between instructions 00 to 0F and F0 to FF. When only one data byte per transmission is present, the DAC addressed by the subaddress will always receive the data.

Valid subaddresses (bits SD to SA) are 0 to 7 (hexadec) relating numerically to DAC0 to DAC7. When the auto-incrementing function is used, the subaddress will sequence through all possible values (0 to F, 0 to F, etc.).

I²C-bus

Input SCL (pin 3) and input/output SDA (pin 4) conform to I²C-bus specifications.* Pins 3 and 4 are protected against positive voltage pulses by internal zener diodes connected to the ground plane and therefore the normal bus line voltage should not exceed 5.5 V.

The address inputs A0, A1, A2 are programmed by a connection to GND for An = 0 or to Vp for An = 1. If the inputs are left floating, An = 1 will result.

Octuple 6-bit DAC with I²C-bus

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FUNCTIONAL DESCRIPTION (continued)

Input V_{max}

Input V_{max} (pin 2) provides a means of compressing the output voltage swing of the DACs. The maximum DAC output voltage is restricted to approximately V_{max} while the 6-bit resolution is maintained, so giving a finer voltage resolution of smaller output swings.

Digital-to-analogue converters

Each DAC comprises a 6-bit data latch, current switches and an output driver. Current sources with values weighted by 2^0 up to 2^5 are switched according to the data input so that the sum of the selected currents gives the required analogue voltage from the output driver. The range of the output voltage is approximately 0.5 to 10.5 V when $V_{max} = V_P$.

The DAC outputs are protected against short-circuits to V_P and GND.

To avoid the possibility of oscillations, capacitive loading at the DAC outputs should not exceed 2 nF.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		$V_P = V_1$	−0.5	18	V
Supply current (source)		$I_p = I_1$	−	−10	mA
		$I_P = I_l$	−	40	mA
I²C-bus line voltage		$V_{3,4}$	−0.5	5.9	V
Input voltage		V_l	−0.5	$V_P + 0.5$	V
Output voltage		V_O	−0.5	$V_P + 0.5$	V
Maximum current on any pin (except pins 1 and 8)		$\pm I_{max}$	−	10	mA
Total power dissipation		P_{tot}	−	500	mW
Operating ambient temperature range		T_{amb}	−20	+ 70	°C
Storage temperature range		T_{stg}	−65	+ 150	°C

THERMAL RESISTANCE

From junction to ambient

$R_{th\ j-a}$ 75 K/W

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CHARACTERISTICS

All voltages are with respect to GND; T_{amb} = 25 °C; V_P = 12 V unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	4.5	12.0	13.2	V
Voltage level for power-on reset		V_1	1	—	4.8	V
Supply current	no loads; $V_{max} = V_P$; all data = 00	$I_P = I_1$	8	12	15	mA
Total power dissipation	no loads; $V_{max} = V_P$; all data = 00	P_{tot}	—	150	—	mW
Effective range of V_{max} input (pin 2)	V_P = 12 V	$V_{max} = V_2$	1.0	—	10.5	V
Pin 2 current	V_2 = 1 V	I_2	—	—	−10	μA
	$V_2 = V_P$	I_2	—	—	10	μA
SDA, SCL inputs (pins 3 and 4)						
Input voltage range		V_I	0	—	5.5	V
Input voltage LOW		V_{IL}	—	—	1.5	V
Input voltage HIGH		V_{IH}	3.0	—	—	V
Input current LOW	$V_{3;4}$ = 0.3 V	I_{IL}	—	—	−10	μA
Input current HIGH	$V_{3;4}$ = 6 V	I_{IH}	—	—	±10	μA
SDA output (pin 3)						
Output voltage LOW	I_3 = 3 mA	V_{OL}	—	—	0.4	V
Sink current		I_O	3	8	—	mA
Address inputs (pins 5 to 7)						
Input voltage range		V_I	0	—	V_P	V
Input voltage LOW		V_{IL}	—	—	1	V
Input voltage HIGH		V_{IH}	2.1	—	—	V
Input current LOW		I_{IL}	—	−7	−12	μA
Input current HIGH		I_{IH}	—	—	1	μA

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CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
DAC outputs (pins 9 to 16)						
Output voltage range		V_O	0.1	–	V_P–0.5	V
Minimum output voltage	data = 00; I_O = –2 mA	V_{Omin}	0.1	0.4	0.8	V
Maximum output voltage	data = 3F; I_O = –2 mA					
at V_{max} = V_P		V_{Omax}	10	10.5	11.5	V
at $1 < V_{max} < 10.5$ V		V_{Omax}		see note		V
Output sink current	V = V_P; data = 1F	I_O	2	8	15	mA
Output source current	V = 0V; data = 1F	I_O	–2	–	–6	mA
Output impedance	data = 1F; $-2 < I_O < +2$ mA	Z_O	–	4	50	Ω
Step value of 1 LSB	V_{max} = V_P; I_O = –2 mA	V_{LSB}	70	160	250	mV
Deviation from linearity	I_O = –2 mA; N ≠ 32		0	–	50	mV
Deviation from linearity	I_O = –2 mA; N = 32		0	–	70	mV

Note to the characteristics

$V_O = 0.95 \, V_{max} + V_{Omin}$.

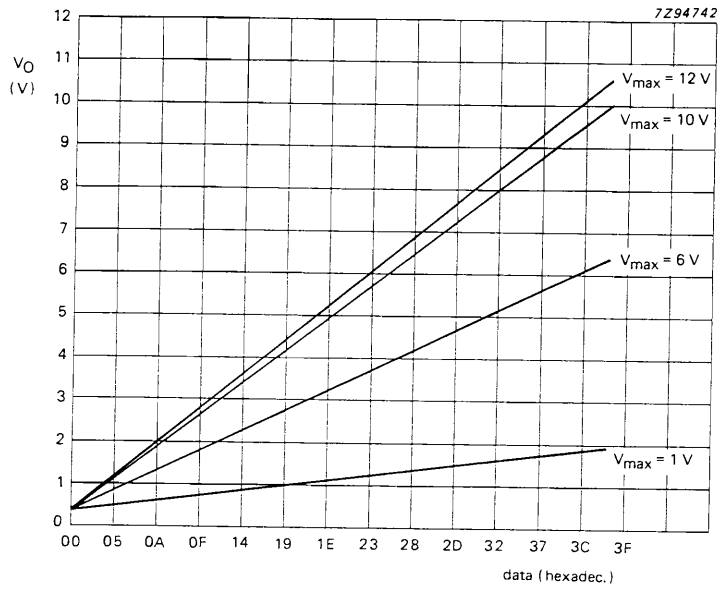## Octuple 6-bit DAC with I²C-bus

APPLICATION INFORMATION

Fig. 4 Graph showing output voltage as a function of the input data value for V_{max} values of 1, 6, 10 and 12 V; V_P = 12 V.