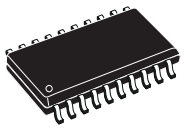
TDA7410ND

Signal processor for car radio applications

Features

- Device Includes Audio Processor, Stereo Decoder And Noiseblanker
- No External Components Required
- Fully Programmable Via I^2C Bus
- Softstep Volume and Bass
- Low Distortion
- Low Noise
- SO20 Package



SO20

Description

TDA7410ND is a signal processor specifically designed for car radio applications. The device includes a complete audioprocessor and a stereo decoder with noiseblanker, stereoblend and all signal processing functions for car radio system.

Switched-capacitors design technique allows the users to enjoy these features without external components or adjustments. This means higher quality and reliability as well as overall cost saving.

The device is fully programmable by I^2C bus interface allowing customization of key device parameters, especially filter characteristics..

Table 1. Device summary

Part number	Package	Packing
TDA7410ND	SO20	Tube
TDA7410NDTR	SO20	Tape and reel

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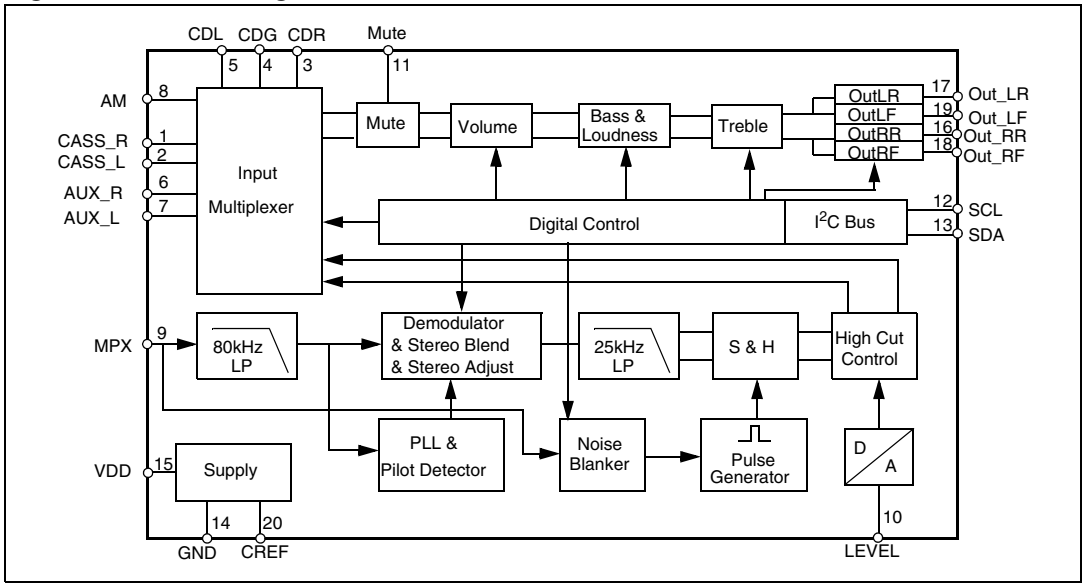
1 Block diagram

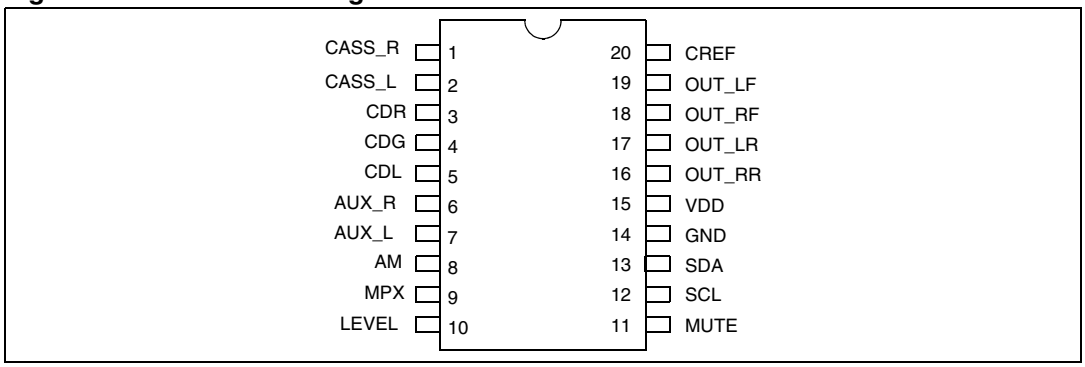
Figure 1. Block diagram



2 Pins description and connection diagram

2.1 Connection diagram

Figure 2. Connection diagram



2.2 Pin description

Table 2. Pins list

N°	Pin #	Function	Type
1	CASS_R	Cassette Input Right	I
2	CASS_L	Cassette Input Left	I
3	CDR	CD Right Channel Input	I
4	CDG	Ground reference CD	I
5	CDL	CD Left Channel Input	I
6	AUX_R	Aux Input Right	I
7	AUX_L	Aux Input Left Channel	I
8	AM	AM input	I
9	MPX	FM Input (MPX)	I
10	LEVEL	Level Input Stereodecoder	I
11	MUTE	Mute	I
12	SCL	I^2C Clock Line	I
13	SDA	I^2C Data Line	I/O
14	GND	Supply Ground	S
15	VDD	Supply Voltage	S
16	OUT_RR	Right Rear Speaker Output	O
17	OUT_LR	Left Rear Speaker Output	O
18	OUT_RF	Right Front Speaker Output	O
19	OUT_LF	Left Front Speaker Output	O
20	CREF	Reference Capacitor Pin	O

Pin Type:

I = input

O = Output

I/O = Input/Output

S = Supply

3 Audio Processor Part

Input Multiplexer

- Quasi-differential CD
- Cassette stereo and Aux stereo input
- AM mono and MPX
- Input gain stage with auto zero function

Volume Control

- 1dB attenuator
- Max. gain 32dB
- Max. attenuation 79dB
- Softstep function

Treble

- 2nd order frequency response
- Fixed center frequency 12.5kHz
- 7x2dB steps

Bass Control

- 2nd order frequency response
- Fixed center frequency 100Hz
- DC gain programmable
- 7x 2dB steps
- Softstep function

Speaker control

- 4 independent speaker controls (control range 50dB)
- Speaker mute

Mute functions

- Direct mute
- Mute by I^2C

4 Electrical Specification

4.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$R_{th\text{-}j\ pins}$	Thermal resistance junction-pins	85	°C/W
V_S	Operating supply voltage	10.5	V
T_{amb}	Operating ambient temperature	-40 to 85	°C
T_{stg}	Storage temperature range	-55 to 150	°C
V_{ESD}	ESD protection (Human Body Model)	±2000	V
V_{ESD}	ESD protection (Machine Model)	±200	V
V_{ESD}	ESD protection (Change Device Model)	±750	V

4.2 Supply

Table 4. Supply

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{DD}	Supply voltage		7.5	8.5	10	V
I_{DD}	Supply current	V_{DD} = 8.5V	15	20	25	mA

4.3 Electrical characteristics

Table 5. Electrical characteristics

V_S = 8.5V; T_{amb}= 25°C; R_L= 10kΩ; all gains = 0dB; f = 1kHz; unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Input selector						
R_{in}	Input resistance	All single ended inputs	70	100	130	kΩ
V_{CL}	Clipping level	CASS, CD, AUX input		2		V_{RMS}
		AM, MPX input		1.4		V_{RMS}
G_{IN_MIN}	Min. input gain			0		dB
G_{IN_MAX}	Max. input gain			15		dB
G_{STEP}	Step resolution			1		dB
Differential stereo inputs						
R_{in}	Input resistance	Differential	70	100	130	kΩ
CMRR	Common mode rejection ratio	V_{CM}=1 V_{RMS}@ 1kHz	40	50		dB
Volume control						

Table 5. Electrical characteristics (continued)

V_S = 8.5V; T_{amb}= 25°C; R_L= 10kΩ; all gains = 0dB; f = 1kHz; unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
G_{MAX}	Max gain			32		dB
A_{MAX}	Max attenuation		-83	-79	-75	dB
A_{STEP}	Step resolution		-0.5	1	1.5	dB
E_A	Attenuation set error	G = -20 to +15dB		0		dB
		G = -79 to -20dB	-4	0	3	dB
E_T	Tracking error				2	dB
V_{DC}	DC steps	Adjacent attenuation steps		0.1	3	mV
		From 0dB to G_{MIN}		0.5	5	mV
Bass control						
Fc	Center frequency	f_C	90	100	110	Hz
		Q	1.3	1.5	1.7	
C_{RANGE}	Control range		±13	±14	±15	dB
A_{STEP}	Step resolution		1	2	3	dB
DC_{GAIN}	Bass-DC-gain	DC = off	-1	0	1	dB
		DC = on	3.5	4.4	5.5	dB
Treble control						
C_{RANGE}	Clipping level		±13	±14	±15	dB
A_{STEP}	Step resolution		1	2	3	dB
fc	Center frequency	f_{C1}	10	12.5	15	kHz
Speaker attenuators						
A_{MAX}	Max Attenuation		-53	-50	-47	dB
A_{STEP}	Step Resolution		0.5	1	2	dB
Audio outputs						
V_{CL}	Clipping level	d = 0.3%	1.8	2		V_{RMS}
R_{OUT}	Output impedance			30	100	Ω
R_L	Output load resistance		2			kΩ
C_L	Output load capacitor				10	nF
V_{DC}	DC voltage level			4.0		V
General						
e_{NO}	Output noise	BW=20Hz to 20 kHz all gain = 0dB		15	25	μV
S/N	Signal to noise ratio	all gain = 0dB flat; Vo=2V_{RMS}		100		dB
D	Distortion	VIN=1V_{RMS}; all stages 0dB		0.01	0.3	%
S_C	Channel separation left/right		80	90		dB

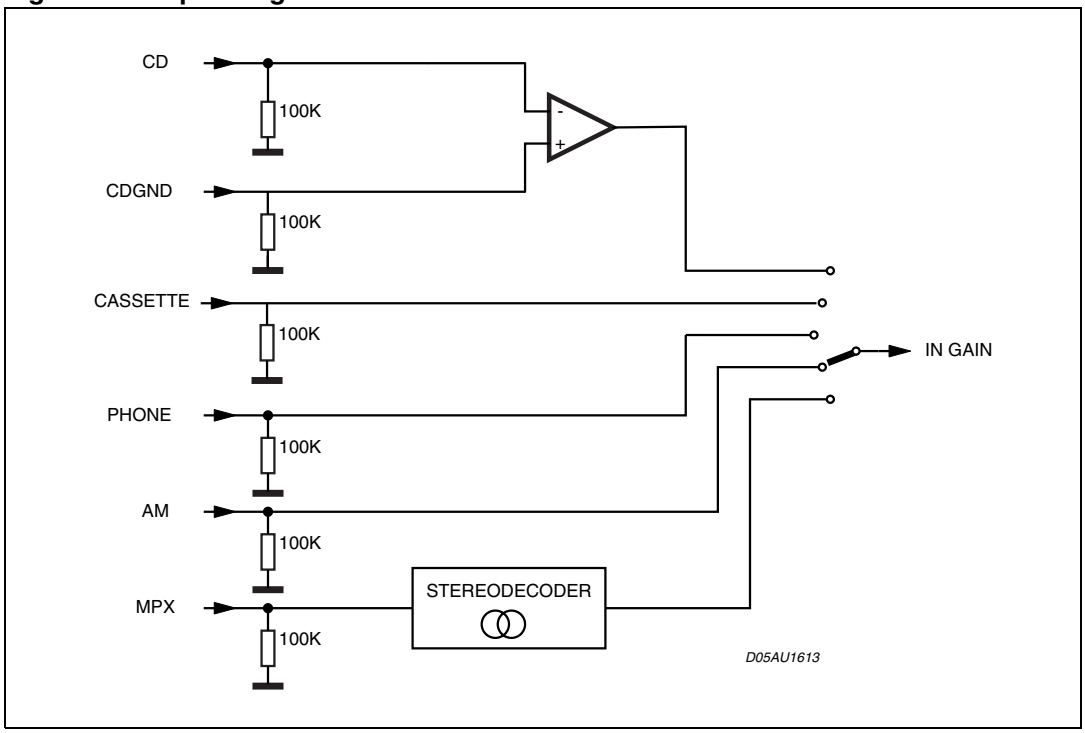
5 Description of the audioprocessor part

5.1 Input matrix

The input matrix of the TDA7410ND offers several possibilities to adapt the audioprocessor to the desired application (see *Figure 1*). Into the standard application we have:

- CD quasi differential
- Cassette stereo
- Phone
- AM mono
- Stereodecoder input

Figure 3. Input Stage



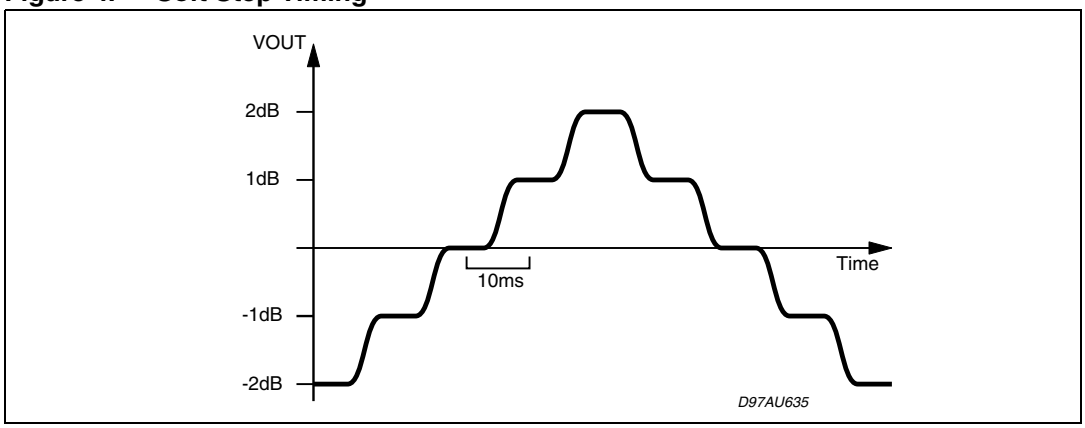
5.2 AutoZero

In order to reduce the number of pins there is no AC coupling between the In-Gain and the following stage, so that any offset generated by or before the In-Gain stage would be transferred or even amplified to the output. To avoid that effect a special offset cancellation stage called AutoZero is implemented. To avoid audible clicks the audioprocessor is muted before the volume stage during this time. In some cases, for example if the P is executing a refresh cycle of the I2C bus programming, it is not useful to start a new AutoZero action because no new source is selected and an undesired mute would appear at the outputs. For such applications the TDA7410D could be switched in the "Auto Zero Remain" mode (Bit 6 of the subaddress byte). If this bit is set to high, the DATABYTE 0 could be loaded without invoking the AutoZero and the old adjustment value remains.

5.3 Softstep Volume

When volume level is changed often an audible click appears at the output. The root cause of those clicks could be either a DC offset before the volume stage or the sudden change of the envelope of the audio signal. With the Softstep feature both kinds of clicks could be reduced to a minimum and are no more audible (see *Figure 4*).

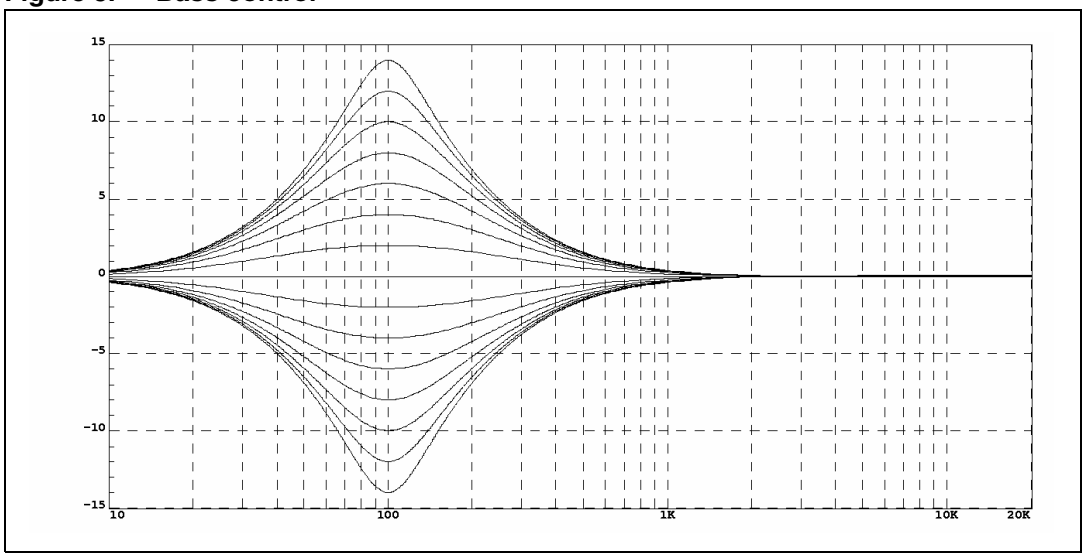
Figure 4. Soft Step Timing



5.4 Bass

The attenuation is programmable in the bass stage (see *Figure 5*):

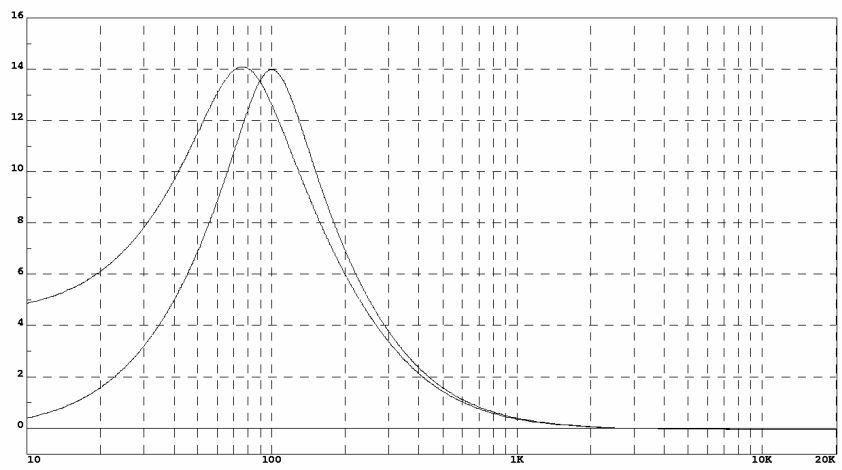
Figure 5. Bass control



5.5 DC Mode

In this mode the DC gain is increased by 4.4dB. In addition the programmed center frequency and quality factor is decreased by 25% which can be used to reach alternative center frequencies or quality factors. (see *Figure 6*):

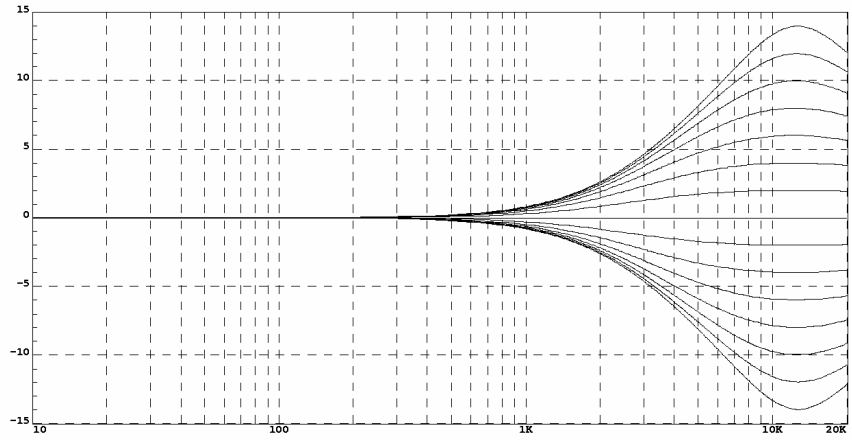
Figure 6. Bass normal and DC mode



5.6 Treble

The attenuation is programmable in the treble stage (see *Figure 7*):

Figure 7. Treble Control



5.7 Speaker Attenuator

Due to practical aspects the steps in the speaker attenuators are not linear over the full range. At attenuations more than 24dB the steps increase from 2dB to 8dB (please see data byte specification).

5.8 Stereodecoder part

- No External components necessary
- PLL with adjustment fully integrated VCO
- Automatic pilot dependent MONO/STEREO switching
- Very high suppression of intermodulation and interference
- Highcut and Stereoblend characteristics programmable in a wide range
- Internal noiseblanker with threshold controls
- I^2C bus control of all necessary functions

Table 6. Stereodecoder electrical characteristics

V_{DD} = 8.5V, Deemphasis time const = 50µs, V_{MPX} = 500mV, In Gain = 6dB, 75kHz deviation, f = 1kHz, T_{amb} =25°C, unless otherwise spificied

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IN}	MPX input level	Input gain = 3.5dB		0.5		V_{RMS}
Rin	Input resistance			100		kΩ
Gain	Minimum input gain			3.5		dB
Gmax	Maximum input gain			11		dB
G_{STEP}	Step resolution			2.5		dB
a	Max. channel separation			40		dB
Mono/stereo switch						
V_{PTHST1}	Pilot threshold voltage	For stereo, PTH=1	10	15	25	mV
V_{PTHST0}		For stereo, PTH=0	15	25	35	mV
V_{PTHMO1}		For mono, PTH=1	7	12	17	mV
V_{PTHMO0}		For mono, PTH=0	10	19	25	mV
PLL						
Δf/f	Capture Range			0.5		%
Deemphass and highcut						
τHC50	Deemphasis time constant	Stereodecoder-Byte D5=0 V_{LEVEL} >> V_{HCH}		50		µs
τHC75		Stereodecoder-Byte D5=1 V_{LEVEL} >> V_{HCH}		75		µs
τHC50	Highcut time constant	Stereodecoder-Byte D5=0 V_{LEVEL} >> V_{HCH}		150		µs
τHC75		Stereodecoder-Byte D5=1 V_{LEVEL} >> V_{HCH}		225		µs

Table 6. Stereodecoder electrical characteristics (continued)
V_{DD} = 8.5V, Deemphasis time const = 50µs, V_{MPX} = 500mV, In Gain = 6dB, 75kHz deviation, f = 1kHz, T_{amb} =25°C, unless otherwise spificied

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Stereoblend and highcut control						
REF5V	Internal reference voltage			5		V
L_{Gmin}	Min. level gain			0		dB
L_{Gmax}	Max. level gain			10		dB
L_{Gstep}	Level gain step resolution			0.67		dB
VSBLmin	Min. voltage for mono			33		%REF5V
VSBLmax	Max. voltage for mono			58		%REF5V
VSBLstep	Step resolution			8.4		%REF5V
Groll	Roll off compensation			2.5		dB
VHCHmin	Min. voltage for no highcut			42		%REF5V
VHCHmax	Max. voltage for no highcut			66		%REF5V
VHCHstep	Step resolution			8.4		%REF5V
VHCLmin	Min. voltage for full highcut			17		%VHCH
VHCLmax	Max. voltage for full highcut			33		%VHCH
Carrier and harmonic suppression at the output						
α19	Pilot signal	f = 19kHz		40		dB
α39	Subcarrier	f = 38kHz		65		dB
α57	Subcarrier	f = 57kHz		55		dB
α76	Subcarrier	f = 76kHz		80		dB
ACI - Adjacent channel interference						
α114	Signal	f = 114kHz		80		dB
α190	Signal	f = 190kHz		70		dB

5.9 Noise blanker part

- Internal highpass filter
- Programmable trigger threshold
- Additional circuit for trigger adjustment (deviation, field-strength)
- Very low offset current during hold time
- Selectable pulse suppression times

Table 7. Noise blanker electrical characteristics

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
V_{TH}	Trigger threshold(1),(2)	means. with V_{PEAK}=0.9V	NBT=111		30		mV_{OP}
			NBT=110		35		mV_{OP}
			NBT=101		40		mV_{OP}
			NBT=100		45		mV_{OP}
			NBT=011		50		mV_{OP}
			NBT=010		55		mV_{OP}
			NBT=001		60		mV_{OP}
			NBT=000		65		mV_{OP}
$V_{TRNOISE}$	Noise controlled trigger threshold(3)	means. with V_{PEAK}=1.5V	NCT=00		260		mV_{OP}
			NCT=01		220		mV_{OP}
			NCT=10		180		mV_{OP}
			NCT=11		140		mV_{OP}
V_{RECT}	Rectifier voltage	V_{MPX} = 0mV			0.9		V
		V_{MPX} = 50mV; f = 150kHz			1.7		V
		V_{MPX} = 100mV; f = 150kHz			2.5		V
$V_{RECT\ DEV}$	deviation dependent rectifier voltage(4)	means. with V_{MPX}=800mV (75kHz dev.)	OVD=11		0.9(off)		V_{OP}
			OVD=10		1.2		V_{OP}
			OVD=01		2.0		V_{OP}
			OVD=00		2.8		V_{OP}
$V_{RECT\ FS}$	Fieldstrength Controlled Rectifier Voltage(5)	means. with V_{MPX}=0mV V_{LEVEL}<<V_{SBL} (fully mono)	FSC=11		0.9(off)		V
			FSC=10		1.3		V
			FSC=01		1.8		V
			FSC=00		2.3		V

1. All thresholds are measured using a pulse with T_R = 2 ms, T_{HIGH} = 2 ms and T_F = 10ms
2. NBT represents the Noiseblanker-Byte D2~D0 for the noise blanker trigger threshold
3. NAT represents the Noiseblanker-Byte D4~D3 for the noise controlled trigger adjustment
4. OVD represents the Noiseblanker-Byte D7~D6 for the over deviation detector
5. FSC represents the Fieldstrength-Byte D1~D0 for the fieldstrength control

Figure 8. Vn timing diagram

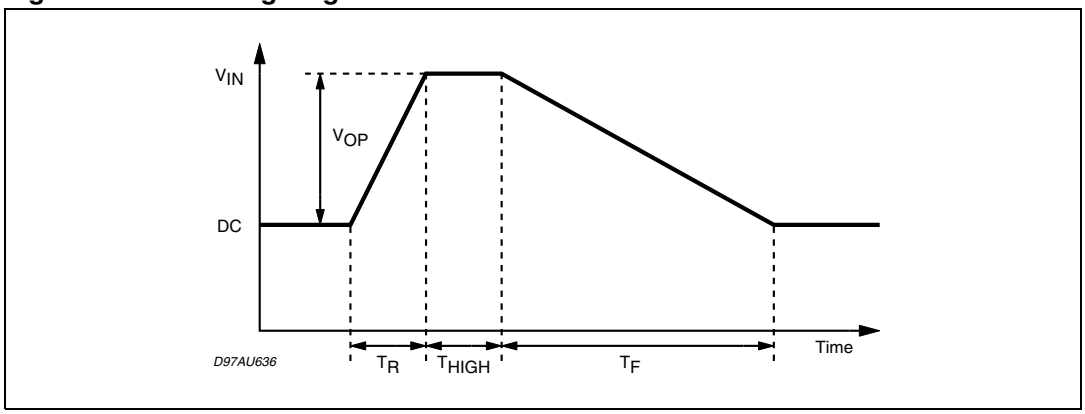


Figure 9. Trigger Threshold vs. V_{PEAK}

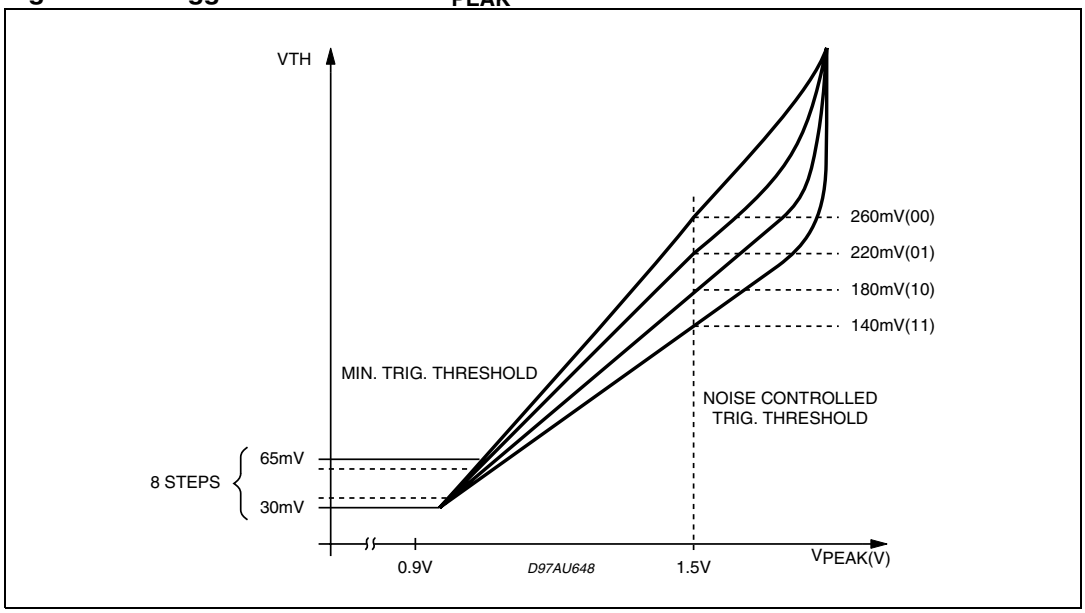


Figure 10. Deviation Controlled Trigger Adjustment

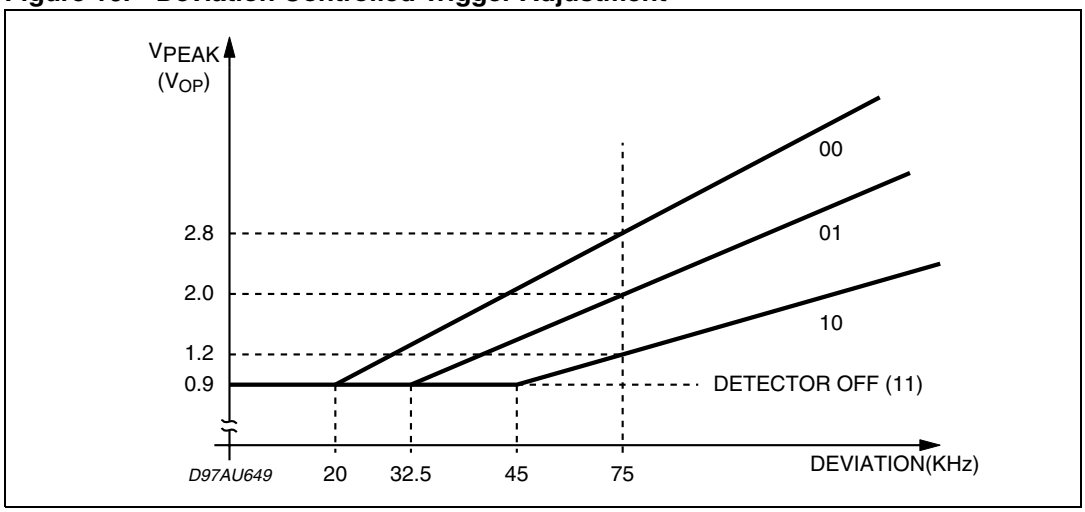
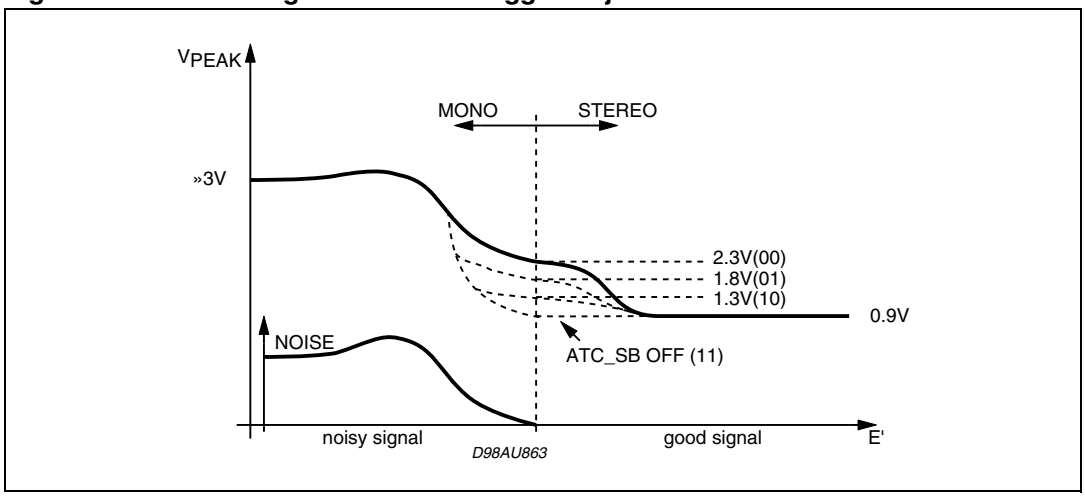


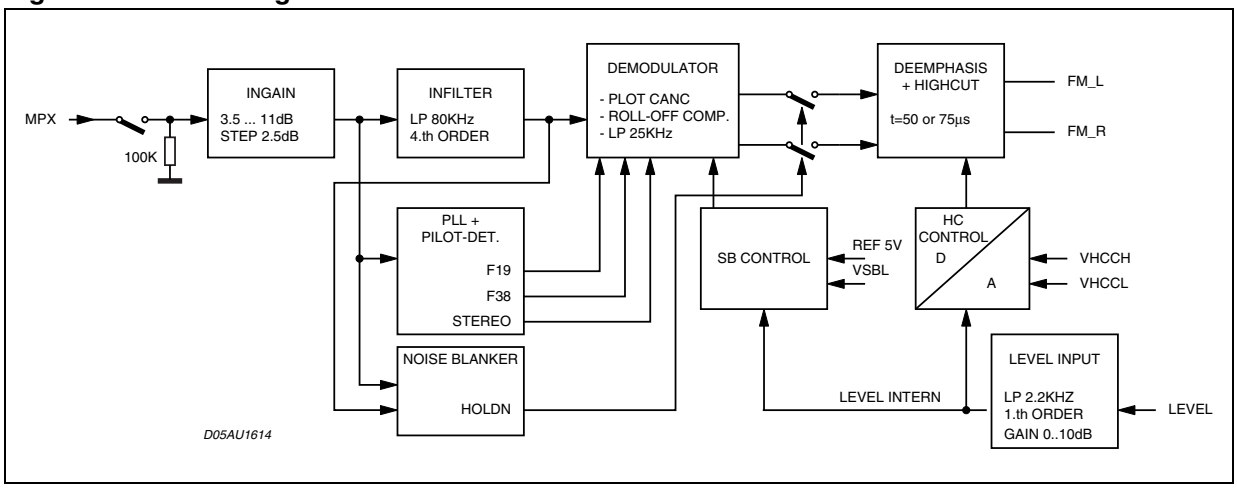
Figure 11. Fieldstrength Controlled Trigger Adjustment



6 Description of stereodecoder

The stereodecoder part of the TDA7410ND (see *Figure 12*) contains all functions necessary to demodulate the MPX signal like pilot tone dependent MONO/STEREO switching as well as "stereoblend" and "highcut" functions. Adaptations like programmable input gain, selectable deemphasis time constant and a programmable fieldstrength input allow to use different IF devices.

Figure 12. Block diagram of the stereodecoder



6.1 Input stages

The Ingain stage allows to adjust the MPX signal to a magnitude of about 1Vrms internally which is the recommended value. The 4th order input filter has a corner frequency of 80kHz and is used to attenuate spikes and noise and acts as an antialiasing filter for the following switch capacitor filters.

6.2 Demodulator

In the demodulator block the left and the right channel are separated from the MPX signal. In this stage also the 19kHz pilot tone is cancelled.

6.3 Deemphasis and highcut

The lowpass filter for the deemphasis allows to choose between a time constant of 50µs and 75µs (bit D5, Stereodecoder Adjustment byte).

The highcut control range will be in both cases $t_{HC} = 2 \cdot t_{Deemp}$. Inside the highcut control range (between VHCH and VHCL) the LEVEL signal is converted into a 5 bit word which controls the lowpass time constant between $t_{Deemp}...3 \cdot t_{Deemp}$. There by the resolution will remain always 5 bits independently of the absolute voltage range between the VHCH and VHCL values. The highcut function can be switched off by I2C bus (bit D7, Fieldstrength Control byte set to "0").

6.4 PLL and pilot tone detector

The PLL has the task to lock on the 19kHz pilotone during a stereo transmission to allow a correct demodulation. The included detector enables the demodulation if the pilot tone reaches the selected pilottone threshold VPTHST. Two different thresholds are available. The detector output (signal STEREO, see block diagram) can be checked by reading the status byte of the TDA7410ND via I^2C bus.

6.5 Fieldstrength control

The fieldstrength input is used to control the highcut and the stereoblend function. In addition the signal can be also used to control the noiseblanker thresholds.

6.6 LEVEL input and gain

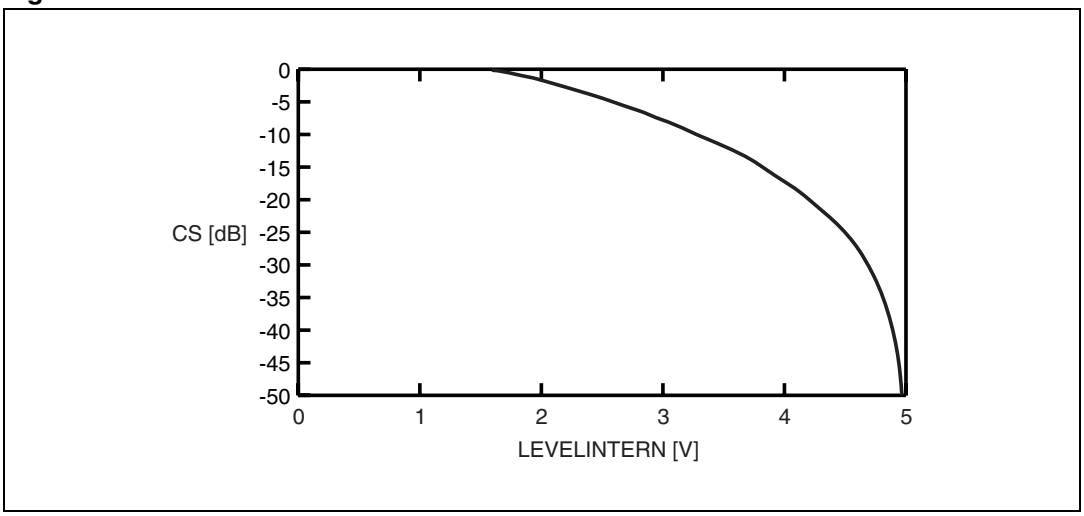
To suppress undesired high frequency modulation on the highcut and stereoblend function the LEVEL signal is lowpass filtered firstly. The filter is a combination of a 1^{st} order RC lowpass at 53kHz (working as anti-aliasing filter) and a 1^{st} order switched capacitor lowpass at 2.2kHz. The second stage is a programmable gain stage to adapt the LEVEL signal internally to different IF. The gain is widely programmable in 16 steps from 0dB to 10dB (step = 0.67dB).

6.7 Stereoblend control

The stereoblend control block converts the internal LEVEL voltage (LEVEL INTERN) into an demodulator

compatible analog signal which is used to control the channel separation between 0dB and the maximum separation. Internally this control range has a fixed upper limit which is the internal reference voltage REF5V. The lower limit can be programmed to be 33%, 42%, 50% or 58% of REF5V (see *Figure 13*, *14*).

Figure 13. Internal stereoblend characteristics

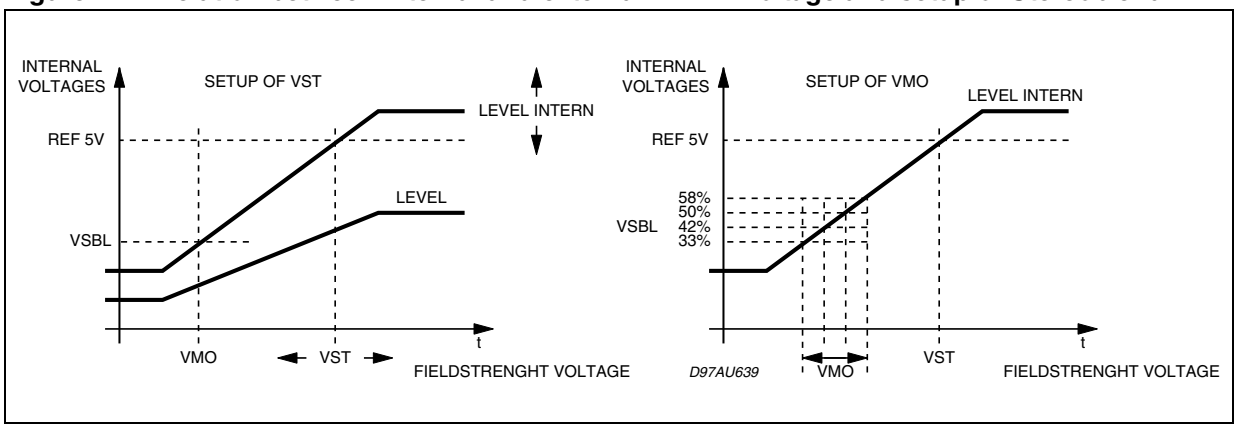


To adjust the external LEVEL voltage to the internal range two values must be defined: the LEVEL gain LG and VSBL. To adjust the voltage where the full channel separation is reached (VST) the LEVEL gain LG has to be defined. The following equation can be used to estimate the gain:

$$L_G = \frac{REF5V}{\text{Field strength voltage[STEREO]}}$$

The gain can be programmed through 4 bits in the "Level Gain" byte. The MONO voltage VMO (0dB channel separation) can be choosen selecting 33, 42, 50 or 58% of REF5V.

Figure 14. Relation between internal and external LEVEL voltage and setup of Stereoblend

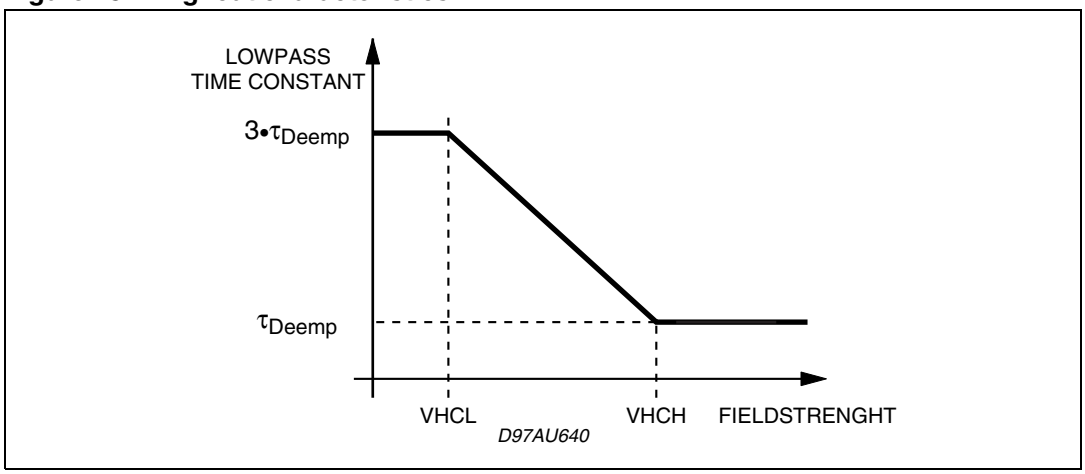


6.8 Highcut Control

The highcut control setup is similar to the stereoblend control setup : the starting point

VHCH can be set with 2 bits to be 42, 50, 58 or 66% of REF5V whereas the range can be set to be 17 or 33% of VHCH (see *Figure 15*).

Figure 15. Highcut characteristics



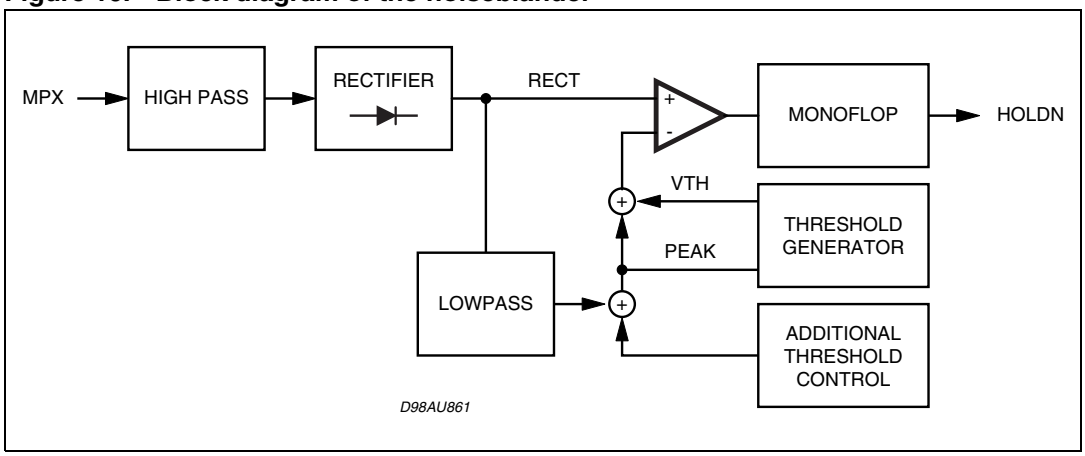
7 Functional description of the noiseblanker

In the automotive environment the MPX signal is disturbed by spikes produced by the ignition and for example the wiper motor. The aim of the noiseblanker part is to cancel the audible influence of the spikes. Therefore the output of the stereodecoder is held at the actual voltage for 40µs. In a first stage the spikes must be detected but to avoid a wrong triggering on high frequency (white) noise a complex trigger control is implemented. Behind the triggerstage a pulse former generates the "blanking" pulse. To avoid any crosstalk to the signal path the noiseblanker is supplied by its own biasing circuit.

7.1 Trigger path

The incoming MPX signal is highpass filtered, amplified and rectified. This second order highpass-filter has a corner frequency of 140kHz. The rectified signal, RECT, is lowpass filtered to generate a signal called PEAK. Also noise with a frequency 140kHz increases the PEAK voltage. The PEAK voltage is fed to a threshold generator, which adds to the PEAK voltage a DC dependent threshold VTH. Both signals, RECT and PEAK+VTH are fed to a comparator which triggers a re-triggerable monoflop. The monoflop's output activates the sample-and-hold circuits in the signalpath for 40µs. The block diagram of the noiseblanker is given in *Figure 16*.

Figure 16. Block diagram of the noiseblander



7.2 Automatic noise controlled threshold adjustment (ATC)

There are mainly two independent possibilities for programming the trigger threshold:

a) the low threshold in 8 steps (bits D0 to D2 of the noiseblanker byte)

b) the noise adjusted threshold in 4 steps (bits D3 and D4 of the noiseblanker byte, (see *Figure 9*).

The low threshold is active in combination with a good MPX signal without any noise; the PEAK voltage is less than 1V. The sensitivity in this operation is high. If the MPX signal is noisy the PEAK voltage increases

due to the higher noise, which is also rectified. With increasing of the PEAK voltage the trigger threshold increases, too. This particular gain is programmable in 4 steps (see *Figure 9*).

7.3 Automatic threshold control

Besides the noise controlled threshold adjustment there is an additional possibility for influencing the trigger threshold. It is depending on the stereoblend control. The point where the MPX signal starts to become noisy is fixed by the RF part. Therefore also the starting point of the normal noise-controlled trigger adjustment is fixed (*Figure 11*). In some cases the behaviour of the noiseblanker can be improved by increasing the threshold even in a region of higher fieldstrength. Sometimes a wrong triggering occures for the MPX signal often shows distortion in this range which can be avoided even if using a low threshold. Because of the overlap of this range and the range of the stereo/mono transition it can be controlled by stereoblend. This threshold increase is programmable in 3 steps or switched off with bits D0 and D1 of the fieldstrength control byte.

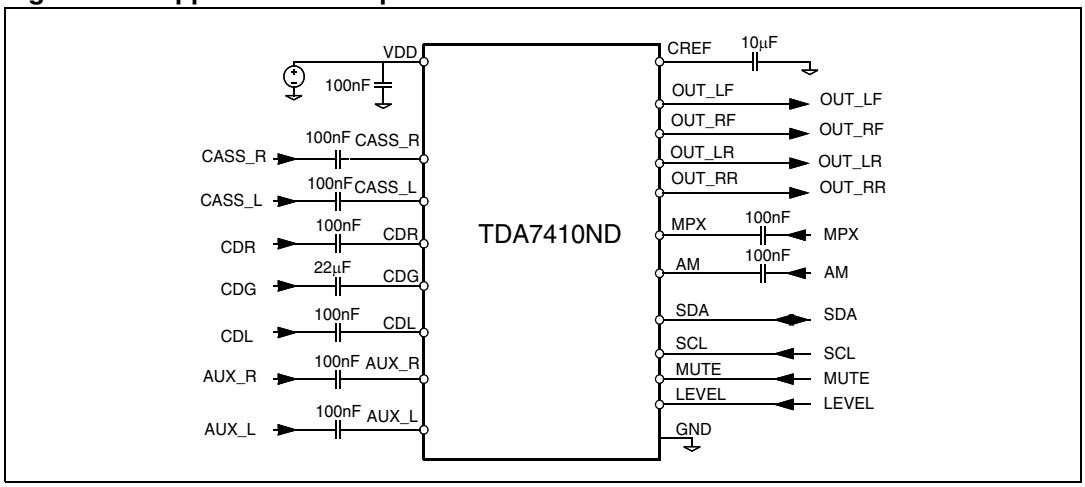
7.4 Over deviation detector

If the system is tuned to stations with a high deviation the noiseblanker can trigger on the higher frequencies of the modulation. To avoid this wrong behaviour, which causes noise in the output signal, the noiseblanker offers a deviation dependent threshold adjustment. By rectifying the MPX signal a further signal representing the actual deviation is obtained. It is used to increase the PEAK voltage. Offset and gain of this circuit are programmable in 3 steps with the bits D6 and D7 of the stereodecoder byte (the first step turns off the detector, see *Figure 10*).

7.5 Test Mode

During the test mode which can be activated by setting bit D0 of the testing byte and bit D5 of the subaddress byte to ”1” several internal signals are available at the CASSR pin. During this mode the input resistance of 100kOhm is disconnected from the pin. The internal signals available are shown in the software specification.

Figure 17. Application Example



8 I²C bus specification

8.1 Interface protocol

The interface protocol comprises:

- a start condition (S)
- a chip address byte (the LSB determines read/write transmission)
- a subaddress byte
- a sequence of data (N-bytes + acknowledge)
- a stop condition (P)
- the max. clock speed is 500kbits/s

Table 8. Receive mode

S	1	0	0	0	1	1	0	R/W	ACK	X	AZ	TS	AI	A3	A2	A1	A0	ACK	DATA	ACK	P

S = Start

R/W = "0" -> Receive Mode (Chip could be programmed by μP)

"1" -> Transmission Mode (Data could be received by μP)

ACK = Acknowledge

P = Stop

TS = Testing mode

AZ = Auto zero remain

AI = Auto increment

Table 9. Transmission mode

S	1	0	0	0	1	0	0	R/W	ACK	X	X	X	X	ST	X	X	X	ACK	P

ST = Stereo

X = Not Used

The transmitted data is automatic updated after each ACK. Transmission can be repeated without new chip address.

8.2 Reset condition

A Power-On-Reset is invoked if the Supply-Voltage is below than 3.5V. After that the following data is written automatically into the registers of all subaddresses:

Table 10. Reset condition

MSB							LSB
1	1	1	1	1	1	1	0

Table 11. Subaddress (Receive mode)

MSB							LSB	Function
X	AZ	TS	AI	A3	A2	A1	A0	
	0 1							**AZ Remain** Off On
		0 1						**Test Mode** Off On
			0 1					**Auto Increment** Off On
				0 0 0 0 0 0 0 0 1 1 1 1 1	0 0 0 0 1 1 1 1 0 0 0 0 1	0 0 1 1 0 0 1 1 0 0 1 1 0	0 1 0 1 0 1 0 1 0 1 0 1 0	Source Selector Volume Control Speaker Attenuator LF Speaker Attenuator LR Speaker Attenuator RF Speaker Attenuator RR Treble / Level Gain Stereodecoder Adjustment Noiseblanker Adjustment Fieldstrength Control Test Bass Softstep Configuration

Table 12. Source selector (0)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	Source Selector / Bass
								Source Selector
					0	0	0	CD
					0	0	1	Cassette
					0	1	0	Aux
					0	1	1	AM
					1	0	0	Stereo Decoder
					1	0	1	Mute
					1	1	0	Not Used
					1	1	1	Not Used
								Input Gain
	0	0	0	0				0dB
	0	0	0	1				1dB
	:	:	:	:				:
	1	1	1	0				14dB
	1	1	1	1				15dB
x								Not Used

Table 13. Volume Control (1)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Gain/Attenuation
	0	0	0	0	0	0	0	+0dB
	0	0	0	0	0	0	1	+1dB
	:	:	:	:	:	:	:	:
	0	0	1	1	1	1	1	+31dB
	0	1	0	0	0	0	0	-0dB
	0	1	0	0	0	0	1	-1dB
	:	:	:	:	:	:	:	:
	1	1	0	1	1	1	0	-78dB
	1	1	0	1	1	1	1	-79dB
	1	1	1	x	x	x	x	mute
								Soft Step
0								on
1								off

Table 14. Speaker attenuation (2, 3, 4, 5)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	Speaker Attenuation LF (LR,RF,RR)
								Attenuation
		0	0	0	0	0	0	0dB
		0	0	0	0	0	1	-1dB
		:	:	:	:	:	:	:
		0	1	0	1	1	1	-23dB
		0	1	1	0	0	0	-25dB
		0	1	1	0	0	1	-27dB
		0	1	1	0	1	0	-29dB
		0	1	1	0	1	1	-31.5dB
		0	1	1	1	0	0	-34dB
		0	1	1	1	0	1	-37.5dB
		0	1	1	1	1	0	-42dB
		0	1	1	1	1	1	-50dB
		1	x	x	x	x	x	Speaker Mute
x	x							**Not used**

Table 15. Treble / Level gain (6)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	Treble / Level Gain
								Treble
				0	0	0	0	-14dB
				0	0	0	1	-12dB
				:	:	:	:	:
				0	1	1	0	-2dB
				0	1	1	1	0dB
				1	1	1	1	0dB
				1	1	1	0	+2dB
				:	:	:	:	:
				1	0	0	1	+12dB
				1	0	0	0	+14dB
								LEVEL Gain
0	0	0	0					0dB
0	0	0	1					0.66dB
0	0	1	0					1.33dB
:	:	:	:					:
1	1	1	1					10dB

Table 16. Stereodecoder adjustment (7)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	Stereodecoder Adjustment
							0 1	STD Unmuted STD Muted
					0 0 1 1	0 1 0 1		In-Gain 11dB In-Gain 8.5dB In-Gain 6dB In-Gain 3.5dB
				0 1				**Forced MONO** MONO/STEREO switch automatically
			0 1					Pilot Threshold HIGH Pilot Threshold LOW
		0 1						Deemphasis Threshold 50µs Deemphasis Threshold 75µs
0 0 1 1	0 1 0 1							**Blank Time Adj** 38µs 25.5µs 32µs 22µs

Table 17. Noise blanker adjustment (8)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	Noiseblanker
					0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1	Low Threshold 65mV Low Threshold 60mV Low Threshold 55mV Low Threshold 50mV Low Threshold 45mV Low Threshold 40mV Low Threshold 35mV Low Threshold 30mV
			0 0 1 1	0 1 0 1				Noise Controlled Threshold 260mV Noise Controlled Threshold 220mV Noise Controlled Threshold 180mV Noise Controlled Threshold 140mV
		0 1						Noise Blanker OFF Noise Blanker ON
0 0 1 1	0 1 0 1							Over deviation Adjust 2.8V Over deviation Adjust 2.0V Over deviation Adjust 1.2V Over deviation Adjust OFF

Table 18. Fieldstrength Control (9)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	Fieldstrength Control
						0	0	NoiseBlanker Field strength Adj 2.3V
						0	1	NoiseBlanker Field strength Adj 1.8V
						1	0	NoiseBlanker Field strength Adj 1.3V
						1	1	NoiseBlanker Field strength Adj OFF
				0	0			VSBL at 33% REF 5V
				0	1			VSBL at 42% REF 5V
				1	0			VSBL at 50% REF 5V
				1	1			VSBL at 58% REF 5V
		0	0					VHCH at 42% REF 5V
		0	1					VHCH at 50% REF 5V
		1	0					VHCH at 58% REF 5V
		1	1					VHCH at 66% REF 5V
	0							VHCL at 17% VHCH
	1							VHCL at 33% VHCH
0								High cut OFF
1								High cut ON

Table 19. Test (10)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	Test
								Stereodecoder test signal
							0	OFF
							1	Test signal enabled
						0		External Clock
						1		Internal Clock
								Test signal
		0	0	0	0			VHCCH
		0	0	0	1			Level internal
		0	0	1	0			Pilot magnitude
		0	0	1	1			VCO control voltage
		0	1	0	0			Pilot Threshold
		0	1	0	1			HOLDN
		0	1	1	0			NB threshold
		0	1	1	1			F228
		1	0	0	0			VHCCL
		1	0	0	1			VSBL
		1	0	1	0			SBPWM
		1	0	1	1			TBD
		1	1	0	0			PEAK
		1	1	0	1			REF5V
		1	1	1	0			REF5V5
		1	1	1	1			VBG1.95
	0							**VCO**
	1							OFF
								ON
								Audio processor test mode
0								Enabled
1								OFF

Table 20. Bass (11)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	Bass
								Bass
				0	0	0	0	-14dB
				0	0	0	1	-12dB
				:	:	:	:	:
				0	1	1	0	-2dB
				0	1	1	1	0dB
				1	1	1	1	0dB
				1	1	1	0	+2dB
				:	:	:	:	:
				1	0	0	1	+12dB
				1	0	0	0	+14dB
								Bass DC Mode
			0					DC Gain = 0dB
			1					DC Gain = 4.4 dB
								Bass Softstep
		0						On
		1						Off
x	x							Not Used

Table 21. Softstep Control (12)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	Softstep Control
								AutoZero Function
							0	Off
							1	On
								Soft Step Time
					0	0		0.84ms
					0	1		1.68ms
					1	0		3.36ms
					1	1		6.72ms
			1	1				Reserved
								STD Discharge
		0						Off
		1						On
x	x							Not Used

9 Package information

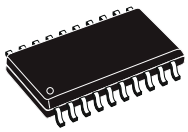
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.
ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 18. SO20 Mechanical data and package dimensions

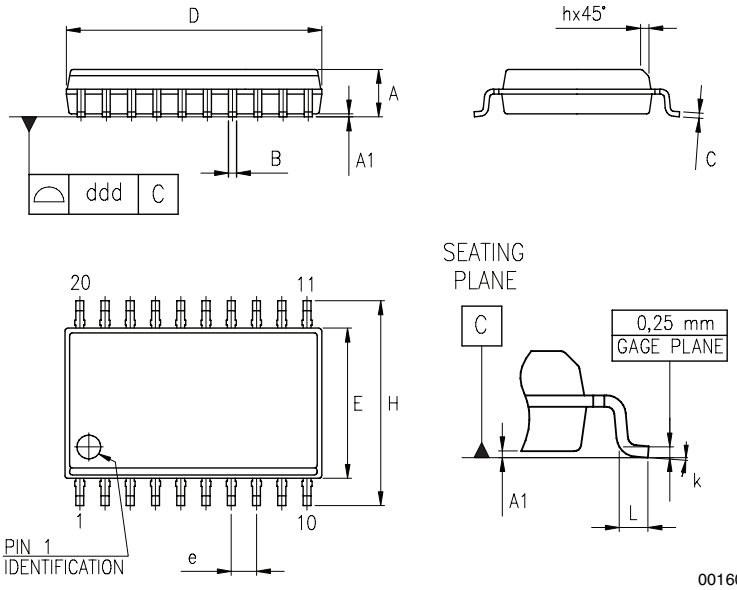
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
B	0.33		0.51	0.013		0.200
C	0.23		0.32	0.009		0.013
D (1)	12.60		13.00	0.496		0.512
E	7.40		7.60	0.291		0.299
e		1.27			0.050	
H	10.0		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

(1) "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

OUTLINE AND MECHANICAL DATA



SO20



10 Revision history

Table 22. Document revision history

Date	Revision	Changes
20-Feb-2007	1	Initial release.
28-Feb-2007	2	Corrected typos.