

**QUADRUPL 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS**

APRIL 1985 — REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

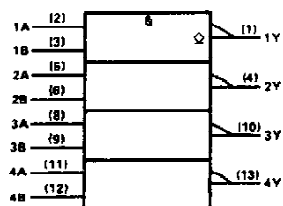
**description**

These devices contain four independent 2-input NAND gates. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher  $V_{OH}$  levels.

The SN5401 and SN54LS01 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN7401 and SN74LS01 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

**FUNCTION TABLE (each gate)**

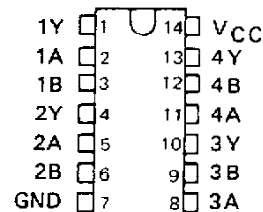
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

**logic symbol†**

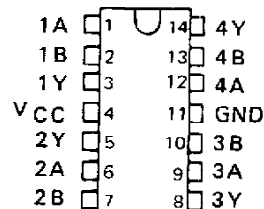
†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

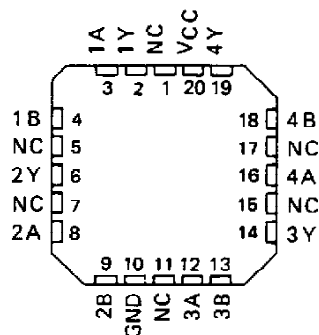
SN5401 . . . J PACKAGE  
SN54LS01 . . . J OR W PACKAGE  
SN7401 . . . N PACKAGE  
SN74LS01 . . . D OR N PACKAGE  
(TOP VIEW)



SN5401 . . . W PACKAGE  
(TOP VIEW)



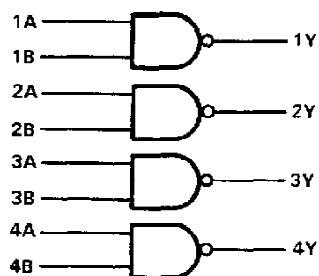
SN54LS01 . . . FK PACKAGE  
(TOP VIEW)



NC - No internal connection

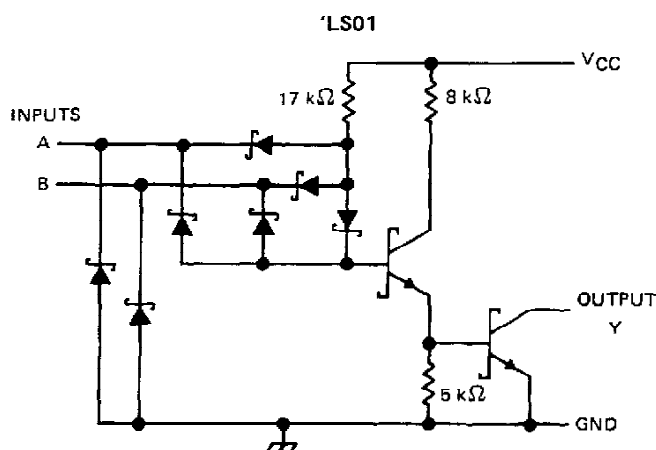
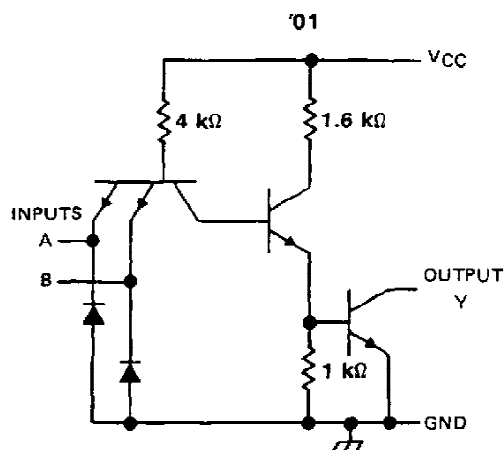
**SN5401, SN54LS01,  
SN7401, SN74LS01  
QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS**

logic diagram (positive logic)



positive logic:  $Y = \overline{A \cdot B}$  or  $Y = \overline{A} + \overline{B}$

schematics (each gate)



Resistor values shown are nominal.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, $V_{CC}$ (see Note 1): '01, 'LS01	7 V
Input voltage: '01	5.5 V
'LS01	7 V
Off-state output voltage	7 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminals.

**TEXAS  
INSTRUMENTS**

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# SN5401, SN7401 QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

## recommended operating conditions

	SN5401			SN7401			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub> Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub> High-level input voltage	2			2			V
V <sub>IL</sub> Low-level input voltage			0.8			0.8	V
V <sub>OH</sub> High-level output voltage			5.5			5.5	V
I <sub>OL</sub> Low-level output current			16			16	mA
T <sub>A</sub> Operating free-air temperature	-55		125	0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN5401			SN7401			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -12 mA			-1.5			-1.5	V
I <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.8 V, V <sub>OH</sub> = 5.5 V						0.25	mA
	V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.7 V, V <sub>OH</sub> = 5.5 V			0.25				
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 16 mA			0.2			0.4	V
I <sub>I</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V			1			1	mA
I <sub>IH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V			40			40	μA
I <sub>IL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V			-1.6			-1.6	mA
I <sub>CCH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0			4			8	mA
I <sub>CCL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 4.5 V			12			22	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

## switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	A or B	Y	R <sub>L</sub> = 4 kΩ,	C <sub>L</sub> = 15 pF		35	55	ns
t <sub>PHL</sub>			R <sub>L</sub> = 400 Ω,	C <sub>L</sub> = 15 pF		8	15	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

**SN54LS01, SN74LS01****QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS****recommended operating conditions**

	SN54LS01			SN74LS01			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$ Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$V_{IH}$ High-level input voltage	2			2			V
$V_{IL}$ Low-level input voltage			0.7			0.8	V
$V_{OH}$ High-level output voltage			5.5			5.5	V
$I_{OL}$ Low-level output current			4			8	mA
$T_A$ Operating free-air temperature	-55		125	0		70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS†	SN54LS01			SN74LS01			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IK}$	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
$I_{OH}$	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{OH} = 5.5 \text{ V}$			0.1			0.1	mA
$V_{OL}$	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 4 \text{ mA}$	0.25		0.4	0.25		0.4	V
	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 8 \text{ mA}$				0.35		0.5	
$I_I$	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
$I_{IH}$	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	µA
$I_{IL}$	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
$I_{CCH}$	$V_{CC} = \text{MAX}, V_I = 0$	0.8		1.6	0.8		1.6	mA
$I_{CCL}$	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$	2.4		4.4	2.4		4.4	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .**switching characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$  (see note 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	A or B	Y	$R_L = 2 \text{ k}\Omega, C_L = 15 \text{ pF}$		17	32	ns
$t_{PHL}$					15	28	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

  
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**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN5401J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS01J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS01J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SN7401N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN7401N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN7401N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN7401N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74LS01D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI
SN74LS01D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI
SN74LS01DR	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI
SN74LS01DR	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI
SN74LS01N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74LS01N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74LS01N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74LS01N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SNJ5401J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ5401J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ5401W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
SNJ5401W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
SNJ54LS01FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
SNJ54LS01FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
SNJ54LS01J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS01J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS01W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
SNJ54LS01W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

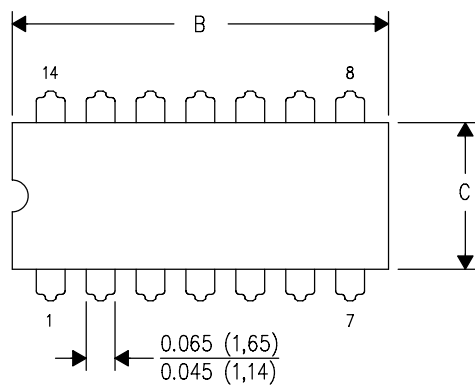
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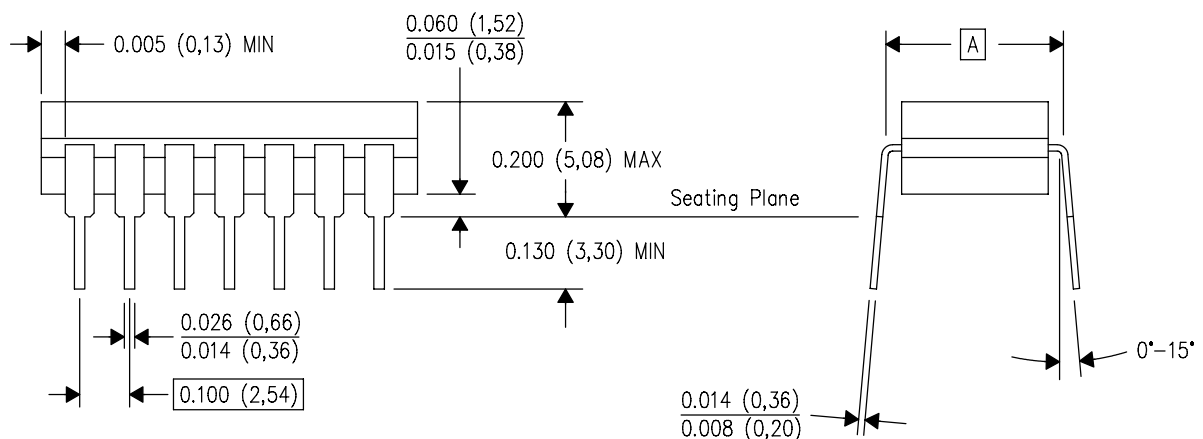
J (R—GDIP—T\*\*) (R—GDIP—T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN—LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



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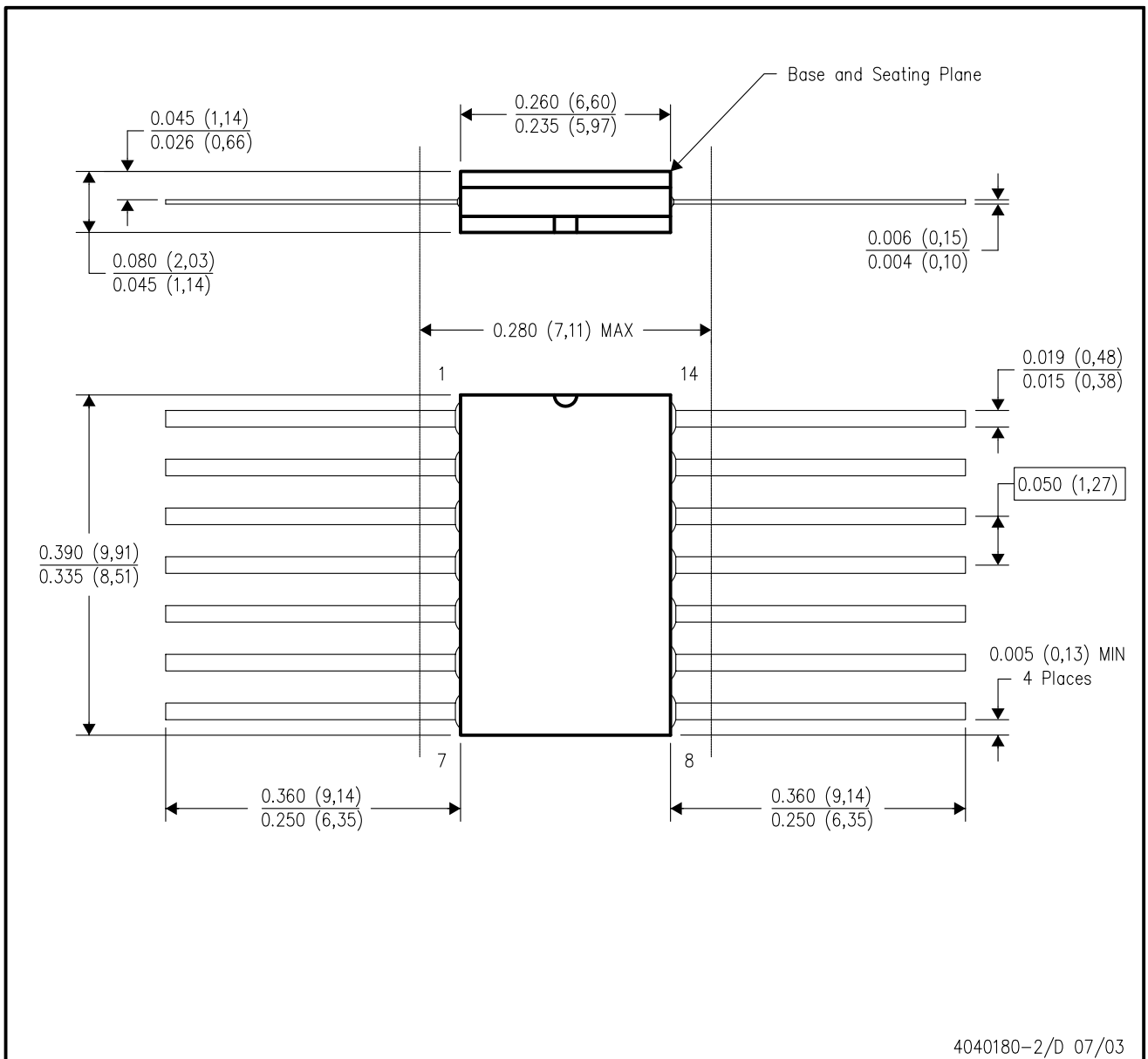
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1—T14, GDIP1—T16, GDIP1—T18 and GDIP1—T20.



## MECHANICAL DATA

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

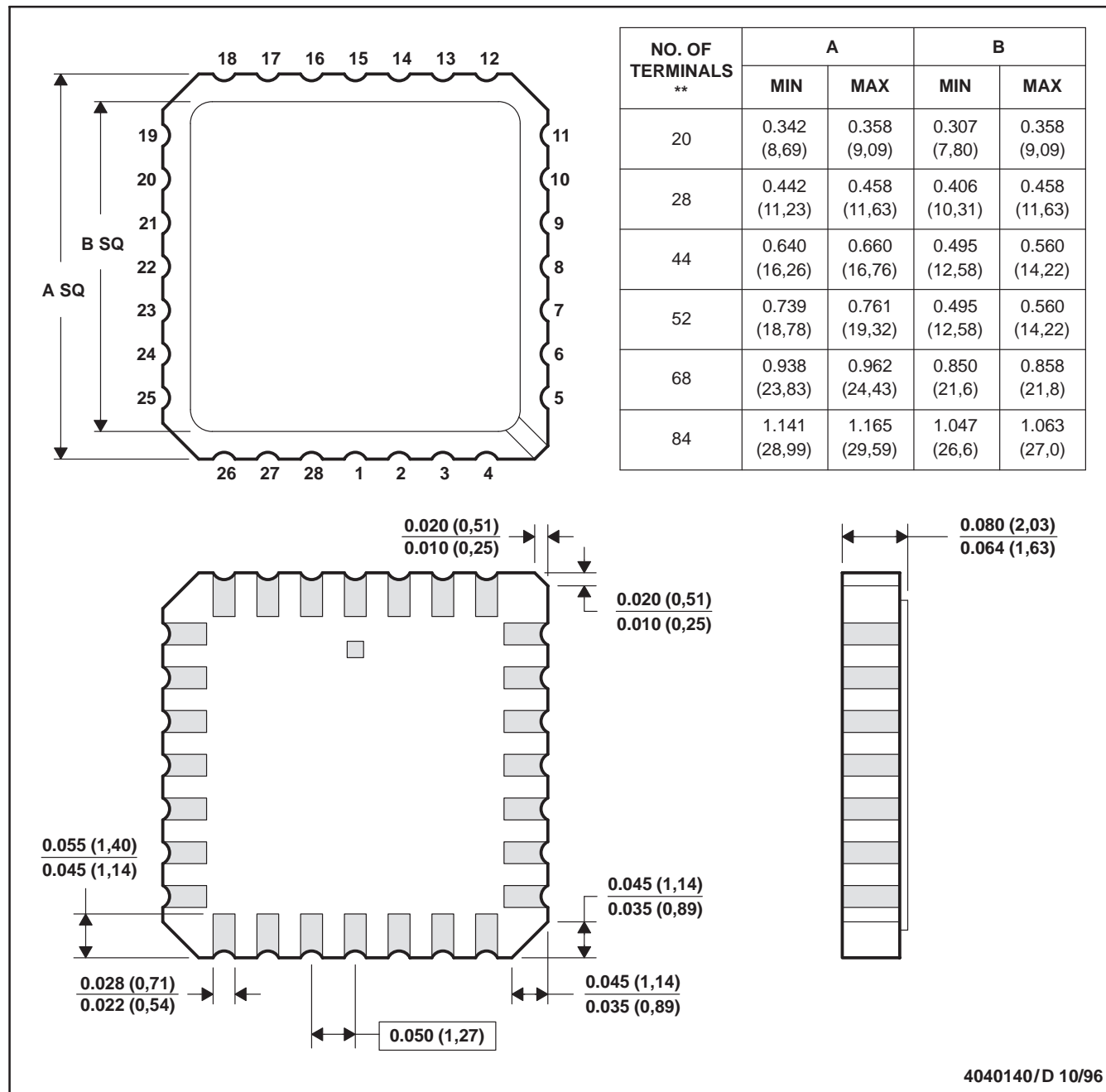
# MECHANICAL DATA

MLCC006B – OCTOBER 1996

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



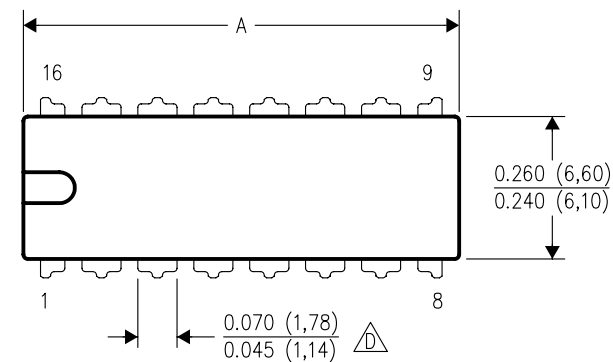
- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - The terminals are gold plated.
  - Falls within JEDEC MS-004

## MECHANICAL DATA

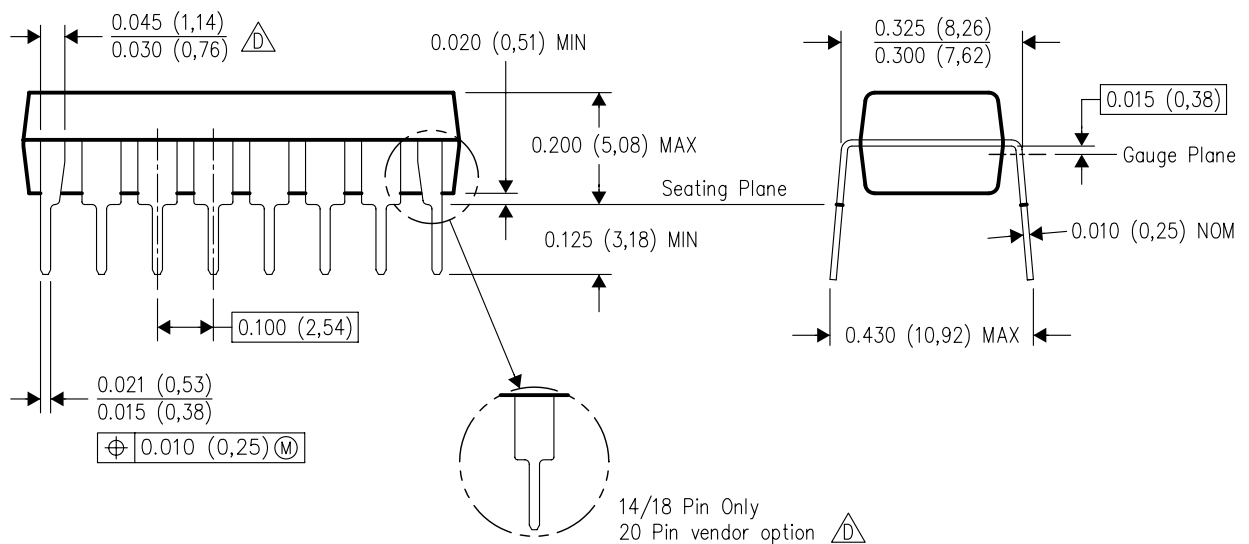
N (R-PDIP-T\*\*)

16 PINS SHOWN



# PLASTIC DUAL-IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



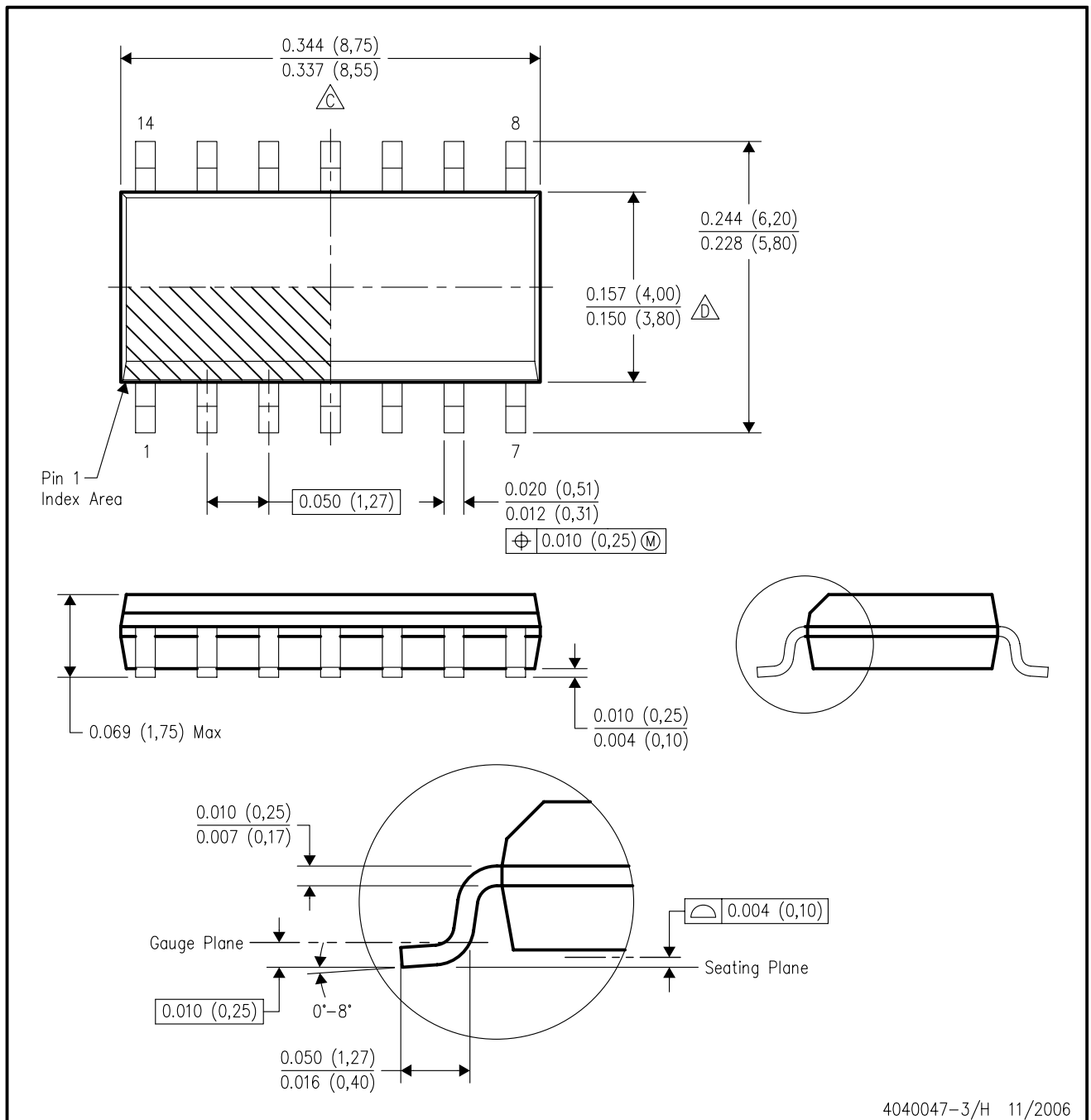
4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

# MECHANICAL DATA

## D (R-PDSO-G14)

## PLASTIC SMALL-OUTLINE PACKAGE



4040047-3/H 11/2006

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AB.

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