Features

- Minimal External Circuitry Requirements, no RF Components on the PC Board Except Matching to the Receiver Antenna
- High Sensitivity, Especially at Low Data Rates
- SSO20 and SO20 package
- Fully Integrated VCO
- Supply Voltage 4.5V to 5.5V, Operating Temperature Range –40°C to +105°C
- Single-ended RF Input for Easy Adaptation to l/4 Antenna or Printed Antenna on PCB
- Low-cost Solution Due to High Integration Level
- Various Types of Protocols Supported (i.e., PWM, Manchester and Bi-phase)
- Distinguishes the Signal Strength of Several Transmitters via RSSI (Received Signal Strength Indicator)
- ESD Protection According to MIL-STD. 883 (4KV HBM)
- High Image Frequency Suppression Due to 1 MHz IF in Conjunction with a SAW Front-end Filter, up to 40 dB is thereby Achievable with Newer SAWs
- Power Management (Polling) is Possible by Means of a Separate Pin via the Microcontroller
- Receiving Bandwidth BIF = 600 kHz

Lead Free

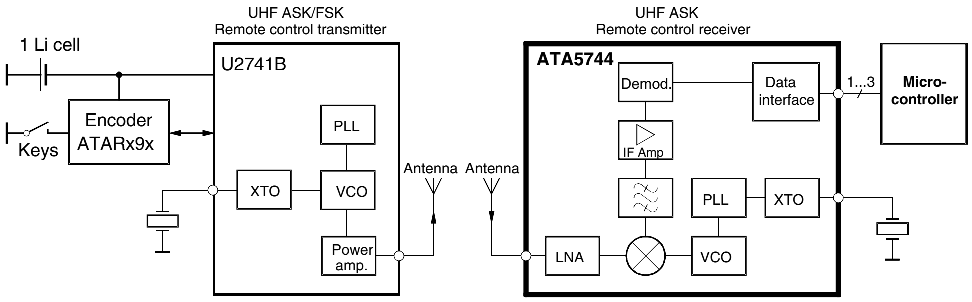
UHF ASK Receiver

ATA5744

1. Description

The ATA5744 is a PLL receiver device for the receiving range of f_0 = 300 MHz to 450 MHz. It is developed for the demands of RF low-cost data communication systems with low data rates and fits for most types of modulation schemes including Manchester, Bi-phase and most PWM protocols. Its main applications are in the areas of telemetering, security technology and keyless-entry systems.

Figure 1-1. System Block Diagram



Rev. 4893A–RKE–11/05

2. Pin Configuration

Figure 2-1. Pinning SO20 and SSO20

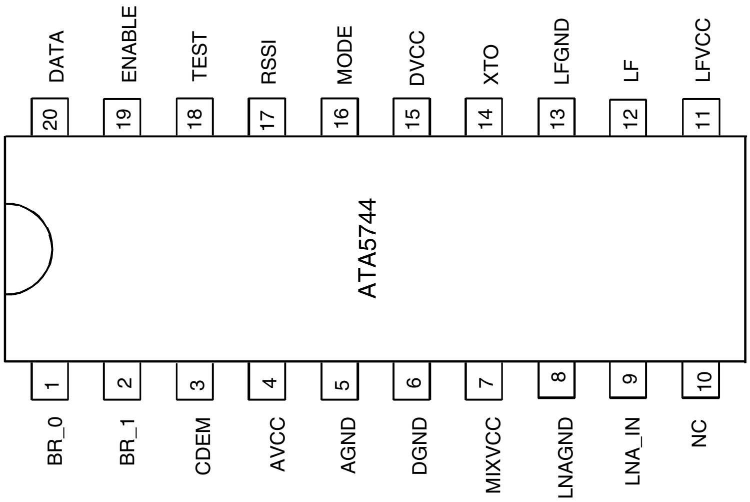
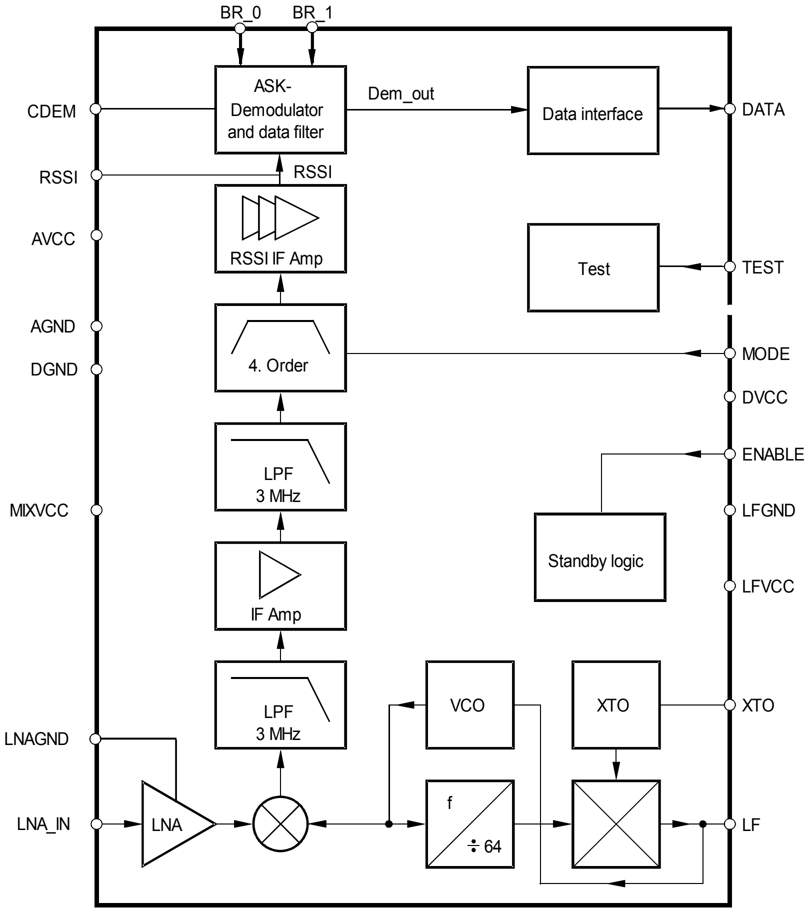


Table 2-1. Pin Description

Pin	Symbol	Function
1	BR_0	Baud rate select LSB
2	BR_1	Baud rate select MSB
3	CDEM	Lower cut-off frequency data filter
4	AVCC	Analog power supply
5	AGND	Analog ground
6	DGND	Digital ground
7	MIXVCC	Power supply mixer
8	LNAGND	High-frequency ground LNA and mixer
9	LNA_IN	RF input
10	NC	Not connected
11	LFVCC	Power supply VCO
12	LF	Loop filter
13	LFGND	Ground VCO
14	XTO	Crystal oscillator
15	DVCC	Digital power supply
16	MODE	Selecting 433.92 MHz /315 MHz Low: 315 MHz (USA) High: 433.92 MHz (Europe)
17	RSSI	Output of the RSSI amplifier
18	TEST	Test pin, during operation at GND
19	ENABLE	Selecting operation mode Low: sleep mode High: receiving mode
20	DATA	Data output

Figure 2-2. Block Diagram



3. RF Front End

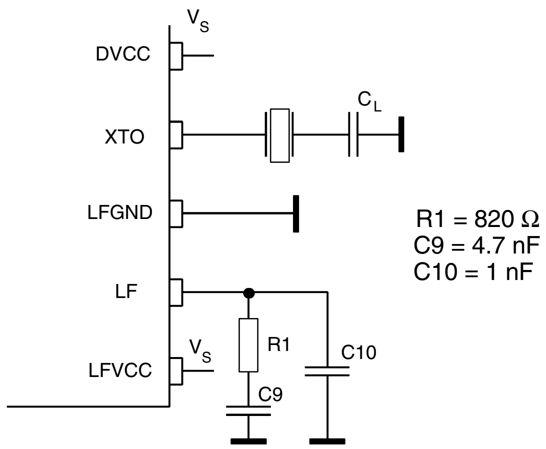
The RF front end of the receiver is a heterodyne configuration that converts the input signal into a 1-MHz IF signal. According to Figure 2-2, the front end consists of an LNA (Low-Noise Amplifier), LO (Local Oscillator), a mixer and RF amplifier.

The LO generates the carrier frequency for the mixer via a PLL synthesizer. The XTO (crystal oscillator) generates the reference frequency f_{XTO}. The VCO (Voltage-Controlled Oscillator) generates the drive voltage frequency f_{LO} for the mixer. f_{LO} is dependent on the voltage at pin LF. f_{LO} is divided by factor 64. The divided frequency is compared to f_{XTO} by the phase frequency detector. The current output of the phase frequency detector is connected to a passive loop filter and thereby generates the control voltage VLF for the VCO. By means of that configuration, VLF is controlled in a way that $f_{LO}/64$ is equal to f_{XTO}. If f_{LO} is determined, f_{XTO} can be calculated using the following formula:

$$f_{XTO} = f_{LO}/64$$

The XTO is a one-pin oscillator that operates at the series resonance of the quartz crystal. According to Figure 3-1, the crystal should be connected to GND via a capacitor CL. The value of that capacitor is recommended by the crystal supplier. The value of CL should be optimized for the individual board layout to achieve the exact value of f_{XTO} and hereby of f_{LO}. When designing the system in terms of receiving bandwidth, the accuracy of the crystal and the XTO must be considered.

Figure 3-1. PLL Peripherals



The passive loop filter connected to pin LF is designed for a loop bandwidth of B_{Loop} = 100 kHz. This value for B_{Loop} exhibits the best possible noise performance of the LO. Figure 3-1 shows the appropriate loop filter components to achieve the desired loop bandwidth

f_{LO} is determined by the RF input frequency f_{RF} and the IF frequency f_{IF} using the following formula:

$f_{LO} = f_{RF} - f_{IF}$

To determine f_{LO}, the construction of the IF filter must be considered at this point. The nominal IF frequency is f_{IF} = 1 MHz. To achieve a good accuracy of the filter's corner frequencies, the filter is tuned by the crystal frequency f_{XTO}. This means that there is a fixed relation between f_{IF} and f_{LO} that depends on the logic level at pin mode. This is described by the following formulas:

MODE = 0 USA $f_{IF} = f_{LO}/314$

MODE = 1 Europe $f_{IF} = f_{LO}/432.92$

The relation is designed to achieve the nominal IF frequency of f_{IF} = 1 MHz for most applications. For applications where f_{RF} = 315 MHz, MODE must be set to '0'. In the case of f_{RF} = 433.92 MHz, MODE must be set to '1'. For other RF frequencies, f_{IF} is not equal to 1 MHz. f_{IF} is then dependent on the logical level at pin MODE and on f_{RF}. Table 3-1 on page 5 summarizes the different conditions.

The RF input either from an antenna or from a generator must be transformed to the RF input pin LNA_IN. The input impedance of that pin is provided in the electrical parameters. The parasitic board inductances and capacitances also influence the input matching. The RF receiver ATA5744 exhibits its highest sensitivity at the best signal-to-noise ratio in the LNA. Hence, noise matching is the best choice for designing the transformation network.

A good practice when designing the network, is to start with power matching. From that starting point, the values of the components can be varied to some extent to achieve the best sensitivity.

If a SAW is implemented into the input network a mirror frequency suppression of ΔP_{Ref} = 40 dB can be achieved. There are SAWs available that exhibit a notch at Δf = 2 MHz. These SAWs work best for an intermediate frequency of IF = 1 MHz. The selectivity of the receiver is also improved by using a SAW. In typical automotive applications, a SAW is used.

Figure 3-2 shows a typical input matching network for f_{RF} = 315 MHz and f_{RF} = 433.92 MHz using a SAW. Figure 3-3 on page 6 illustrates the input matching to 50Ω without a SAW. The input matching networks shown in Figure 3-3 on page 6 are the reference networks for the parameters given in the electrical characteristics.

Table 3-1. Calculation of LO and IF Frequency

Conditions	Local Oscillator Frequency	Intermediate Frequency
f_{RF} = 315 MHz, MODE = 0	f_{LO} = 314 MHz	f_{IF} = 1 MHz
f_{RF} = 433.92 MHz, MODE = 1	f_{LO} = 432.92 MHz	f_{IF} = 1 MHz
300 MHz < f_{RF} < 365 MHz, MODE = 0	$f_{LO} = \frac{f_{RF}}{1 + \frac{1}{314}}$	$f_{IF} = \frac{f_{LO}}{314}$
365 MHz < f_{RF} < 450 MHz, MODE = 1	$f_{LO} = \frac{f_{RF}}{1 + \frac{1}{432.92}}$	$f_{IF} = \frac{f_{LO}}{432.92}$

Figure 3-2. Input Matching Network with SAW Filter

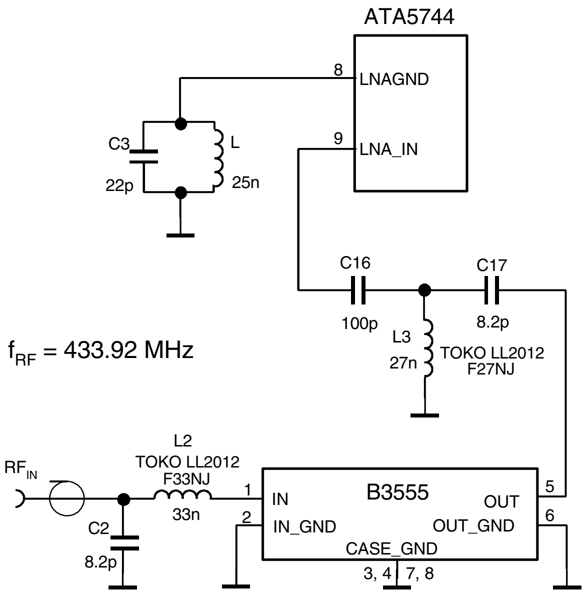
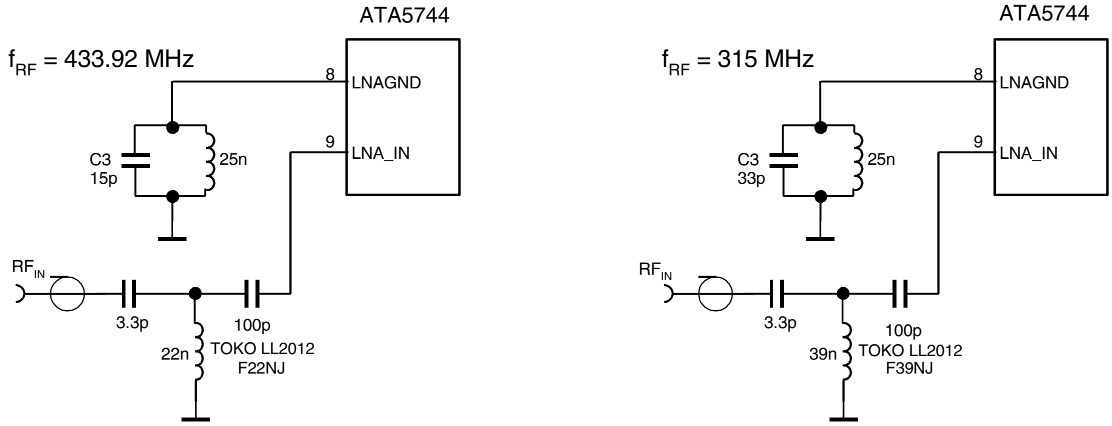


Figure 3-3. Input Matching Network without SAW Filter



Please note that for all coupling conditions (see Figure 3-2 on page 5 and Figure 3-3), the bond wire inductivity of the LNA ground is compensated. C3 forms a series resonance circuit together with the bond wire. L = 25 nH is a feed inductor to establish a DC path. Its value is not critical but must be large enough not to detune the series resonance circuit. For cost reduction, this inductor can be easily printed on the PCB. This configuration improves the sensitivity of the receiver by about 1 dB to 2 dB.

4. Analog Signal Processing

4.1 IF Amplifier

The signals coming from the RF front end are filtered by the fully integrated 4th-order IF filter. The IF center frequency is f_{IF} = 1 MHz for applications where f_{RF} = 315 MHz or f_{RF} = 433.92 MHz is used. For other RF input frequencies, refer to Table 3-1 on page 5 to determine the center frequency.

The receiver ATA5744 employs an IF bandwidth of B_{IF} = 600 kHz and can be used together with the U2741B in ASK mode.

4.2 RSSI Amplifier

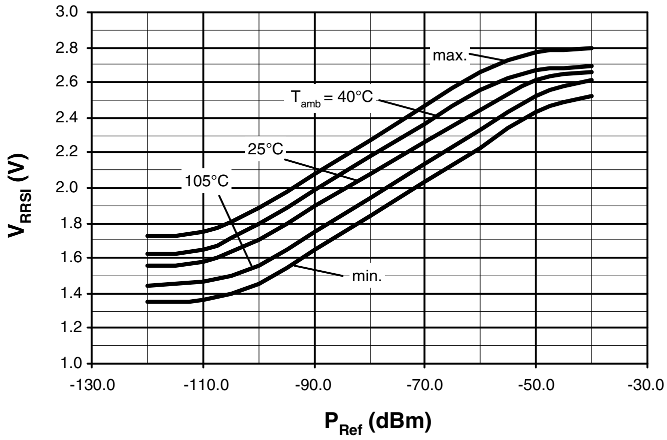
The subsequent RSSI amplifier enhances the output signal of the IF amplifier before it is fed into the demodulator. The dynamic range of this amplifier is DRRSSI = 60 dB. If the RSSI amplifier is operated within its linear range, the best S/N ratio is maintained. If the dynamic range is exceeded by the transmitter signal, the S/N ratio is defined by the ratio of the maximum RSSI output voltage and the RSSI output voltage due to a disturber. The dynamic range of the RSSI amplifier is exceeded if the RF input signal is about 60 dB higher compared to the RF input signal at full sensitivity.

4.3 Pin RSSI

The output voltage of the RSSI amplifier (VRSSI) is available at pin RSSI. Using the RSSI output signal, the signal strength of different transmitters can be distinguished. The usable input power range P_{Ref} is –100 dBm to –55 dBm.

Since different RF input networks may exhibit slightly different values for the LNA gain, the sensitivity values given in the electrical characteristics refer to a specific input matching. This matching is illustrated in Figure 3-3 and exhibits the best possible sensitivity.

Figure 4-1. RSSI Characteristics



4.4 ASK Demodulator and Data Filter

The signal coming from the RSSI amplifier is converted into the raw data signal by the ASK demodulator.

An automatic threshold control circuit (ATC) is employed to set the detection reference voltage to a value where a good signal-to-noise ratio is achieved. This circuit also implies the effective suppression of any kind of inband noise signals or competing transmitters. If the S/N ratio exceeds 10 dB, the data signal can be detected properly.

The output signal of the demodulator is filtered by the data filter before it is fed into the digital signal processing circuit. The data filter improves the S/N ratio as its passband can be adopted to the characteristics of the data signal. The data filter consists of a 1st-order highpass and a 1st-order lowpass filter.

The highpass filter cut-off frequency is defined by an external capacitor connected to pin CDEM. The cut-off frequency of the highpass filter is defined by the following formula:

$$\text{fcu\_DF} = \frac{1}{2 \times \pi \times R_1 \times \text{CDEM}}$$

Recommended values for CDEM are given in the electrical characteristics.

The cut-off frequency of the lowpass filter is defined by the selected baudrate range (BR_Range). BR_Range is defined by the pins BR_0 and BR_1. BR_Range must be set in accordance to the used baudrate.

Table 4-1. Definition of BR_Range by the Pins BR_0 and BR_1

BR_1	BR_0	BR_Range
0	0	0
0	1	1
1	0	2
1	1	2

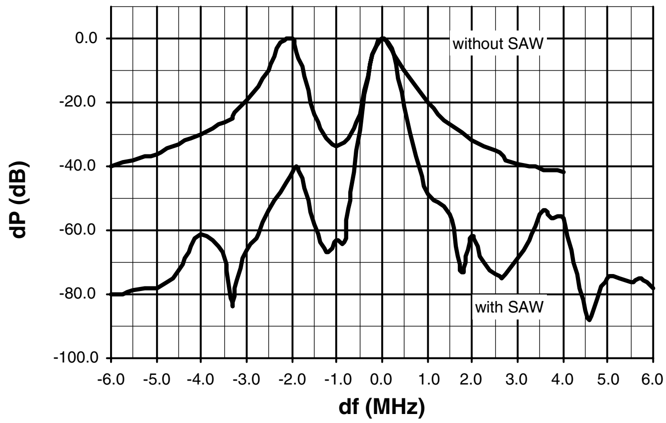
Each BR_Range is defined by a minimum and a maximum edge-to-edge time (tee_sig). These limits are defined in the electrical characteristics. They should not be exceeded to maintain full sensitivity of the receiver.

4.5 Receiving Characteristics

The RF receiver ATA5744 can be operated with and without a SAW front-end filter. In a typical automotive application, a SAW filter is used to achieve better selectivity. The selectivity with and without a SAW front-end filter is illustrated in Figure 4-1 on page 7. Note that the mirror frequency is reduced by 40 dB. The plots are printed relatively to the maximum sensitivity. If a SAW filter is used, an insertion loss of about 4 dB must be considered.

When designing the system in terms of receiving bandwidth, the LO deviation must be considered as it also determines the IF center frequency. The total LO deviation is calculated to be the sum of the deviation of the crystal and the XTO deviation of the ATA5744. Low-cost crystals are specified to be within ±100 ppm. The XTO deviation of the ATA5744 is an additional deviation due to the XTO circuit. This deviation is specified to be ±30 ppm. If a crystal of ±100 ppm is used, the total deviation is ±130 ppm in that case. Note that the receiving bandwidth and the IF-filter bandwidth are equivalent.

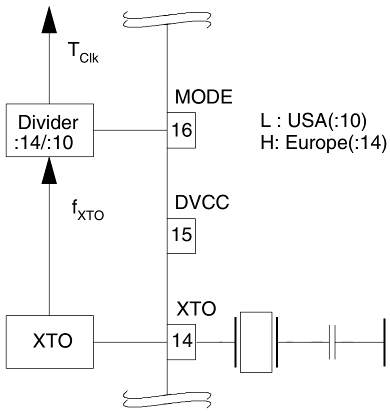
Figure 4-2. Receiving Frequency Response



4.6 Basic Clock Cycle of the Digital Circuitry

The complete timing of the digital circuitry and the analog filtering is derived from one clock. According to Figure 4-3, this clock cycle TClk is derived from the crystal oscillator (XTO) in combination with a divider. The division factor is controlled by the logical state at pin MODE. According to chapter 'RF Front End', the frequency of the crystal oscillator (f_{XTO}) is defined by the RF input signal (f_{RFin}) which also defines the operating frequency of the local oscillator (f_{LO}).

Figure 4-3. Generation of the Basic Clock Cycle



Pin MODE can now be set in accordance with the desired clock cycle T_{Clk}. T_{Clk} controls the following application-relevant parameters:

Timing of the analog and digital signal processing

IF filter center frequency (f_{IF0})

Most applications are dominated by two transmission frequencies: f_{Send} = 315 MHz is mainly used in USA, f_{Send} = 433.92 MHz in Europe. In order to ease the usage of all T_{Clk}-dependent parameters, the electrical characteristics display three conditions for each parameter.

- Application USA
  (f_{XTO} = 4.90625 MHz, MODE = L, T_{Clk} = 2.0383 µs)
- Application Europe
  (f_{XTO} = 6.76438 MHz, MODE = H, T_{Clk} = 2.0697 µs)
- Other applications
  (T_{Clk} is dependent on f_{XTO} and on the logical state of pin MODE. The electrical characteristic is given as a function of T_{Clk}).

The clock cycle of some function blocks depends on the selected baud rate range (BR_Range) which is defined by the pins BR_0 and BR_1. This clock cycle T_{XClk} is defined by the following formulas for further reference:

BR_Range = BR_Range0: $T_{XClk} = 8 \times T_{Clk}$
BR_Range1: $T_{XClk} = 4 \times T_{Clk}$
BR_Range2: $T_{XClk} = 2 \times T_{Clk}$
BR_Range3: $T_{XClk} = 1 \times T_{Clk}$

5. Pin ENABLE

Via the pin ENABLE the operating mode of the receiver can be selected (see Figure 5-1 and Figure 5-2).

If the pin ENABLE is held to Low, the receiver remains in sleep mode. All circuits for signal processing are disabled and only the XTO is running in that case. The current consumption is $I_S = I_{Soff}$ in that case. During the sleep mode the receiver is not sensitive to a transmitter signal.

To activate the receiver, the pin ENABLE must be held to High. During the start-up period, $T_{Startup}$, all signal processing circuits are enabled and settled. The duration of the start-up period depends on the selected baud-rate range (BR_Range).

After the start-up period, all circuits are in a stable condition and the receiver is in the receiving mode.

In receiving mode, the internal data signal (Dem_out) is switched to pin DATA. To avoid incorrect timing at the begin of the data stream, the begin is synchronized to a falling edge of the incoming data signal. The receiver stays in the receiving mode until it is switched back to sleep mode via pin ENABLE.

During start-up and receiving mode, the current consumption is $I_S = I_{Son}$.

Figure 5-1. Enable Timing (1)

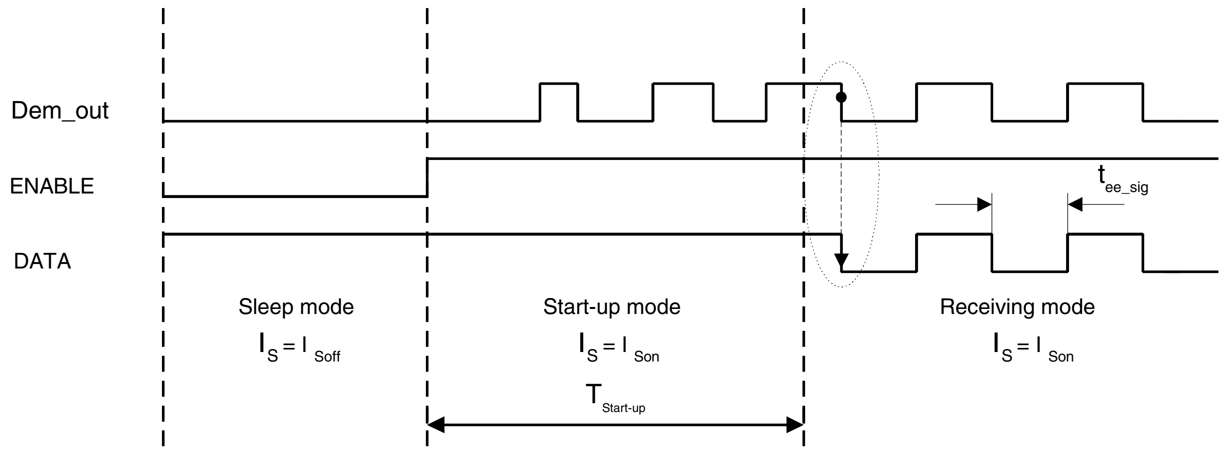
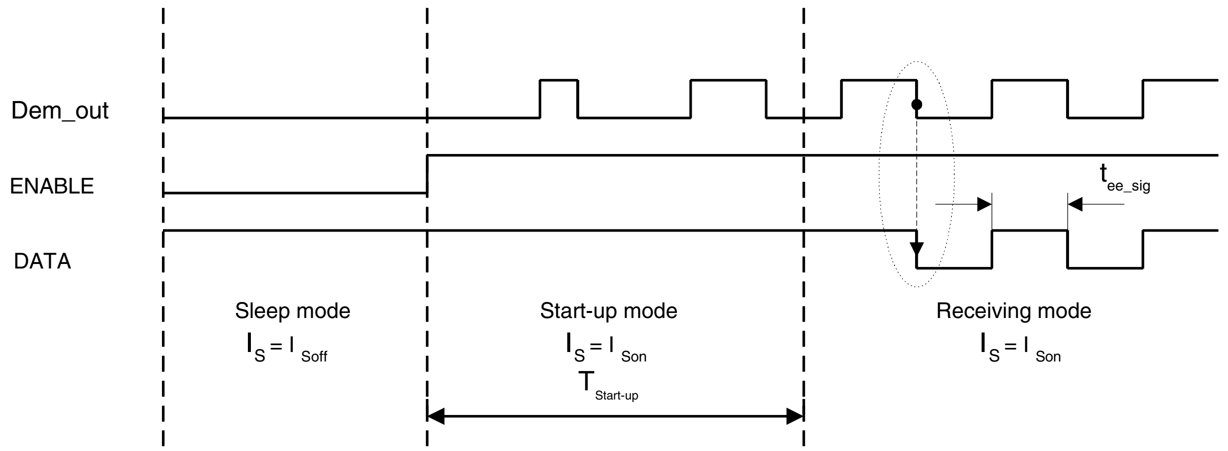


Figure 5-2. Enable Timing (2)



6. Digital Signal Processing

The data from the ASK demodulator (Dem_out) is digitally processed in different ways and as a result converted into the output signal DATA. This processing depends on the selected baudrate range (BR_Range). Figure 6-1 on page 11 illustrates how Dem_out is synchronized by the extended basic clock cycle T_{XClk}. Data can change its state only after T_{XClk} has elapsed. The edge-to-edge time period tee_sig of the DATA signal as a result is always an integral multiple of T_{XClk}.

The minimum time period between two edges of the data signal is limited to tee_sig ≥ T_{DATA_min}. This implies an efficient suppression of spikes at the DATA output. At the same time it limits the maximum frequency of edges at DATA. This eases the interrupt handling of a connected microcontroller.

Figure 6-1. Synchronization of the Demodulator Output

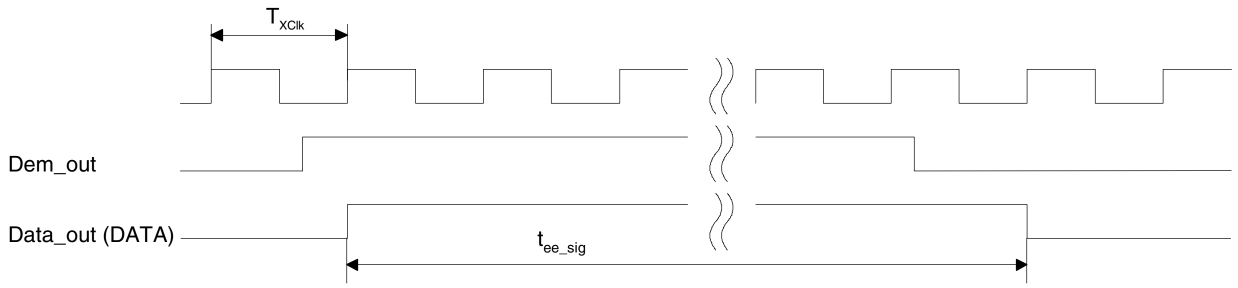
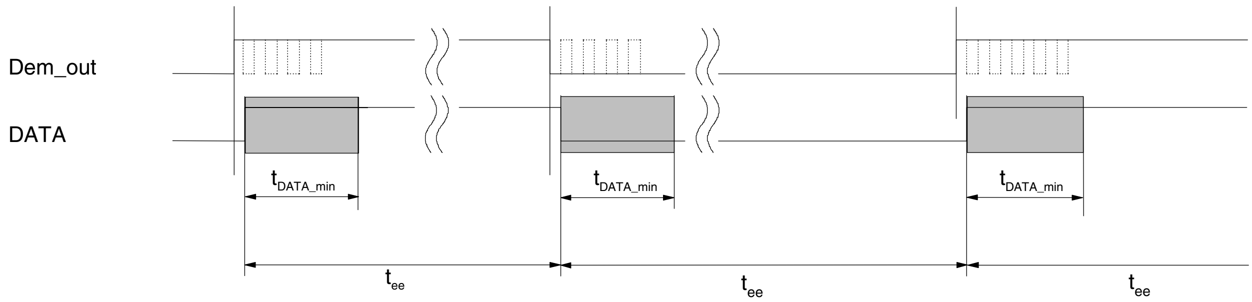


Figure 6-2. Debouncing of the Demodulator Output



7. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Min.	Max.	Unit
Supply voltage	V_S		6	V
Power dissipation	P_{tot}		450	mW
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	–55	+125	°C
Ambient temperature	T_{amb}	–40	+105	°C
Maximum input level, input matched to 50Ω	P_{in_max}		10	dBm

8. Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient SO20 package	R_{thJA}	100	K/W
Junction ambient SSO20 package	R_{thJA}	100	K/W

9. Electrical Characteristics

All parameters refer to GND, T_{amb} = –40°C to +105°C, V_S = 4.5V to 5.5V, f_0 = 433.92 MHz and f_0 = 315 MHz, unless otherwise specified. (V_S = 5V, T_{amb} = 25°C)

Parameters	Test Conditions	Symbol	6.76438 MHz Osc. (MODE:1)			4.90625 MHz Osc. (MODE:0)			Variable Oscillator			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Basic Clock Cycle of the Digital Circuitry												
Basic clock cycle	MODE = 0 (USA) MODE = 1 (Europe)	T_{Clk}	2.0697		2.0697	2.0383		2.0383	$1/(f_{xto}/10)$ $1/(f_{xto}/14)$		$1/(f_{xto}/10)$ $1/(f_{xto}/14)$	µs µs
Extended basic clock cycle	BR_Range0 BR_Range1 BR_Range2 BR_Range3	T_{XClk}	16.6 8.3 4.1 2.1		16.6 8.3 4.1 2.1	16.3 8.2 4.1 2.0		16.3 8.2 4.1 2.0	$8 \times T_{Clk}$ $4 \times T_{Clk}$ $2 \times T_{Clk}$ $1 \times T_{Clk}$		$8 \times T_{Clk}$ $4 \times T_{Clk}$ $2 \times T_{Clk}$ $1 \times T_{Clk}$	µs µs µs µs
Start-up time (see Figure 5-1 and Figure 5-2 on page 10)	BR_Range0 BR_Range1 BR_Range2 BR_Range3	$T_{Startup}$	1855 1061 1061 663		1855 1061 1061 663	1827 1045 1045 653		1827 1045 1045 653	896.5 512.5 512.5 320.5 $\times T_{Clk}$		896.5 512.5 512.5 320.5 $\times T_{Clk}$	µs µs µs µs µs
Receiving Mode												
Intermediate frequency	MODE=0 (USA) MODE=1 (Europe)	f_{IF}		1.0			1.0		$f_{XTO} \times 64/314$ $f_{XTO} \times 64/432.92$			MHz MHz
Minimum time period between edges at pin DATA	BR_Range0 BR_Range1 BR_Range2 BR_Range3 (Figure 6-2 on page 11)	T_{DATA_min}	165 83 41.4 20.7		165 83 41.4 20.7	163 81 40.7 20.4		163 81 40.7 20.4	$10 \times T_{XClk}$ $10 \times T_{XCl}$ $10 \times T_{XClk}$ $10 \times T_{XClk}$		$10 \times T_{XClk}$ $10 \times T_{XCl}$ $10 \times T_{XClk}$ $10 \times T_{XClk}$	µs µs µs µs
Edge to edge time period of the data signal for full sensitivity	BR_Range0 BR_Range1 BR_Range2 BR_Range3 (Figure 5-1 on page 10)	t_{ee_sig}	400 200 100 50		8479 8479 8479 8479	400 200 100 50		8350 8350 8350 8350	BR_Range $\times$ 2 µs/T_{CLK}		$4097 \times$ T_{CLK}	µs µs µs µs

10. Electrical Characteristics (continued)

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Current consumption	Sleep mode (XTO active)	IS_{off}		190	276	µA
	IC active (startup-, receiving mode) pin DATA = H	IS_{on}		7.1	8.7	mA
LNA Mixer						
Third-order intercept point	LNA/ mixer/ IF amplifier input matched according to Figure 3-3 on page 6	IIP3		–28		dBm
LO spurious emission at RF_{In}	Input matched according to Figure 3-3 on page 6, required according to I-ETS 300220	IS_{LORF}		–73	–57	dBm
Noise figure LNA and mixer (DSB)	Input matching according to Figure 3-3 on page 6	NF		7		dB
LNA_IN input impedance	At 433.92 MHz At 315 MHz	Zi_{LNA_IN}		1.0 ǁ 1.56 1.3 ǁ 1.0		kΩ ǁ pF kΩ ǁ pF

10. Electrical Characteristics (continued)

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
1 dB compression point (LNA, mixer, IF amplifier)	Input matched according to Figure 3-3 on page 6, referred to RF_{in}	IP_{1db}		–40		dBm
Maximum input level	Input matched according to Figure 3-3 on page 6, BER $\leq 10^{-3}$	P_{in_max}			–20	dBm
Local Oscillator						
Operating frequency range VCO		f_{VCO}	299		449	MHz
Phase noise VCO/LO	f_{osc} = 432.92 MHz at 1 MHz at 10 MHz	L (fm)		–93 –113	–90 –110	dBC/Hz dBC/Hz
Spurious of the VCO	at $\pm f_{XTO}$			–55	–47	dBC
VCO gain		K_{VCO}		190		MHz/V
Loop bandwidth of the PLL	For best LO noise (design parameter) R1 = 820Ω C9 = 4.7 nF C10 = 1 nF	B_{Loop}		100		kHz
Capacitive load at pin LF		C_{LF_tot}			10	nF
XTO operating frequency	XTO crystal frequency, appropriate load capacitance must be connected to XTAL f_{XTAL} = 6.764375 MHz (EU) f_{XTAL} = 4.90625 MHz (US)	f_{XTO}	6.764375 –30 ppm 4.90625 –30 ppm	6.764375 4.90625	6.764375 +30 ppm 4.90625 +30 ppm	MHz MHz
Series resonance resistor of the crystal	f_{XTO} = 6.764 MHz 4.906 MHz	R_S			150 220	Ω Ω
Static capacitance of the crystal		C_o			6.5	pF
Analog Signal Processing						
Input sensitivity	Input matched according to Figure 3-3 ASK (level of carrier) BER $\leq 10^{-3}$ (Manchester), f_{in} = 433.92 MHz/ 315 MHz T = 25°C, V_S = 5V, f_{IF} = 1 MHz	P_{Ref_ASK}				
	BR_Range0 (1 kBd)		–107	–110	–112	dBm
	BR_Range1 (2 kBd)		–105	–108	–110	dBm
	BR_Range2 (4kBd)		–103	–106	–108	dBm
	BR_Range3 (8 kBd)		–101	–104	–106	dBm
Sensitivity variation for the full operating range compared to T_{amb} = 25°C, V_S = 5V	f_{in} = 433.92 MHz/315 MHz f_{IF} = 1 MHz $P_{ASK} = P_{Ref\_ASK} + \Delta P_{Ref}$	ΔP_{Ref}	+2.5		–1.5	dB

10. Electrical Characteristics (continued)

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Sensitivity variation for full operating range including IF filter compared to T_{amb} = 25°C, V_S = 5V	f_{in} = 433.92 MHz/ 315 MHz f_{IF} = 0.79 MHz to 1.21 MHz f_{IF} = 0.73 MHz to 1.27 MHz $P_{ASK} = P_{Ref\_ASK} + \Delta P_{Ref}$	ΔP_{Ref}	+5.5 +7.5		–1.5 –1.5	dB dB
S/N ratio to suppress inband noise signals		SNR		10	12	dB
Dynamic range RSSI amplifier		ΔR_{RSSI}		60		dB
RSSI output voltage range		V_{RSSI}	1.0		3.0	V
RSSI gain		G_{RSSI}		20		mV/dB
RI of pin CDEM for cut-off frequency calculation	$fcu\_DF = \frac{1}{2 \times \pi \times R_1 \times CDEM}$	R_I	28	40	55	kΩ
Recommended CDEM for best performance	BR_Range0 BR_Range1 BR_Range2 BR_Range3	CDEM		33 18 10 6.8		nF nF nF nF
Upper cut-off frequency data filter	Upper cut-off frequency BR_Range0 BR_Range1 BR_Range2 BR_Range3	f_u	1.75 3.5 7.0 14.0	2.2 4.4 8.8 17.6	2.65 5.3 10.6 21.2	kHz kHz kHz kHz
Digital Ports						
Data output - Saturation voltage LOW - Internal pull-up resistor	I_{ol} = 1 mA	V_{Ol} R_{Pup}	39	0.08 50	0.3 65	V kΩ
ENABLE input - Low-level input voltage - High-level input voltage	Sleep mode Receiving mode	V_{Il} V_{Ih}	$0.8 \times V_S$		$0.2 \times V_S$	V V
MODE input - Low-level input voltage - High-level input voltage	Division factor = 10 Division factor = 14	V_{Il} V_{Ih}	$0.8 \times V_S$		$0.2 \times V_S$	V V
BR_0 input - Low-level input voltage - High-level input voltage		V_{Il} V_{Ih}	$0.8 \times V_S$		$0.2 \times V_S$	V V
BR_1 input - Low-level input voltage - High-level input voltage		V_{Il} V_{Ih}	$0.8 \times V_S$		$0.2 \times V_S$	V V
TEST input - Low-level input voltage	Test input must always be set to LOW	V_{Il}			$0.2 \times V_S$	V

Figure 10-1. Application Circuit: f_{RF} = 433.92 MHz, without SAW Filter

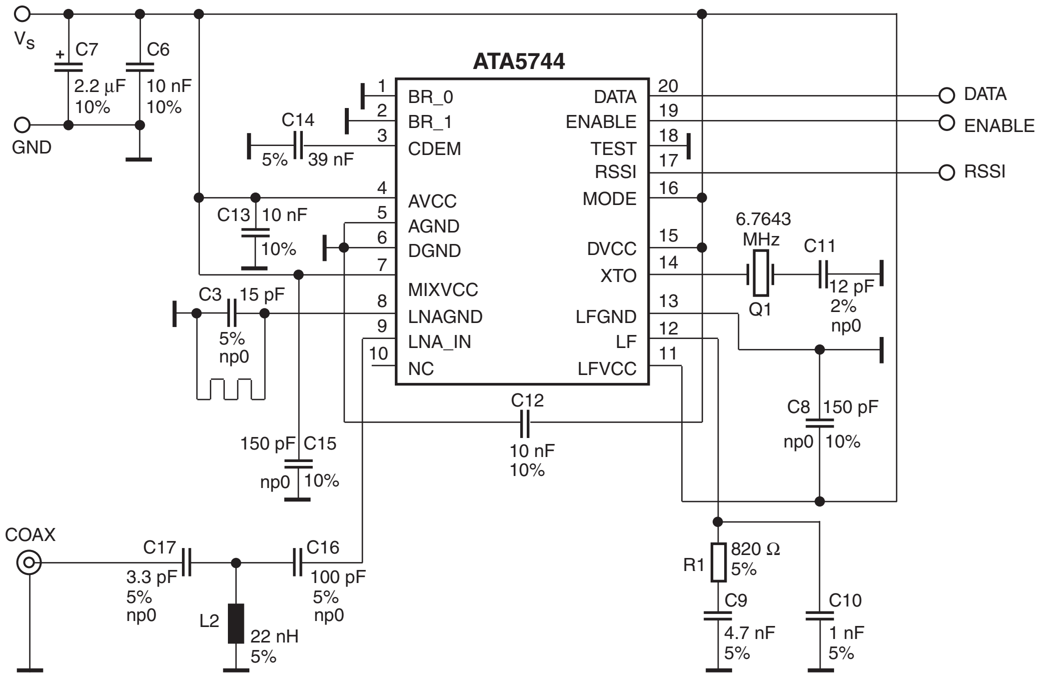


Figure 10-2. Application Circuit: f_{RF} = 315 MHz, without SAW Filter

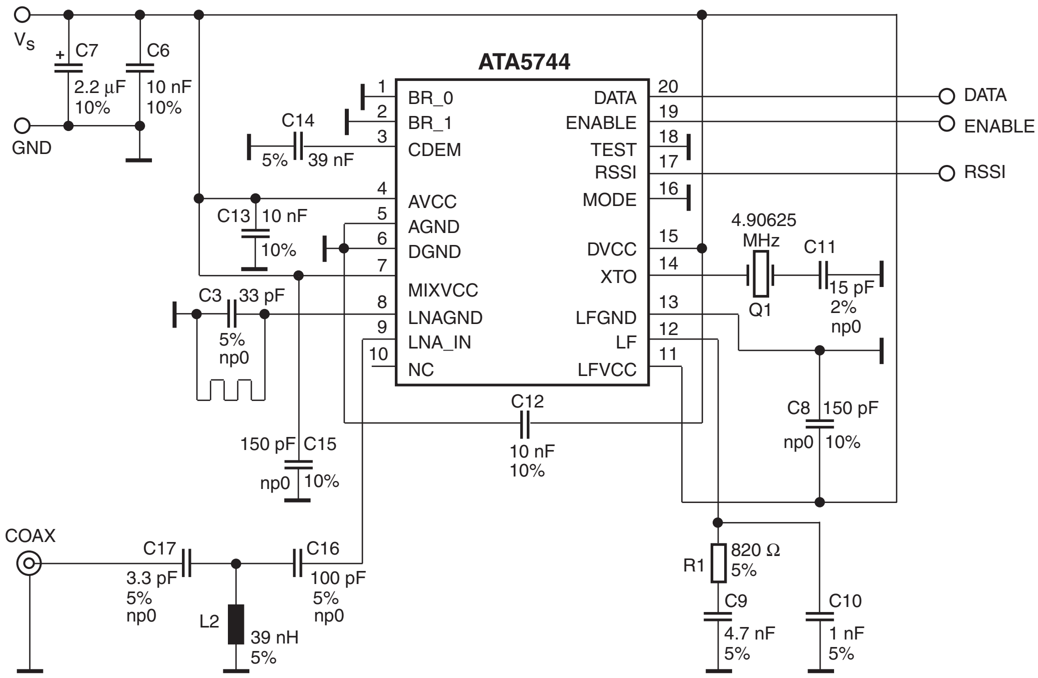


Figure 10-3. Application Circuit: f_{RF} = 433.92 MHz, with SAW Filter

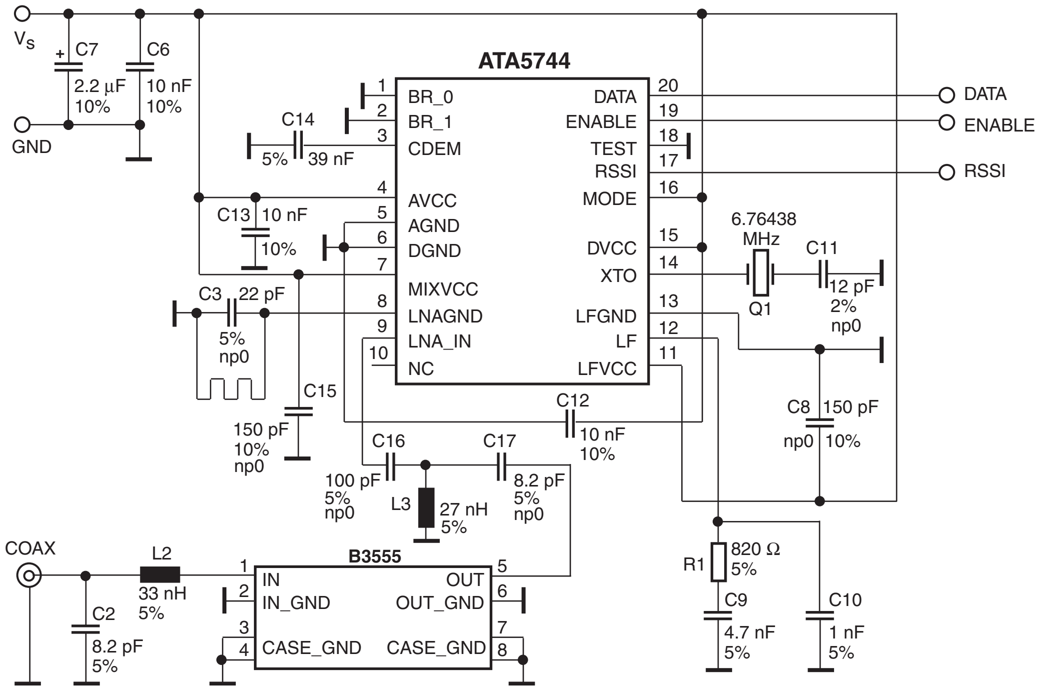
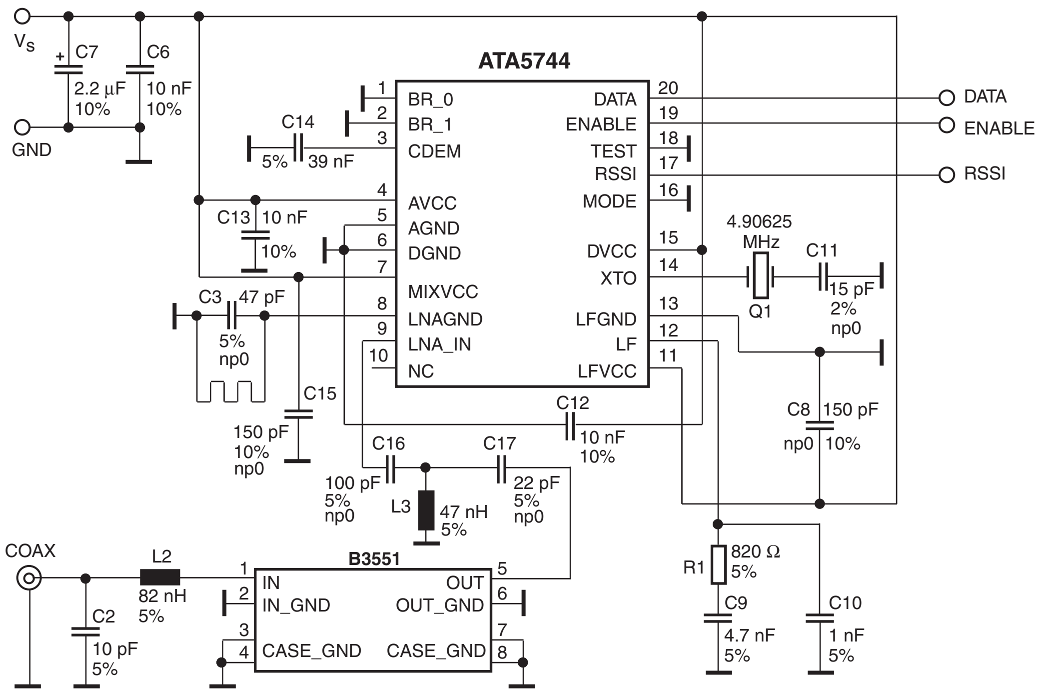


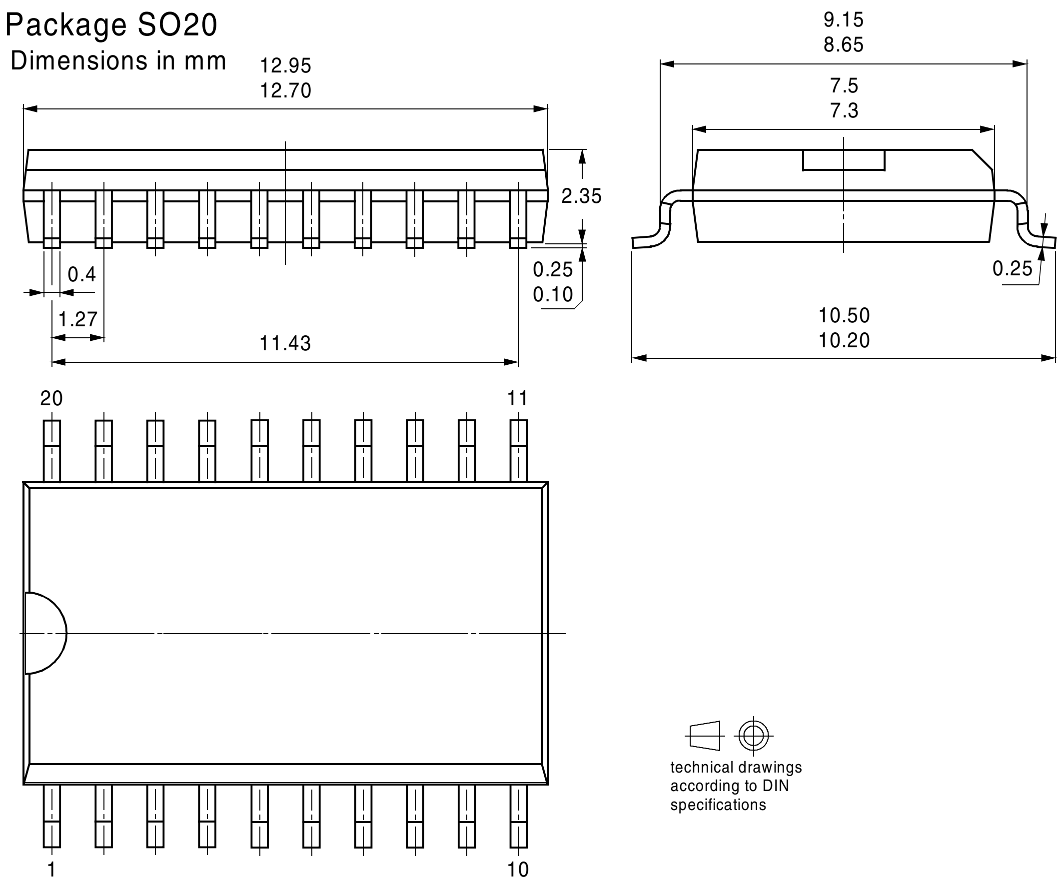
Figure 10-4. Application Circuit: f_{RF} = 315 MHz, with SAW Filter



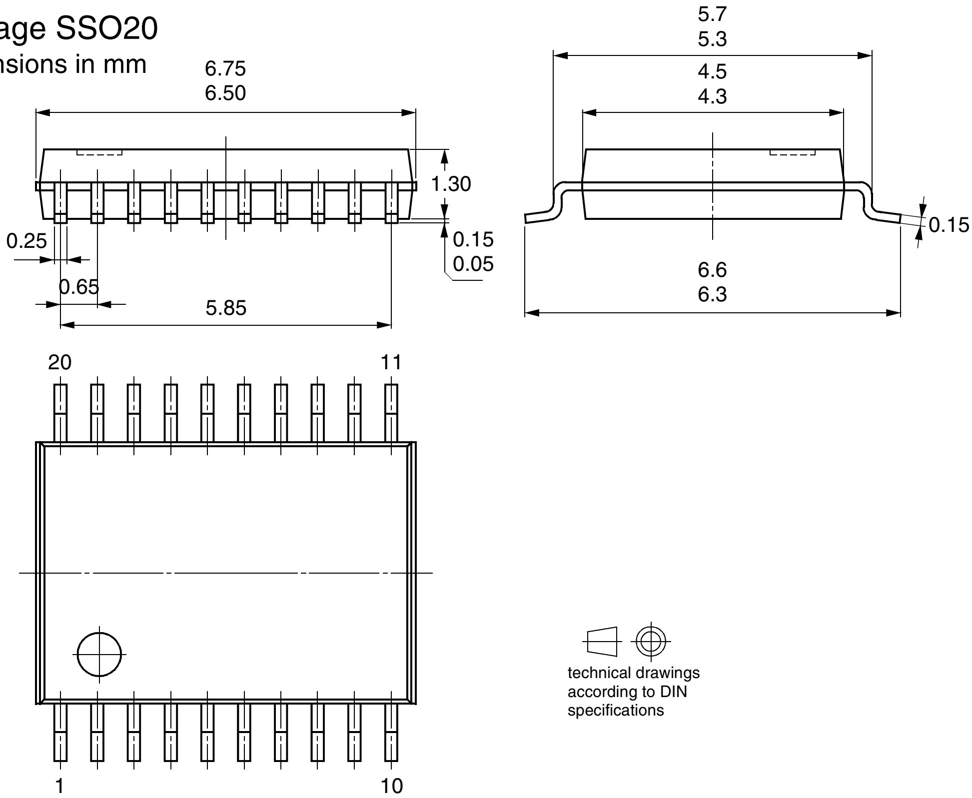
11. Ordering Information

Extended Type Number	Package	Remarks
ATA5744N-TKSY	SSO20	Tube, Pb-free
ATA5744N-TKQY	SSO20	Taped and reeled, Pb-free
ATA5744N-TGSY	SO20	Tube, Pb-free
ATA5744N-TGQY	SO20	Taped and reeled, Pb-free

12. Package Information



Package SSO20
Dimensions in mm



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