T-45-17-00

54AC11286, 74AC11286
9-BIT PARITY GENERATORS/CHECKERS
WITH BUS DRIVER PARITY I/O PORTS

TI0119—D3165, AUGUST 1988—REVISED MARCH 1990

- Generates Either Odd or Even Parity for Nine Data Lines
- Cascadable for n-Bits Parity
- Direct Bus Connection for Parity Generation or for Checking by using the Parity I/O Port
- Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
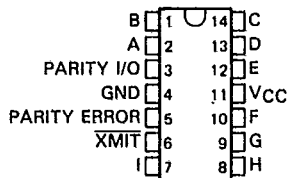
description

The 'AC11286 universal 9-bit parity generator/checkers feature a local output for parity checking and a bus-driving parity I/O port for parity generation/checking. The word-length capability is easily expanded by cascading.
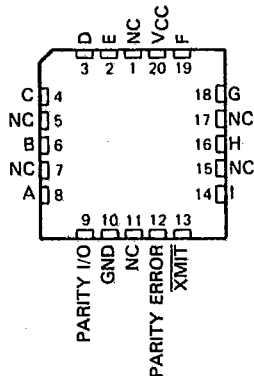
The XMIT control input is implemented specifically to accommodate cascading. When the XMIT is low, the parity tree is disabled and the Parity Error output will remain at a high logic level regardless of the input levels. When XMIT is high, the parity tree is enabled. The Parity Error output will indicate a parity error when either an even number of inputs (A through I) are high and Parity I/O is forced to a low logic level, or when an odd number of inputs are high and Parity I/O is forced to a high logic level.

The 54AC11286 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11286 is characterized for operation from −40°C to 85°C.

54AC11286 ... J PACKAGE
74AC11286 ... D OR N PACKAGE
(TOP VIEW)

```
            B [ 1  U 14 ] C
            A [ 2    13 ] D
    PARITY I/O [ 3    12 ] E
          GND [ 4    11 ] VCC
  PARITY ERROR [ 5    10 ] F
         XMIT [ 6     9 ] G
            I [ 7     8 ] H
```

54AC11286 ... FK PACKAGE
(TOP VIEW)

```
              D  E  NC VCC F
              3  2  1  20 19
          C [ 4           18 ] G
         NC [ 5           17 ] NC
          B [ 6           16 ] H
         NC [ 7           15 ] NC
          A [ 8           14 ] I
              9 10 11 12 13
         PARITY I/O  GND  NC  PARITY ERROR  XMIT
```

NC—No internal connection

FUNCTION TABLE

NUMBER OF INPUTS (A THRU I) THAT ARE HIGH	XMIT INPUT	PARITY I/O	PARITY ERROR OUTPUT
0, 2, 4, 6, 8	l	H	H
1, 3, 5, 7, 9	l	L	H
0, 2, 4, 6, 8	h	h	H
	h	l	L
1, 3, 5, 7, 9	h	h	L
	h	l	H

h — high input level   l — low input level
H — high output level   L — low output level

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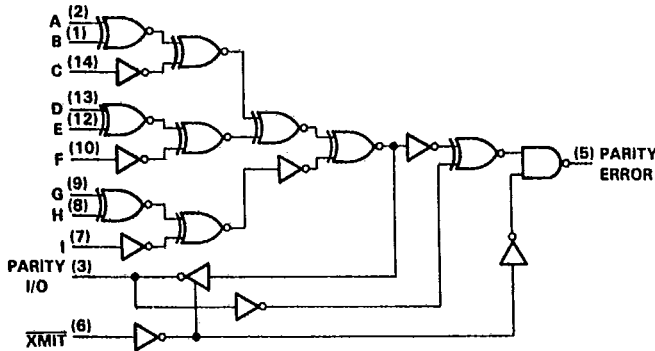
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logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)

Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} .... -0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... -0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1)..................................... -0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) .... ± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)...................................... ± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}).. ± 50 mA
Continuous current through V_{CC} or GND pins .... ± 100 mA
Storage temperature range .... $-65°C$ to $150°C$

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only
  and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is
  not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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recommended operating conditions

			54AC11286			74AC11286			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3		5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 3$ V	2.1			2.1			V
		$V_{CC} = 4.5$ V	3.15			3.15			
		$V_{CC} = 5.5$ V	3.85			3.85			
V_{IL}	Low-level input voltage	$V_{CC} = 3$ V			0.9			0.9	V
		$V_{CC} = 4.5$ V			1.35			1.35	
		$V_{CC} = 5.5$ V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 3$ V			−4			−4	mA
		$V_{CC} = 4.5$ V			−24			−24	
		$V_{CC} = 5.5$ V			−24			−24	
I_{OL}	Low-level output current	$V_{CC} = 3$ V			12			12	mA
		$V_{CC} = 4.5$ V			24			24	
		$V_{CC} = 5.5$ V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25°C$			54AC11286		74AC11286		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -50$ μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	$I_{OH} = -4$ mA	3 V	2.58			2.4		2.48		
	$I_{OH} = -24$ mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	$I_{OH} = -50$ mA†	5.5 V				3.85				
	$I_{OH} = -75$ mA†	5.5 V						3.85		
V_{OL}	$I_{OL} = 50$ μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	$I_{OL} = 12$ mA	3 V			0.36		0.5		0.44	
	$I_{OL} = 24$ mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	$I_{OL} = 50$ mA†	5.5 V					1.65			
	$I_{OL} = 75$ mA†	5.5 V							1.65	
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±10		±5	μA
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		160		80	μA
C_i	$V_I = V_{CC}$ or GND	5 V		3.5						pF
C_o	$V_O = V_{CC}$ or GND	5 V		8.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

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switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11286		74AC11286		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any A thru I	Parity I/O	2.6	10	11.7	2.6	14.2	2.6	13.1	ns
t_{PHL}			3.8	11.6	14.5	3.8	17.1	3.8	16.1	
t_{PLH}	Any A thru I	Parity Error	3	8.5	13.1	3	15.8	3	14.7	ns
t_{PHL}			4	10.9	16	4	19	4	17.8	
t_{PLH}	Parity I/O	Parity Error	2.2	5.9	7.6	2.2	9	2.2	8.4	ns
t_{PHL}			3.4	7.9	10.2	3.4	11.7	3.4	11.1	
t_{PZH}	$\overline{XMIT}$	Parity I/O	1.8	4.9	6.4	1.8	7.4	1.8	7	ns
t_{PZL}			3.5	9.7	12.8	3.5	14.2	3.5	13.6	
t_{PHZ}	$\overline{XMIT}$	Parity I/O	3.2	5.4	6.6	3.2	7.2	3.2	7	ns
PLZ			3.2	5.4	6.7	3.2	7.4	3.2	7.2	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V, (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11286		74AC11286		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any A thru I	Parity I/O	2	5.5	8	2	9.7	2	9	ns
t_{PHL}			3.1	6.9	9.1	3.1	11.5	3.1	10.7	
t_{PLH}	Any A thru I	Parity Error	2.5	5.2	8.9	2.5	10.7	2.5	10	ns
t_{PHL}			3.3	6.5	10.7	3.3	12.9	3.3	12	
t_{PLH}	Parity I/O	Parity Error	1.9	3.9	5.6	1.9	6.6	1.9	6.2	ns
t_{PHL}			2.9	5	7.2	2.9	8.4	2.9	7.9	
t_{PZH}	$\overline{XMIT}$	Parity I/O	1.4	3.3	4.9	1.4	5.6	1.4	5.3	ns
t_{PZL}			3	5.4	8.3	3	9.3	3	8.9	
t_{PHZ}	$\overline{XMIT}$	Parity I/O	3.1	4.8	6.1	3.1	6.7	3.1	6.5	ns
PLZ			3	4.6	6	3	6.5	3	6.3	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

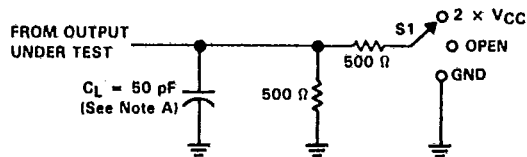| PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 1 MHz	53	pF
	Outputs disabled		46	

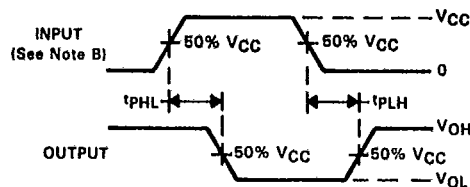**TEXAS INSTRUMENTS**
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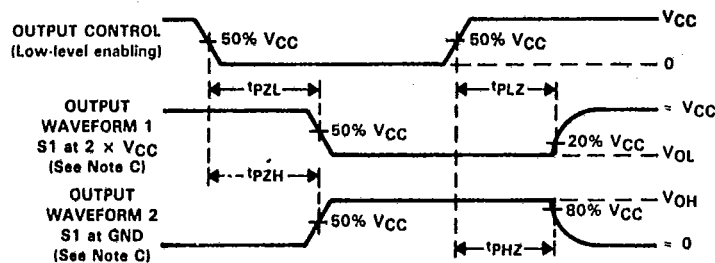
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PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

PROPAGATION DELAY TIMES

ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
   B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
   C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
      Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

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