WM8233

70MSPS 6-Channel AFE with Sensor Timing Generation and LVDS/CMOS Data Output

DESCRIPTION

The WM8233 is a 16-bit analogue front end/digitiser IC which processes and digitises the analogue output signals from CCD sensors or Contact Image Sensors (CIS) at pixel sample rates of up to 35MSPS.

The device has six analogue signal processing channels each of which contains Reset Level Clamping, Correlated Double Sampling (also Sample and Hold), Programmable Gain, Automatic Gain Control (AGC) and Offset adjust functions.

The output from each of these channels is time multiplexed, in pairs, into three high-speed 16-bit Analogue to Digital Converters. The digital data is available in a variety of output formats via the flexible data port.

The WM8233 has a user selectable LVDS or CMOS output architecture.

An internal 8-bit DAC is supplied for internal reference level generation. This may be used during CDS to reference CIS signals or during Clamping to clamp CCD signals. An external reference level may also be supplied. ADC references are generated internally, ensuring optimum performance from the device.

A programmable automatic Black-Level Calibration function is available to adjust the DC offset of the output data.

The WM8233 features a sensor timing clock generator for both CCD and CIS sensors. The clock generator can accept a slow or fast reference clock input and also has a flexible timing adjustment function for output timing clocks to allow use of many different sensors.

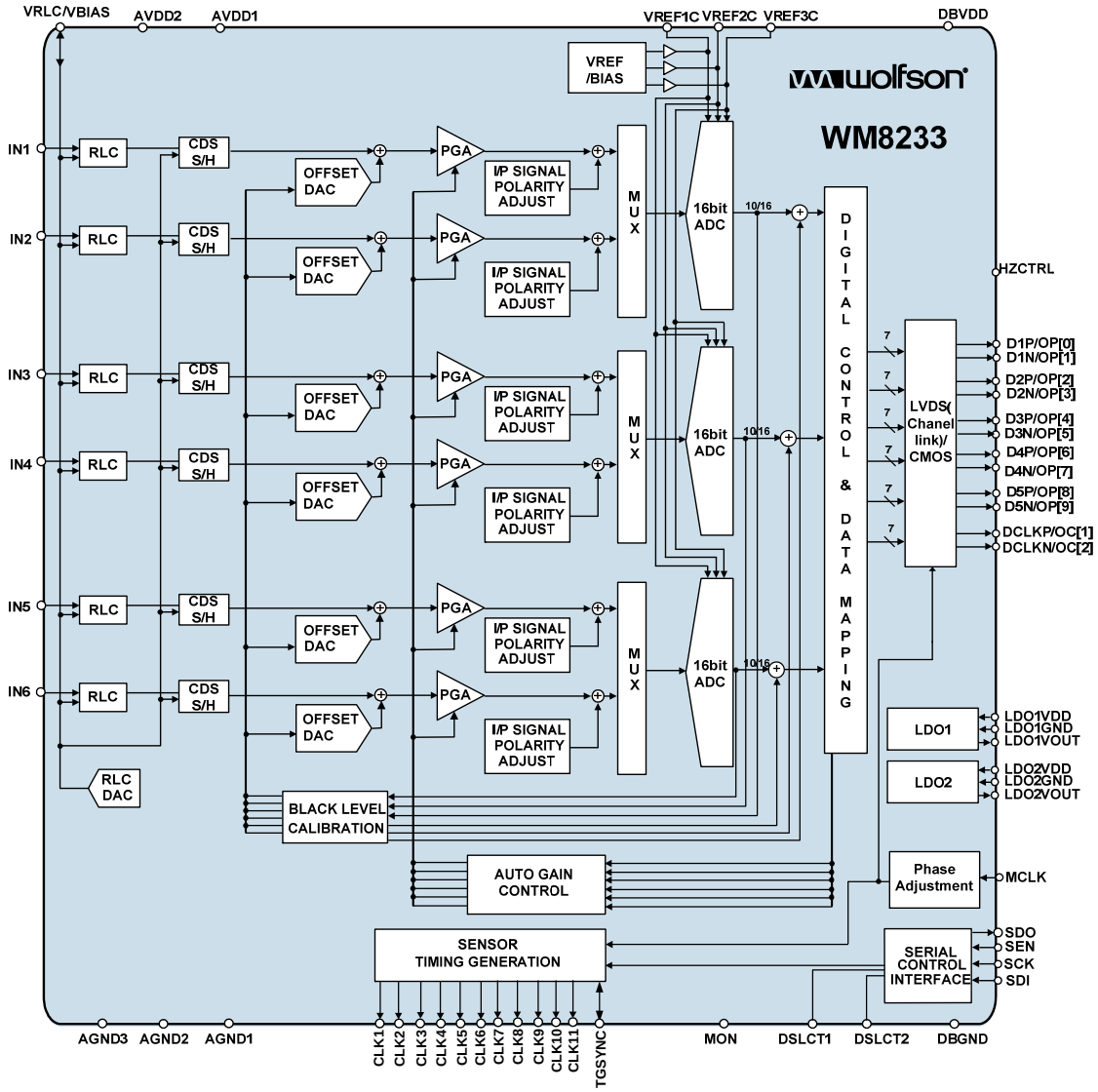
FEATURES

- 70MSPS conversion rate
- 16 bit ADC resolution
- Current consumption – 350mA
- 3.3V single supply operation
- Sample and hold /correlated double sampling
- Programmable offset adjust (8-bit resolution)
- Flexible clamp timing
- Pixel clamp / line clamp mode
- Programmable clamp voltage
- Programmable CIS/CCD timing generator
- Internally generated voltage references
- Compliant for Spread Spectrum Clock
- LVDS/CMOS output options
  - LVDS 5pair 490MHz 35-bit data
  - CMOS 90MHz output maximum
- Complete on chip clock generator. MCLK 5MHz to 35MHz
- Internal timing adjustment
- Automatic Gain Control
- Automatic Black Level Calibration
- 56-lead QFN package 8mm x 8mm
- Serial control interface

APPLICATIONS

- Digital copiers
- USB2.0 compatible scanners
- Multi-function peripherals
- High-speed CCD/CIS sensor interface

BLOCK DIAGRAM



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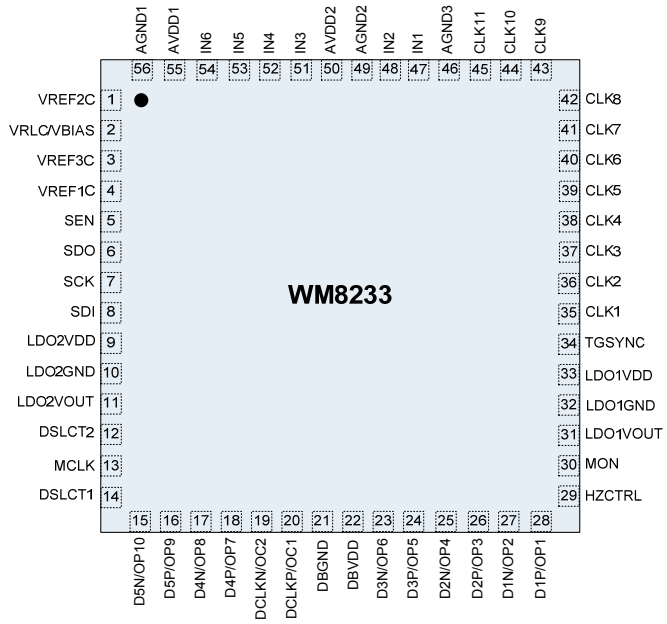
PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8233GEFL/V	-40 to 85°C	56-lead QFN (8X8x0.85mm) (Pb-free)	MSL3	260°C
WM8233GEFL/RV	-40 to 85°C	56-lead QFN (8X8x0.85mm) (Pb-free, tape and reel)	MSL3	260°C

Reel quantity = 2,200

PIN DESCRIPTION

PIN	NAME	Type	DESCRIPTION
1	VREF2C	Analogue output	Mid reference voltage. This pin must be connected to AGND via a decoupling capacitor.
2	VRLC/VBIAS	Analogue I/O	Reference voltage input/output
3	VREF3C	Analogue output	Lower reference voltage. This pin must be connected to AGND via a decoupling capacitor.
4	VREF1C	Analogue output	Upper reference voltage. This pin must be connected to AGND via a decoupling capacitor.
5	SEN	Digital input	Enables the serial interface when high.
6	SDO	Digital output	Serial interface data output
7	SCK	Digital input	Serial interface clock
8	SDI	Digital input	Serial interface data input
9	LDO2VDD	Supply	Analogue supply
10	LDO2GND	Supply	Analogue ground
11	LDO2VOUT	Supply	LDO output This pin must be connected to AGND via a decoupling capacitor.
12	DSLCT2	Analogue input	Device select 2
13	MCLK	Analogue input	Master Clock
14	DSLCT1	Analogue input	Device select 1
15	D5N/OP[9]	LVDS output	LVDS Data output 5 – Negative / CMOS output 9
16	D5P/OP[8]	LVDS output	LVDS Data output 5 – Positive / CMOS output 8
17	D4N/OP[7]	LVDS output	LVDS Data output 4 – Negative / CMOS output 7
18	D4P/OP[6]	LVDS output	LVDS Data output 4 – Positive / CMOS output 6
19	DCLKN/OC[2]	LVDS output	LVDS Clock Output – Negative/ CMOS clock output 2
20	DCLKP/OC[1]	LVDS output	LVDS Clock Output – Positive/ CMOS clock output 1
21	DBGND	Supply	Analogue ground
22	DBVDD	Supply	Analogue supply
23	D3N/OP[5]	LVDS output	LVDS Data output 3 – Negative / CMOS output 5
24	D3P/OP[4]	LVDS output	LVDS Data output 3 – Positive / CMOS output 4
25	D2N/OP[3]	LVDS output	LVDS Data output 2 – Negative / CMOS output 3
26	D2P/OP[2]	LVDS output	LVDS Data output 2 – Positive / CMOS output 2
27	D1N/OP[1]	LVDS output	LVDS Data output 1 – Negative / CMOS output 1
28	D1P/OP[0]	LVDS output	LVDS Data output 1 – Positive / CMOS output 0
29	HZCTRL	Digital input	Internal use only. Must be connected to AGND
30	MON	Analogue output	Clock monitor
31	LDO1VOUT	Supply	LDO output. This pin must be connected to AGND via a decoupling capacitor.
32	LDO1GND	Supply	Analogue ground
33	LDO1VDD	Supply	Analogue supply
34	TGSYNC	Digital input	Sensor Timing Sync pulse from host
35	CLK1	Digital output	Sensor Timing Output 1
36	CLK2	Digital output	Sensor Timing Output 2
37	CLK3	Digital output	Sensor Timing Output 3
38	CLK4	Digital output	Sensor Timing Output 4
39	CLK5	Digital output	Sensor Timing Output 5
40	CLK6	Digital output	Sensor Timing Output 6
41	CLK7	Digital output	Sensor Timing Output 7
42	CLK8	Digital output	Sensor Timing Output 8
43	CLK9	Digital output	Sensor Timing Output 9
44	CLK10	Digital output	Sensor Timing Output 10
45	CLK11	Digital output	Sensor Timing Output 11
46	AGND3	Supply	Analogue ground
47	IN1	Analogue input	Analogue input 1

PIN	NAME	Type	DESCRIPTION
48	IN2	Analogue input	Analogue input 2
49	AGND2	Supply	Analogue ground
50	AVDD2	Supply	Analogue supply
51	IN3	Analogue input	Analogue input 3
52	IN4	Analogue input	Analogue input 4
53	IN5	Analogue input	Analogue input 5
54	IN6	Analogue input	Analogue input 6
55	AVDD1	Supply	Analogue supply
56	AGND1	Supply	Analogue ground

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Analogue supply voltage: AVDD1-2, LDO1VDD-2, DBVDD	GND - 0.3V	GND + 5V
Analogue grounds: AGND1-3, LDO1GND-LDO2GND, DBGND	GND - 0.3V	GND + 0.3V
Analogue inputs (IN1-6)	GND - 0.3V	AVDD + 0.3V
Other Analogue pins	GND - 0.3V	AVDD + 0.3V
Digital I/O pins	GND - 0.3V	AVDD + 0.3V
Operating temperature range: T_A	-40°C	+85°C
Storage temperature prior to soldering	30°C max / 85% RH max	
Storage temperature after soldering	-65°C	+150°C

Notes:

1. GND denotes the voltage of any ground pin.
2. AGND, LDOGND and DBGND pins are intended to be operated at the same potential. Differential voltages between these pins will degrade performance.

RECOMMENDED OPERATING CONDITIONS

CONDITION	SYMBOL	MIN	TYP	MAX	UNITS
Operating temperature range	T_A	-40		85	°C
Analogue Supply voltage	AVDD1-2 LDO1VDD-LDO2VDD DBVDD	2.97	3.3	3.63	V

ELECTRICAL CHARACTERISTICS

Test Conditions
AVDD = LDOVDD = DBVDD = 3.3V , AGND = LDOGND = DBGND= 0V, T_A = 25°C, MCLK= 35MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overall System Specification (including 10-bit ADC, PGA, Offset and CDS functions)						
Conversion rate per channel			5		35	MSPS
Full-scale input voltage range (see Note 1)		ADCFS=0, Max Gain		0.12		Vp-p
		ADCFS=0, Min Gain		2.0		Vp-p
		ADCFS=1, Max Gain		0.18		Vp-p
		ADCFS=1, Min Gain		3.0		Vp-p
Input signal limits (see Note 2)	V_{IN}	SF_INP=0	AGND-0.3		AVDD+0.3	V
		SF_INP=1	AGND		AGND+1.2	V
Input capacitance	C_{IN}	Inputs to AGND		10		pF
Full-scale transition error		Gain = 0dB; AGAIN[4:0] = 02(hex) DGAIN[11:0] = 6AB(hex)		20		mV
Zero-scale transition error		Gain = 0dB; AGAIN[4:0] = 02(hex) DGAIN[11:0] = 6AB(hex)		20		mV
Differential non-linearity	DNL	10-bit		0.5		LSB
Integral non-linearity (pk-pk/2)	INL	10-bit		1		LSB
Channel to channel gain matching	Min Gain			5		%
	Max Gain			15		%
Output noise		Unity Gain (Unused channels grounded)		0.3		LSB rms
Channel to channel crosstalk		10-bit		+/-0.5		LSB
Programmable Gain Amplifier						
Total Resolution (Ga + Gd)	GT			12		bits
Analogue Gain	Ga		0.6 + 0.3 * AGAIN[4:0]			V/V
Max gain, each channel (Ga)	Ga_{MAX}	AGAIN[4:0] = 1F(hex)		9.9		V/V
Min gain, each channel (Ga)	Ga_{MIN}	AGAIN[4:0] = 0(hex)		0.6		V/V
Digital Gain	Gd		DGAIN[11:0] / 2^{11}			V/V
Max gain, each channel (Gd)	Gd_{MAX}	DGAIN[11:0] = FFF(hex)		2		V/V
Min gain, each channel (Gd)	Gd_{MIN}	DGAIN[11:0] = 400 (hex)		0.5		V/V
Max gain, each channel (Ga + Gd)	GT_{MAX}	AGAIN[4:0] = 1F(hex) DGAIN[11:0] = FFF(hex)		19.8		V/V
Min gain, each channel (Ga + Gd)	GT_{MIN}	AGAIN[4:0] = 0(hex) DGAIN[11:0] = 400 (hex)		0.3		V/V
Analogue to Digital Converter						
Resolution				16		bits
Speed					70	MSPS

Notes:

1. **Full-scale input voltage** denotes the differential input signal amplitude (V_{IN}-VRLC in non-CDS mode, V_{IN}-RESET level in CDS mode) that can be gained to match the ADC full-scale input range.
2. **Input signal limits** are the limits within which each input voltage and VRLC reference must lie.

GENERAL CHARACTERISTICS

Test Conditions

AVDD = LDOVDD = DBVDD = 3.3V , AGND = LDOGND = DBGND= 0V, T_A = 25°C, MCLK= 35MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
References						
Upper reference voltage	V_{REF1C}	ADCFS=0 ADCFS=1		2.05 2.25		V V
Lower reference voltage	V_{REF3C}	ADCFS=0 ADCFS=1		1.25 1.05		V V
Input return bias voltage	V_{REF2C}			1.2		V
Diff. Reference voltage (VREF1C-VREF3C)	$V_{REF1C3C}$	ADCFS=0 ADCFS=1		0.8 1.2		V V
Output resistance VREF1C, VREF3C, VREF2C				1		Ω
VRLC/Reset-Level Clamp (RLC)						
RLC switching impedance				50		Ω
RLC short-circuit current				2		mA
RLC output resistance				2		Ω
RLC Hi-Z leakage current		VRLC = 0 to AVDD			1	µA
RLCDAC resolution				5		bits
RLCDAC step size	$V_{RLCSTEP}$	VRLC_TOP_SEL=0		0.09		V/step
	$V_{RLCSTEP}$	VRLC_TOP_SEL=1		0.048		V/step
RLCDAC output voltage at code 0(hex)	V_{RLCBOT}	VRLC_TOP_SEL=0, VRLC_VSEL[4:0]=00000		0.2		V
	V_{RLCBOT}	VRLC_TOP_SEL=1, VRLC_VSEL[4:0]=00000		0.11		V
RLCDAC output voltage at code 1F(hex)	V_{RLCTOP}	VRLC_TOP_SEL=0, VRLC_VSEL[4:0]=11111		3.0		V
	V_{RLCTOP}	VRLC_TOP_SEL=1, VRLC_VSEL[4:0]=11111		1.6		V
VRLC DNL				+/- 0.5		LSB
VRLC INL				+/- 0.5		LSB
Offset DAC, Monotonicity Guaranteed						
Resolution				8		bits
Differential non-linearity	DNL			0.1		LSB
Integral non-linearity	INL			0.75		LSB
Step size				2.04		mV/step
Output voltage		Code 00(hex) Code FF(hex)		-250 +250		mV mV
DIGITAL SPECIFICATIONS						
Digital Inputs						
High level input voltage	V_{IH}		0.7 * AVDD			V
Low level input voltage	V_{IL}				0.2 * AVDD	V
High level input current	I_{IH}				1	µA
Low level input current	I_{IL}				1	µA
Input capacitance	C_I			5		pF

Test Conditions
AVDD = LDOVDD = DBVDD = 3.3V , AGND = LDOGND = DBGND= 0V, T_A = 25°C, MCLK= 35MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMOS Outputs						
High level output voltage	V_{OH}	I_{OH} = 6mA	AVDD – 0.5			V
Low level output voltage	V_{OL}	I_{OL} = 1mA			0.5	V
High impedance output current	I_{OZ}				1	µA
TG Outputs						
High level output voltage	V_{OHTG}	I_{OH} = 1mA	AVDD – 0.5			V
Low level output voltage	V_{OLTG}	I_{OL} = 1mA			0.5	V
High impedance output current	I_{OZTG}	Grounded			1	µA
Digital IO Pins						
Applied high level input voltage	V_{IH}		0.7 * AVDD			V
Applied low level input voltage	V_{IL}				0.2 * AVDD	V
High level output voltage	V_{OH}	I_{OH} = 1mA	AVDD – 0.5			V
Low level output voltage	V_{OL}	I_{OL} = 1mA			0.5	V
Low level input current	I_{IL}				1	µA
High level input current	I_{IH}				1	µA
Input capacitance	C_I			5		pF
Output Impedance	Ro	Io = 1mA		38		Ω
High impedance output current	I_{OZ}				1	µA
LVDS Outputs						
Differential load impedance	RL		90	100	110	Ω
Differential steady-state output voltage magnitude	|VOD|	RL=100Ω	280		450	mV
Change in the steady-state differential output voltage magnitude between opposite binary states	Δ|VOD|	RL=100Ω			15	mV
Steady-state common-mode output voltage	VOC(SS)	RL=100Ω		1.25		V
Peak-to-peak common-mode output	VOC(PP)			20	50	mV
Short-circuit output current	IOS		–6		6	mA
High-impedance state output current	IOZ		–10		10	uA
Supply Currents						
		SF_INP=0, SF_VRLC=0		350		mA
		SF_INP=1, SF_VRLC=1		390		mA
Total supply current – full power down mode				1.0		mA

Notes:

1. **Full-scale input voltage** denotes the differential input signal amplitude (V_{IN}-VRLC in non-CDS mode, V_{IN}-RESET level in CDS mode) that can be gained to match the ADC full-scale input range.
2. **Input signal limits** are the limits within which each input voltage and VRLC reference must lie.

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS

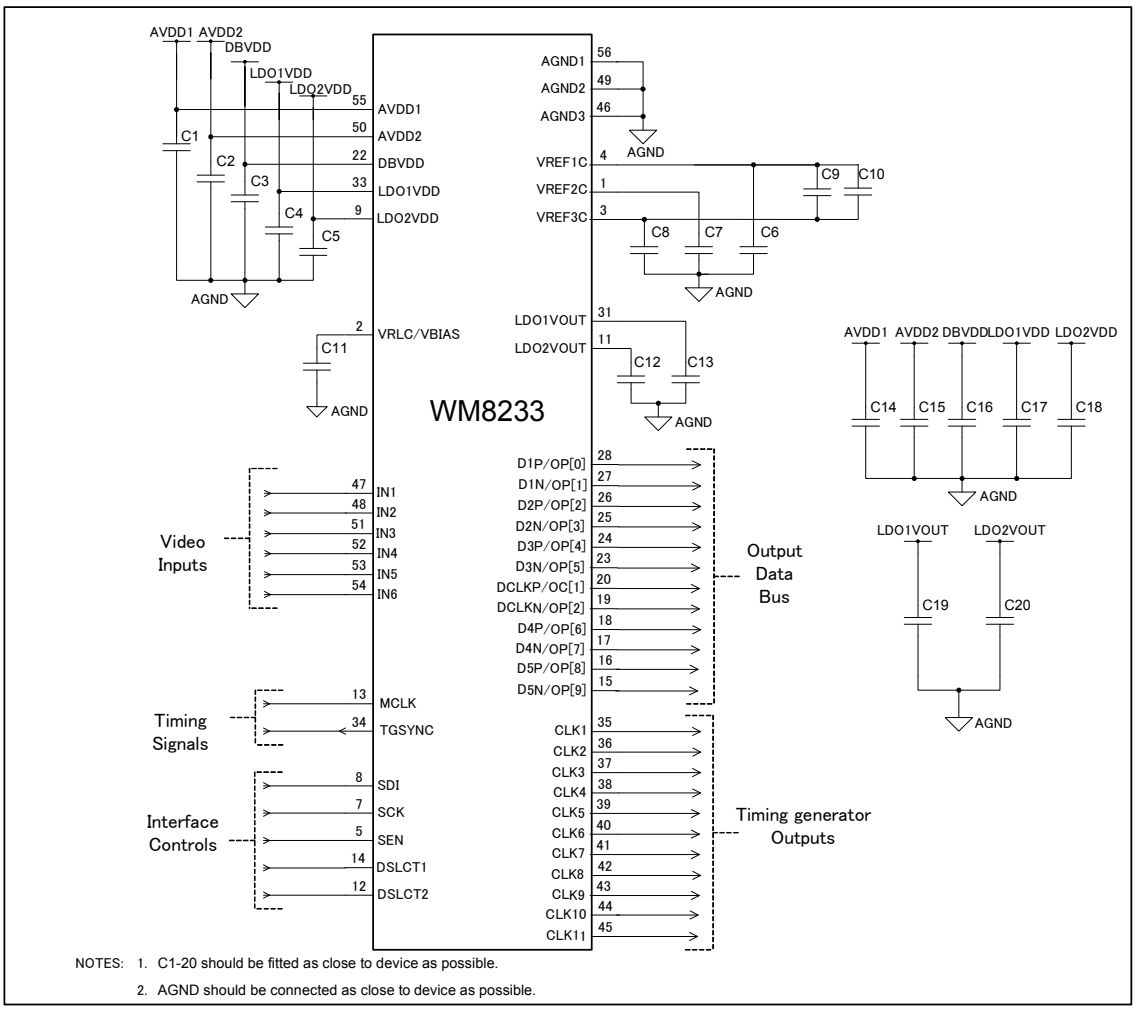


Figure 1 External Components Diagram

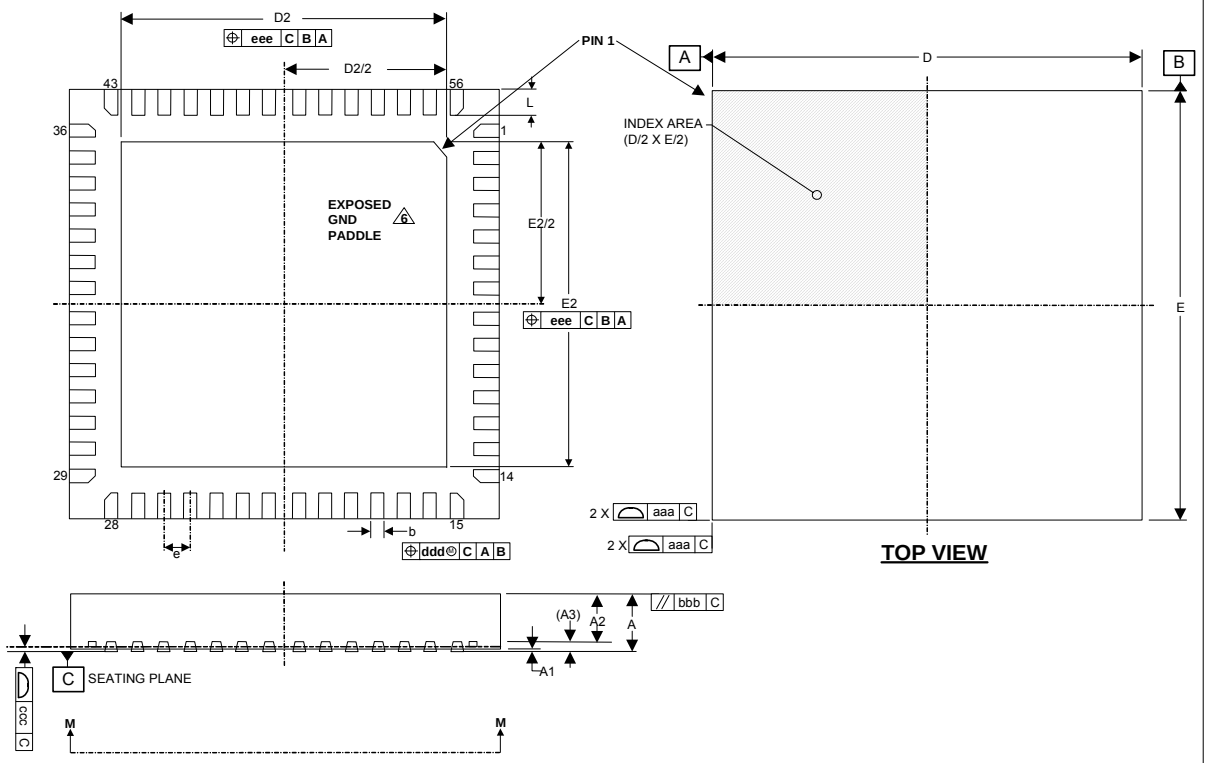
RECOMMENDED EXTERNAL COMPONENT VALUES

COMPONENT REFERENCE	SUGGESTED VALUE	DESCRIPTION
C1	0.1uF	De-coupling for AVDD1
C2	0.1uF	De-coupling for AVDD2
C3	0.1uF	De-coupling for DBVDD
C4	0.1uF	De-coupling for LDO1VDD
C5	0.1uF	De-coupling for LDO2VDD
C6	0.1uF	De-coupling for VREF1C
C7	0.1uF	De-coupling for VREF2C
C8	0.1uF	De-coupling for VREF3C
C9	0.01uF	High frequency decoupling between VREF1C and VREF3C
C10	10uF	Low frequency decoupling between VREF1C and VREF3C
C11	1uF	De-coupling for VRLC/VBIAS
C12	1uF	De-coupling for LDO1VOUT
C13	1uF	De-coupling for LDO2VOUT
C14	10uF	Reservoir capacitor for AVDD1
C15	10uF	Reservoir capacitor for AVDD2
C16	10uF	Reservoir capacitor for DBVDD
C17	10uF	Reservoir capacitor for LDO1VDD
C18	10uF	Reservoir capacitor for LDO2VDD
C19	10uF	Reservoir capacitor for LDOOUT
C20	10uF	Reservoir capacitor for LDOOUT

Table 1 External Components Description

PACKAGE DIMENSIONS

FL: 56 PIN QFN PLASTIC PACKAGE 8 x 8 x 0.85 mm BODY, 0.50 mm LEAD PITCH **DM091.B**



Symbols	Dimensions (mm)			
	MIN	NOM	MAX	NOTE
A	0.8	0.85	0.9	
A1	0	0.035	0.05	
A2	-	0.65	0.67	
A3		0.203 REF		
b	0.20	0.25	0.30	1
D		8.00 BSC		
D2	5.95	6.05	6.15	
E		8.00 BSC		
E2	5.95	6.05	6.15	
e		0.5 BSC		
L	0.35	0.4	0.45	
Tolerances of Form and Position				
aaa	0.10			
bbb	0.10			
ccc	0.08			
ddd	0.10			
eee	0.10			
REF	JEDEC, MO-220, VARIATION VLLD-2			

NOTES:
1. **DIMENSION b APPLIED TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 mm AND 0.30 mm FROM TERMINAL TIP.**
2. **ALL DIMENSIONS ARE IN MILLIMETRES**
3. **THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-002.**
4. **COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.**
5. **THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.**
6. **REFER TO APPLICATIONS NOTE WAN_0118 FOR FURTHER INFORMATION.**

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REVISION HISTORY

DATE	REV	ORIGINATOR	CHANGES
16/11/10	1.0	NB	First Release
09/02/12	3.0	JMacD	Current consumption updated to 350mA DAC description updated from 4-bit to 8-bit Temperature range updated to -40 Updated ADCFS characteristics Updated RLCDAC resolution Updated Parameter Name and Register name for RLCDAC Added test condition for TG output Updated Supply currents
29/02/12	3.0	JMacD	Recommended External Component Values – C9 value updated to 0.01uF