



LB1991V — Monolithic Digital IC For Fan Motor 3-phase Brushless Motor Driver

Overview

The LB1991V is a 3-phase brushless motor driver IC that is optimal for driving the DC fan motor.

Functions

- 3-phase full-wave voltage drive technique (120° voltage-linear technique)
- Torque ripple correction circuit (overlap correction)
- Speed control technique based on motor voltage and current control
- Built-in FG comparators
- Built-in thermal shutdown circuit

Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC1 \text{ max}}$		10	V
	$V_{CC2 \text{ max}}$		11	V
	$V_S \text{ max}$		11	V
Applied output voltage	$V_O \text{ max}$		V_S+2	V
Maximum output current	$I_O \text{ max}$		1.0	A
Allowable power dissipation	$P_d \text{ max}$	Independent IC	440	mW
Operating temperature	T_{opr}		-20 to +75	$^\circ\text{C}$
Storage temperature	T_{stg}		-55 to +150	$^\circ\text{C}$

Allowable Operating Ranges at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC1}	$V_{CC1} \leq V_{CC2}$	2.7 to 6.0	V
	V_{CC2}		3.5 to 9.0	V
	V_S		Up to V_{CC2}	V
Hall input amplitude	V_{HALL}	Between Hall effect element inputs	± 20 to ± 80	mVp-p

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Electrical Characteristics at Ta = 25°C, VCC1 = 3V, VCC2 = 4.75V, VS = 1.5V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply Current						
VCC1 current drain	ICC1	IOUT = 100mA		3	5	mA
VCC2 current drain	ICC2	IOUT = 100mA		7.0	10.0	mA
VCC1 quiescent current	ICC1Q	VSTBY = 0V		1.5	3.0	mA
VCC2 quiescent current	ICC2Q	VSTBY = 0V			100	μA
VS quiescent current	ISQ	VSTBY = 0V		75	100	μA
VX1						
High side residual voltage	VXH1	IOUT = 0.2A	0.15	0.22	0.29	V
Low side residual voltage	VXL1	IOUT = 0.2A	0.15	0.20	0.25	V
VX2						
High side residual voltage	VXH2	IOUT = 0.5A		0.25	0.40	V
Low side residual voltage	VXL2	IOUT = 0.5A		0.25	0.40	V
Output saturation voltage	VO(sat)	IOUT = 0.8A, Sink + Source			1.4	V
Overlap	O.L	RL = 39Ω × 3, Rangle = 20kΩ *2	72	80	87	%
High/low overlap difference	ΔO.L	(Average upper side overlap) – (Average lower side overlap) *2	-8		+8	%
Hall Amplifiers						
Input offset voltage	VHOFF	Design target *1	-5		+5	mV
Common-mode input voltage range	VHCM	Rangle = 20kΩ	0.95		2.1	V
I/O voltage gain	VG VH	Rangle = 20kΩ	25.5	28.5	31.5	dB
Standby Pin						
High-level voltage	VSTH		2.5			V
Low-level voltage	VSTL				0.4	V
Input current	I _{STIN}	VSTBY = 3V		25	40	μA
Leakage current	I _{STLK}	VSTBY = 0V			-30	μA
FRC Pin						
High-level voltage	VFRCH		2.5			V
Low-level voltage	VFRCL				0.4	V
Input current	I _{FRCIN}	VFRC = 3V		25	30	μA
Leakage current	I _{FRCLK}	VFRC = 0V			-30	μA
VH						
Hall supply voltage	VHALL	I _H = 5mA, VH(+) – VH(-)	0.85	0.95	1.05	V
(-) pin voltage	VH(-)	I _H = 5mA	0.81	0.88	0.95	V
FG Comparator						
Input offset voltage	VFGOFF		-3		+3	mV
Input bias voltage	I _{bFG}	VFGIN ⁺ = VFGIN ⁻ = 1.5V			500	nA
Input bias current offset	ΔI _{bFG}	VFGIN ⁺ = VFGIN ⁻ = 1.5V	-100		+100	nA
Common-mode input voltage range	VFGCM		1.2		2.5	V
Output high-level voltage	VFGOH	At the internal pull-up resistors	2.8			V
Output low-level voltage	VFGOL	At the internal pull-up resistors			0.2	V
Voltage gain	VGFG	Design target *1		100		dB
Output current (sink)	I _{FGOS}	For the output pin low level			5	mA
Thermal shutdown						
Operating temperature	TSD	Design target *1		180		°C
Temperature hysteresis	ΔTSD	Design target *1		20		°C

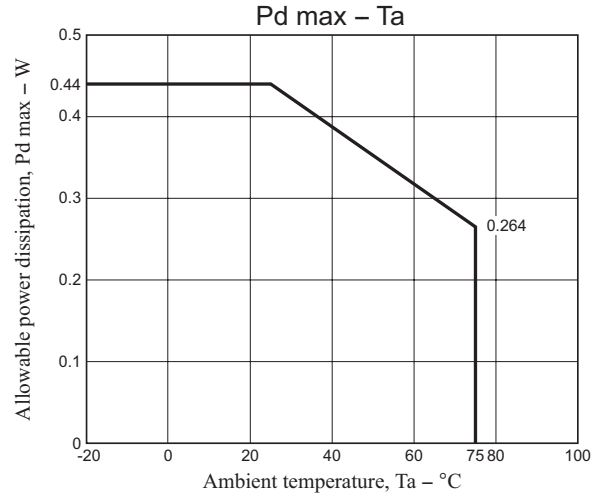
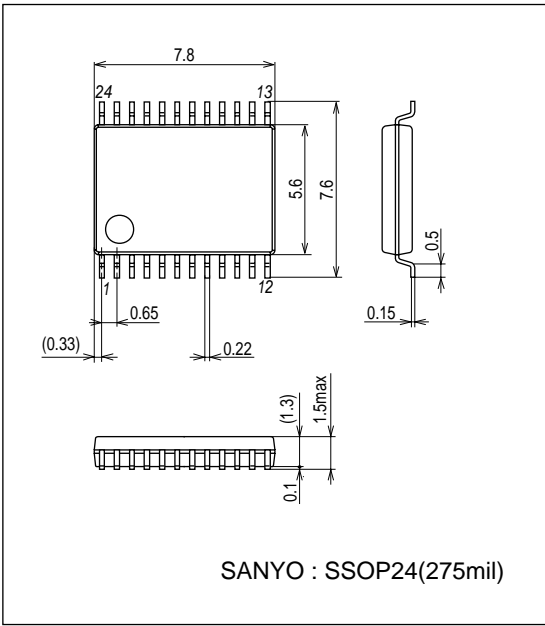
*1: Design target values in the conditions column are not tested.

*2: The standard for overlap is the value as measured.

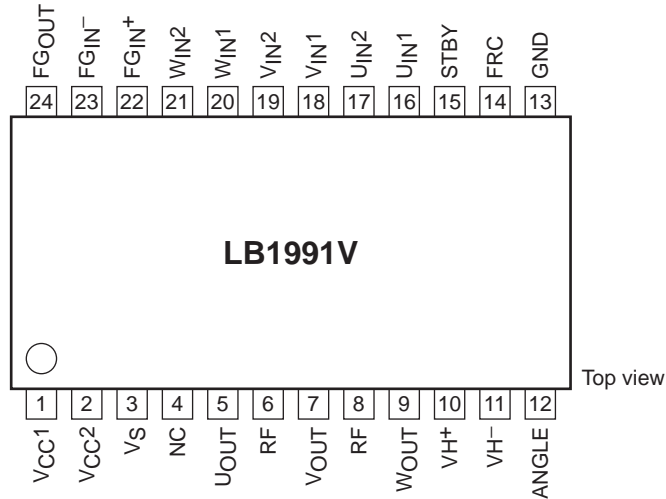
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Package Dimensions

unit : mm (typ)
3175C



Pin Assignment

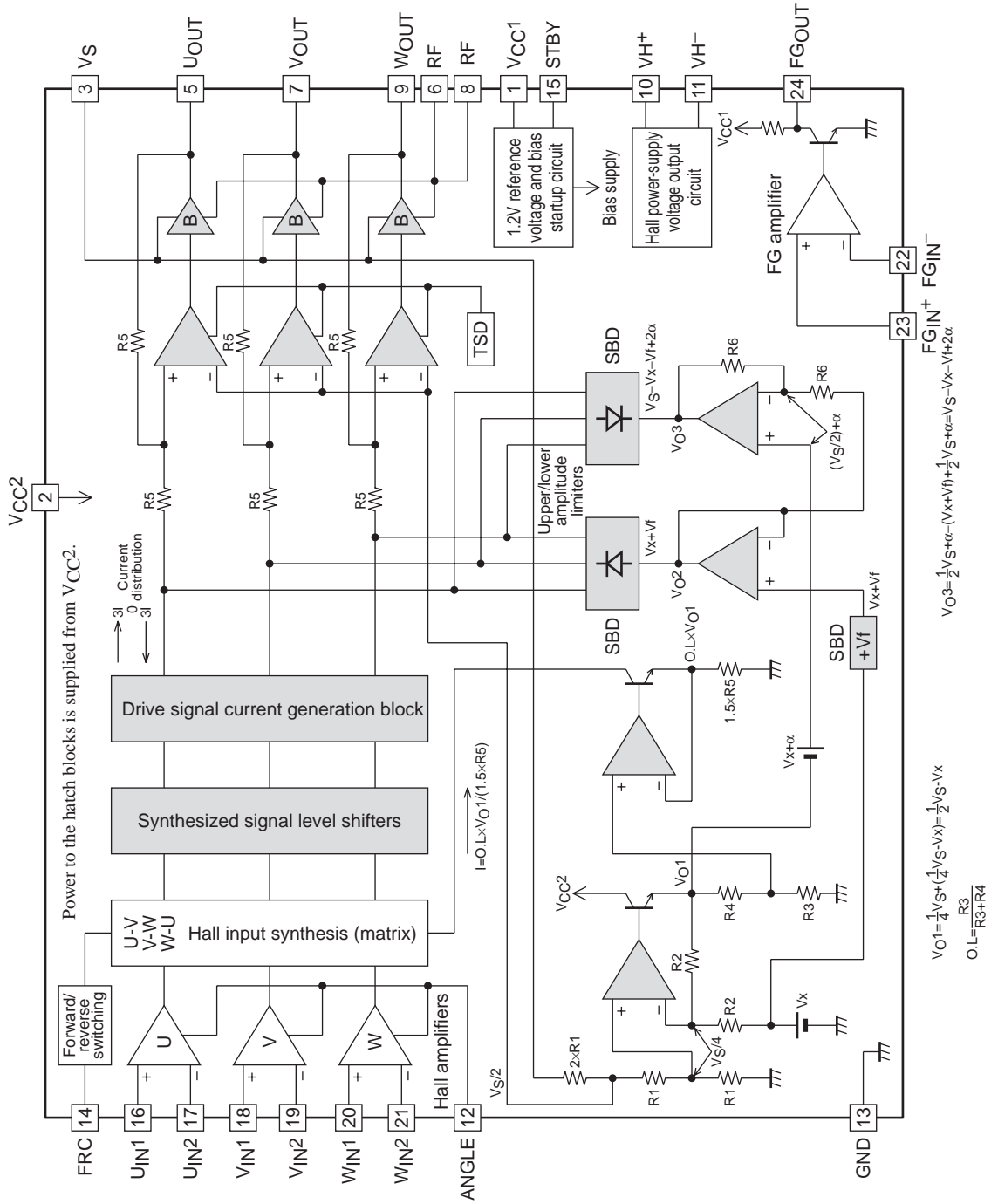


Truth Table

	Source phase → Sink phase	Hall input			FRC
		U	V	W	
1	V → W	H	H	L	H
	W → V	H	H	L	L
2	U → W	H	L	L	H
	W → U	H	L	L	L
3	U → V	H	L	H	H
	V → U	H	L	H	L
4	W → V	L	L	H	H
	V → W	L	L	H	L
5	W → U	L	H	H	H
	U → W	L	H	H	L
6	V → U	L	H	L	H
	U → V	L	H	L	L

Note: The "H" entries in the FRC column indicate a voltage of 2.50V or higher, and the "L" entries indicate a voltage of 0.4V or lower. (When V_{CC1} is 3V.)
At the Hall inputs, for each phase a high-level input is the state where the (+) input is 0.02V or higher than the (-) input. Similarly, a low-level input is the state where the (+) input is 0.02V or lower than the (-) input.

Block Diagram

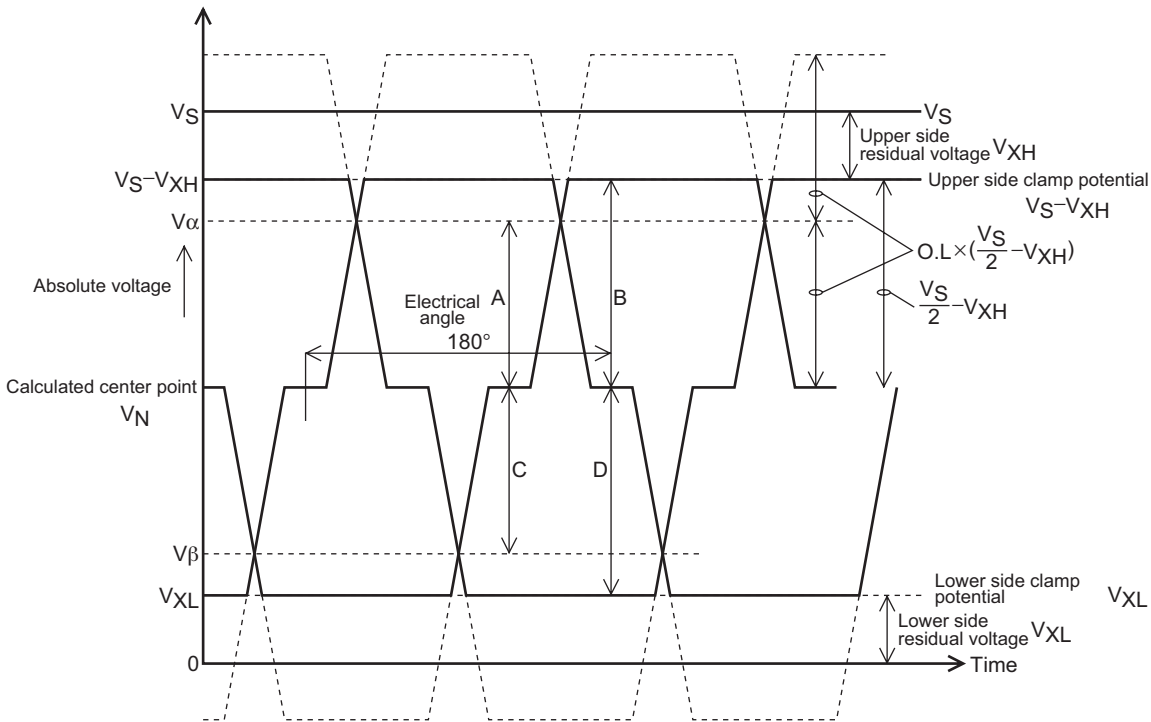


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Pin Function

Pin No.	Pin name	Pin function	Equivalent circuit
1	V _{CC1}	Supply voltage for all circuits other than the IC internal output block and the amplitude control block.	
2	V _{CC2}	Supply voltage for the IC internal output control block and the amplitude control block.	
3	V _S	Motor drive power supply. The voltage applied to this pin must not exceed V _{CC2} .	
5	U _{OUT}	U phase output.	
7	V _{OUT}	V phase output.	
9	W _{OUT}	W phase output. (These outputs include built-in spark killer diodes.)	
6,8	RF	Ground for the output power transistors.	
10	VH ⁺	Hall element bias voltage supply. A voltage that is typically 0.95V is generated between the VH ⁺ and VH ⁻ pins (When I _H is 5mA).	
11	VH ⁻		
13	GND	Ground for circuits other than the output transistor. The RF pin potential is the lowest output transistor potential.	
14	FRC	Forward/reverse selection. Applications can select motor forward or reverse direction rotation using this pin. (This pin has hysteresis characteristics.)	
15	STBY	Selects the bias supply for all circuits other than the FG comparators. The bias supply is cut when this pin is set to the low level.	
16	U _{IN1}	U phase Hall element input.	
17	U _{IN2}	The logic high level is the state where the IN ⁺ voltage is greater than the IN ⁻ voltage.	
18	V _{IN1}	V phase Hall element input.	
19	V _{IN2}	The logic high level is the state where the IN ⁺ voltage is greater than the IN ⁻ voltage.	
20	W _{IN1}	W phase Hall element input.	
21	W _{IN2}	The logic high level is the state where the IN ⁺ voltage is greater than the IN ⁻ voltage.	
12	ANGLE	Hall input/output gain control. The gain is controlled by the resistor connected between this pin and ground.	
22	FG _{IN} ⁺	FG comparator non-inverting inputs. There is no internally applied bias.	
23	FG _{IN} ⁻	FG comparator inverting inputs. There is no internally applied bias.	
24	FG _{OUT}	FG comparator outputs. There is an internal 20kΩ resistor load.	

Overlap Generation and Calculation Method



Overlap Generation

Since the voltage generated in the amplitude control block is, taking the center point as the reference, $2 \times \langle \text{overlap} \rangle \times (1/2 V_S - V_X)$ on one side, the intersection point of the waveform will be $\langle \text{overlap} \rangle \times (1/2 V_S - V_X)$ from the center point.

To clamp that waveform at $(1/2 V_S - V_X)$ referenced to the center point the overlap must be:

$$A/B \times 100 = \langle \text{overlap} \rangle \times 100 (\%)$$

Overlap Calculation

- Upper side overlap

$$\text{Calculated center point: } V_N = \frac{(V_S - V_{XH} - V_{XL})}{2} + V_{XL} = \frac{(V_S - V_{XH} + V_{XL})}{2}$$

Since $A = V_\alpha - V_N$, $B = V_S - V_{XH} - V_N$, the upper side overlap will be:

$$\langle \text{overlap} \rangle = \frac{A}{B} = \frac{V_\alpha - ((V_S - V_{XH} + V_{XL})/2)}{V_S - V_{XH} - ((V_S - V_{XH} + V_{XL})/2)} \times 100$$

Which can be calculated as:

$$= \frac{2V_\alpha - (V_S - V_{XH}) - V_{XL}}{(V_S - V_{XH}) - V_{XL}} \times 100(\%)$$

- Lower side overlap

Since $C = V_N - V_\beta$, and $D = V_N - V_{XL}$, the lower side overlap will be:

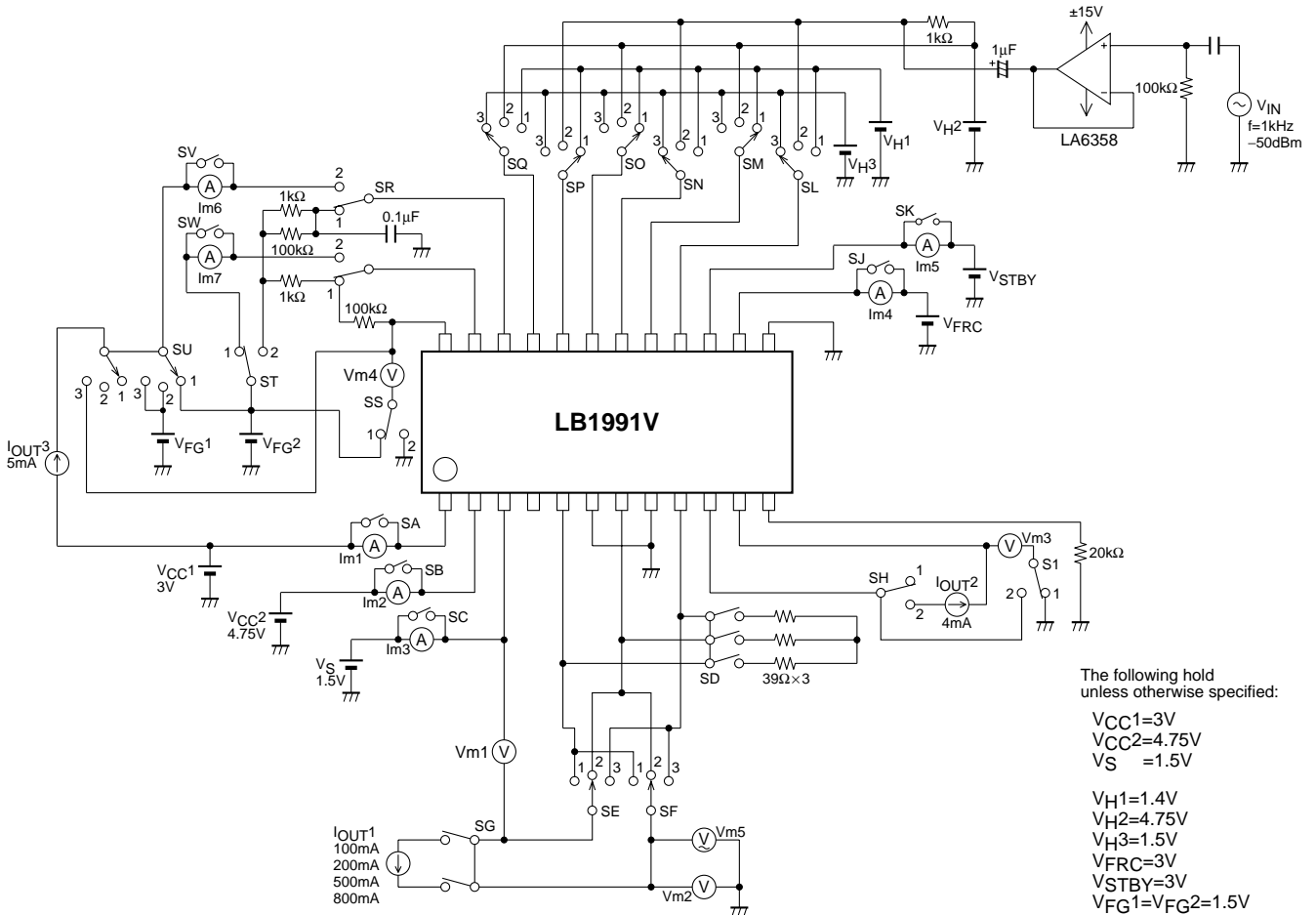
$$\langle \text{overlap} \rangle = \frac{C}{D} = \frac{((V_S - V_{XH} + V_{XL})/2) - V_\beta}{((V_S - V_{XH} + V_{XL})/2) - V_{XL}} \times 100$$

Which can be calculated as:

$$= \frac{(V_S - V_{XH}) + V_{XL} - 2V_\beta}{(V_S - V_{XH}) - V_{XL}} \times 100(\%)$$

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Test Circuit



The following hold unless otherwise specified:

VCC1=3V
VCC2=4.75V
VS =1.5V

VH1=1.4V
VH2=4.75V
VH3=1.5V
VFRC=3V
VSTBY=3V
VFG1=VFG2=1.5V

Switch status:
0 : CLOSED
X : OPEN

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