PRELIMINARY | Data Sheet | March 21, 2006 | FN6251.0

16x16 Video Crosspoint with Differential Inputs

The ISL59531 is a 16x16 integrated video crosspoint switch matrix with differential input and On-Screen Display (OSD) insertion. The ISL59531 is ideal for routing video signals in security and video-on-demand systems. This device operates from a single +5V supply. Any output of the 16 video inputs cable can be switched to any of the 16 outputs. OSD information can be inserted into any output through an internal, dedicated fast 2:1 mux (15ns switching times) located before the output buffer. Also, any input can be broadcast to all 16 outputs. Each output can be tri-stated and its gain set to +1 or +2 through the SPI interface.

The ISL59531 offers a -3dB signal bandwidth of 320MHz. The differential gain and differential phase of 0.025%, along with 0.1dB flatness out to 50MHz, making the ISL59531 suitable for many video applications.

The switch matrix configuration and output buffer gain are programmed through an SPI/QSPI™-compatible three-wire serial interface. The ISL59531 interface is set up to facilitate both fast updates and initialization. On power-up, all outputs are initialized in the disabled state to avoid output conflicts within the user system. The ISL59531 has single-supply signal operation. It can accommodate input common mode voltages from 0V to 3.5V and 0V to 4V at the outputs.

The ISL59531 is available in a 356-pin BGA package and specified over an extended -40°C to +85°C temperature range.

The ISL59530 is a single-ended input version of this device. For capacitor-coupled applications, the ISL59530 inputs include a clamp circuit that restores the input level to an externally applied reference.

Features

- 16x16 non-blocking switch with differential inputs and outputs
- Operates from a single +5V supply
- Output gain switchable +1 or +2
- SPI digital interface
- Tri-state output
- -90dB Isolation at 6MHz
- 0.025%/0.05° dG/dP
- Pb-free plus anneal available (RoHS compliant)

Applications

- Security camera switching
- RGB routing
- HDTV routing

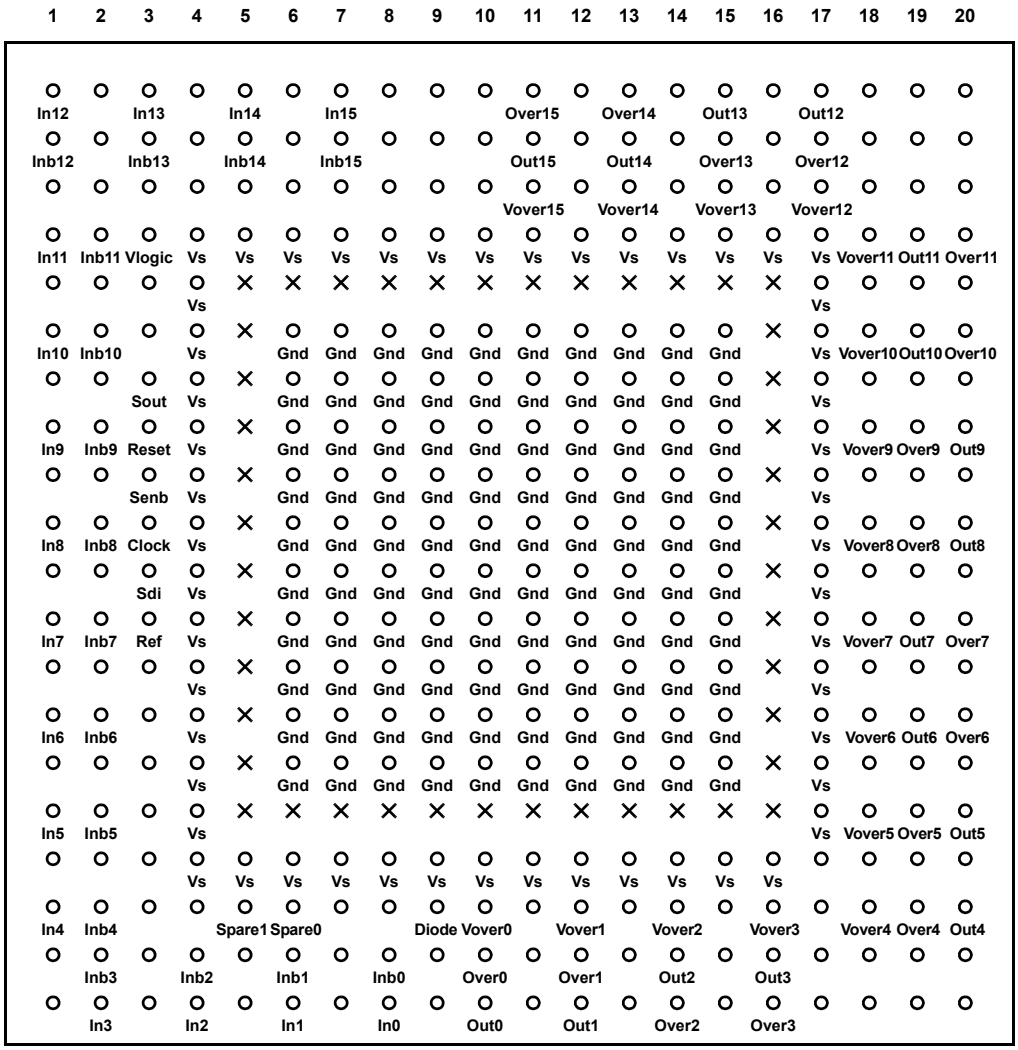
Ordering Information

PART NUMBER	TAPE & REEL	PACKAGE	PKG. DWG. #
ISL59531IKZ (See Note)	-	356-Pin BGA (Pb-free)	V356.27x27

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinout

ISL59531
(356-PIN BGA)
TOP VIEW



× = Empty location (unpopulated)
○ = Ballgrid

Pad name "GND" is the same as package or ball name "ground" or "G"
Pad name "VS" is the same as package or ball name "power" or "P"
Pad X, Y is from pad center. All pads are 70µ by 70µ

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage between V_S and GND 5.5V
Maximum Continuous Output Current 40mA
Ambient Operating Temperature . . . . . .-40°C to +85°C
Maximum Die Temperature . . . . . .+125°C
Storage Temperature . . . . . .-65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

DC Electrical Specifications V_S = 5V

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
V_S	Supply Range		4.5		5.5	V
V_D	Digital Supply	Establishes serial output high level	1.2		5.5	V
A_V	Gain	A_V = 1, R_L = 500Ω	0.97	1	1.03	V/V
		A_V= 2, R_L = 150Ω	1.94	2	2.06	V/V
GM	Gain Matching (to average of all other outputs)	A_V = 1	-1.5	1	1.5	%
		A_V = 2		0.5	1.0	%
V_{IN}	Input Voltage Range	A_V = 1	0		3.5	V
V_{OUT}	Output Voltage Range	A_V = 2, R_L = 150Ω	0		4.0	V
I_B	Input Bias Current		-10	-5	0	µA
V_{OS}	Output Offset Voltage	A_V = 1	-25	0	25	mV
		A_V = 2	-70	0	70	mV
I_{OUT}	Output Current	Sourcing, R_L = 10Ω to GND	60	100		mA
		Sinking, R_L to 2.5V	25	35		mA
PSRR	Power Supply Rejection Ratio			80		dB
I_S	Supply Current	Enabled, all outputs enable, no load current		312	375	mA
		Enable, all outputs disable, no load current		140		mA
		Disabled		0.8	1.1	mA
		Supply current per output channel		7		mA

AC Electrical Specifications

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
BW -3dB	3dB Bandwidth	V_{OUT} = 200mV_{P-P}, A_V = 2		320		MHz
BW 0.1dB	0.1dB Bandwidth	V_{OUT} = 200mV_{P-P}, A_V = 2		50		MHz
SR	Slew Rate	V_{OUT} = 2V_{P-P}, A_V = 2	360	520		V/µs
T_S	Settling Time to 0.1%	V_{OUT} = 2V_{P-P}, A_V = 2		12		ns
Glitch	Switching Glitch, Peak	A_V = 1		40		mV
T_{over}	Overlay Delay Time	Beginning of output transition		6		ns
dG	Diff Gain	A_V = 2, R_L = 150Ω		0.025		%
dP	Diff Phase	A_V = 2, R_L = 150Ω		0.05		°
Xt	Hostile Crosstalk	6MHz		-85		dB
V_N	Input Noise Voltage			42		nV/√Hz

Pin Descriptions

NAME	NUMBER	DESCRIPTION
INB2	W4	Complementary input
IN2	Y4	Input
INB3	W2	Complementary input
IN3	Y2	Input
REF	M3	Output reference
GND	GND	Ground
SDI	L3	Serial data input
VS	VS	Power supply
INB4	V2	Complementary input
IN4	V1	Input
INB5	T2	Complementary input
IN5	T1	Input
VS	VS	Power supply
GND	GND	Ground
INB6	P2	Complementary input
IN6	P1	Input
INB7	M2	Complementary input
IN7	M1	Input
CLOCK	K3	Serial data clock
VS	VS	Power supply
SENB	J3	Serial enable-inverted
GND	GND	Ground
INB8	K2	Complementary input
IN8	K1	Input
INB9	H2	Complementary input
IN9	H1	Input
VS	VS	Power supply
GND	GND	Ground
INB10	F2	Complementary input
IN10	F1	Input
INB11	D2	Complementary input
IN11	D1	Input
RESET	H3	Reset input
VS	VS	Power supply
SOUT	G3	Serial data output
GND	GND	Ground
INB12	B1	Complementary input
IN12	A1	Input
INB13	B3	Complementary input

Pin Descriptions (Continued)

NAME	NUMBER	DESCRIPTION
IN13	A3	Input
INPUT TEST BAR	NONE	Manufacturing test pin - leave open
GND	GND	Ground
GND	GND	Ground
VS	VS	Power supply
VS	VS	Power supply
VLOGIC	D3	Logic power supply for serial output driver
INB14	B5	Complementary input
IN14	A5	Input
INB15	B7	Complementary input
IN15	A7	Input
VSL	VS	Power supply
VGL	GND	Ground
VS	VS	Power supply
GND	GND	Ground
OVER15	A11	Overlay logic control
VOVER15	C11	Overlay analog input
OUT15	B11	Output
OVER14	A13	Overlay logic control
VOVER14	C13	Overlay analog input
OUT14	B13	Output
GND	GND	Ground
VS	VS	Power supply
OUT13	A15	Output
VOVER13	C15	Overlay analog input
OVER13	B15	Overlay logic control
OUT12	A17	Output
VOVER12	C17	Overlay analog input
OVER12	B17	Overlay logic control
GND	GND	Ground
OUT TEST 3	NONE	Manufacturing test pin - leave open
VS	VS	Power supply
OVER11	D20	Overlay logic control
VOVER11	D18	Overlay analog input
OUT11	D19	Output
OVER10	F20	Overlay logic control
VOVER10	F18	Overlay analog input
OUT10	F19	Output

Pin Descriptions (Continued)

NAME	NUMBER	DESCRIPTION
GND	GND	Ground
VS	VS	Power supply
OUT9	H20	Output
VOVER9	H18	Overlay analog input
OVER9	H19	Overlay logic control
OUT8	K20	Output
VOVER8	K18	Overlay analog input
OVER8	K19	Overlay logic control
OUT TEST 2	NONE	Manufacturing test pin - leave open
GND	GND	Ground
VS	VS	Power supply
OVER7	M20	Overlay logic control
VOVER7	M18	Overlay analog input
OUT7	M19	Output
OVER6	P20	Overlay logic control
VOVER6	P18	Overlay analog input
OUT6	P19	Output
GND	GND	Ground
VS	VS	Power supply
OUT5	T20	Output
VOVER5	T18	Overlay analog input
OVER5	T19	Overlay logic control
OUT4	V20	Output
VOVER4	V18	Overlay analog input
OVER4	V19	Overlay logic control
VS	VS	Power supply
OUT TEST 1	NONE	Manufacturing test pin - leave open
GND	GND	Ground
OVER3	Y16	Overlay logic control
VOVER3	V16	Overlay analog input
OUT3	W16	Output
OVER2	Y14	Overlay logic control
VOVER2	V14	Overlay analog input
OUT2	W14	Output
VS	VS	Power supply
GND	GND	Ground
OUT1	Y12	Output
VOVER1	V12	Overlay analog input
OVER1	W12	Overlay logic control
OUT0	Y10	Output

Pin Descriptions (Continued)

NAME	NUMBER	DESCRIPTION
VOVER0	V10	Overlay analog input
OVER0	W10	Overlay logic control
VS	VS	Power supply
OUT TEST 0	NONE	Manufacturing test pin - leave open
GND	GND	Ground
IN0	Y8	Input
INB0	W8	Complementary input
IN1	Y6	Input
INB1	W6	Complementary input
DIODE	V9	Anode of a ground-connected diode: useful for measuring die temperature
VS	VS	Power supply
GND	GND	Ground
VS	VS	Power supply
GND	GND	Ground
SPARE0	V6	Not assigned-do not connect
SPARE1	V5	Not assigned-do not connect

Typical Performance Curves

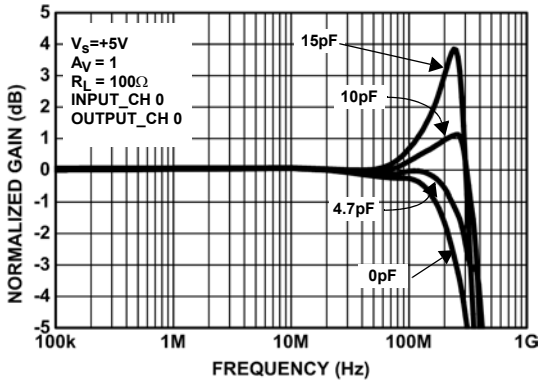


FIGURE 1. FREQUENCY RESPONSE - VARIOUS C_L, A_V = 1, MUX MODE

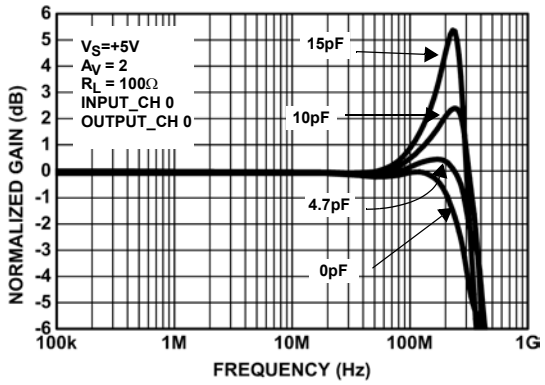


FIGURE 2. FREQUENCY RESPONSE - VARIOUS C_L, A_V = 2, MUX MODE

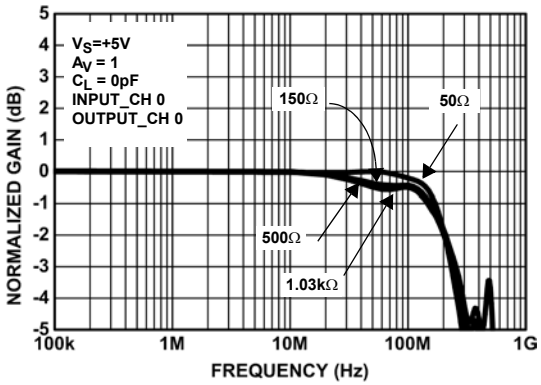


FIGURE 3. FREQUENCY RESPONSE - VARIOUS R_L, A_V = 1, MUX MODE

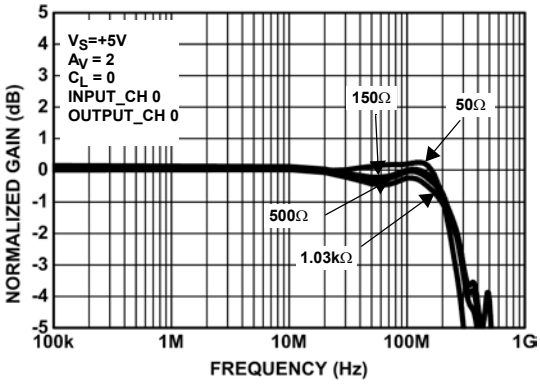


FIGURE 4. FREQUENCY RESPONSE - VARIOUS R_L, A_V = 2, MUX MODE

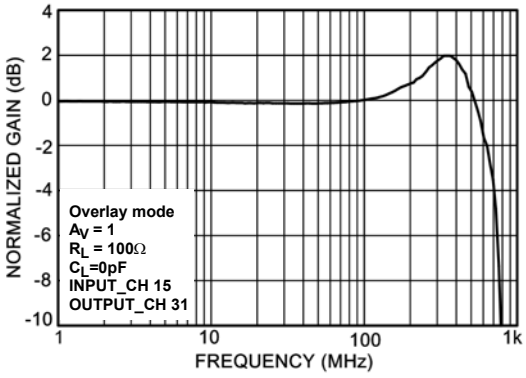


FIGURE 5. FREQUENCY RESPONSE - OVERLAY INPUT, A_V = 1

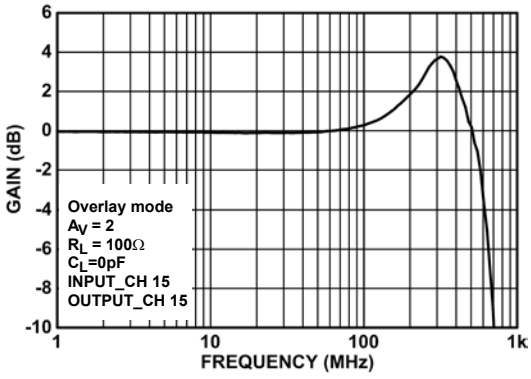


FIGURE 6. FREQUENCY RESPONSE - OVERLAY INPUT, A_V = 2

Typical Performance Curves (Continued)

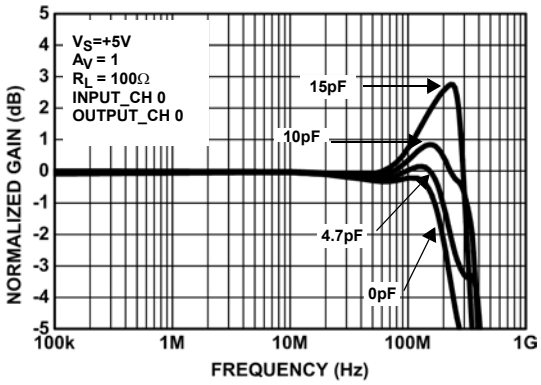


FIGURE 7. FREQUENCY RESPONSE - VARIOUS C_L, A_V = 1, BROADCAST MODE

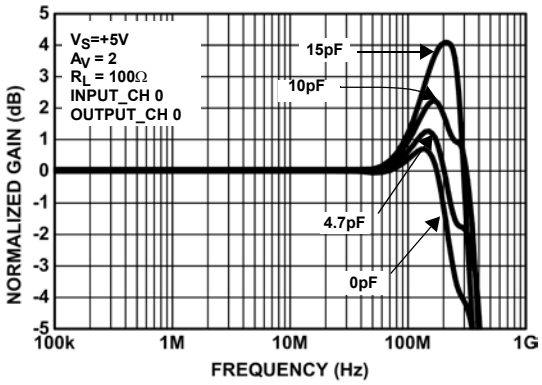


FIGURE 8. FREQUENCY RESPONSE - VARIOUS C_L, A_V = 2, BROADCAST MODE

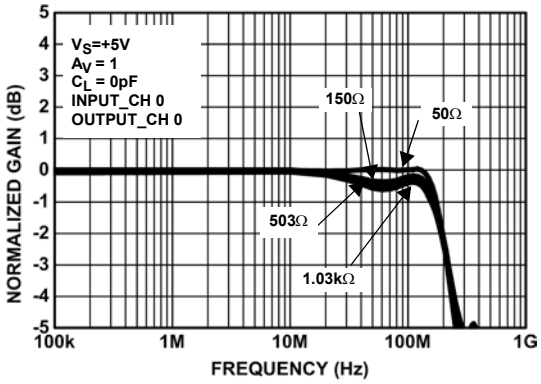


FIGURE 9A. FREQUENCY RESPONSE - VARIOUS R_L, A_V = 1, BROADCAST MODE

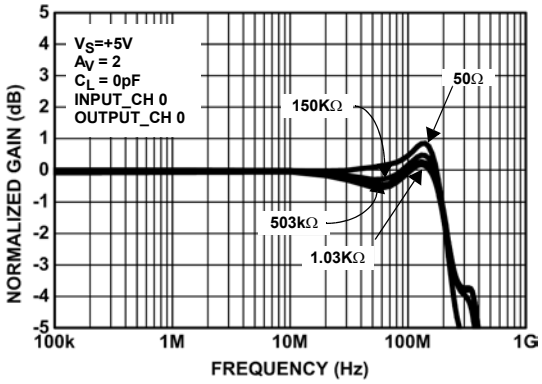


FIGURE 10. FREQUENCY RESPONSE - VARIOUS R_L, A_V = 2, BROADCAST MODE

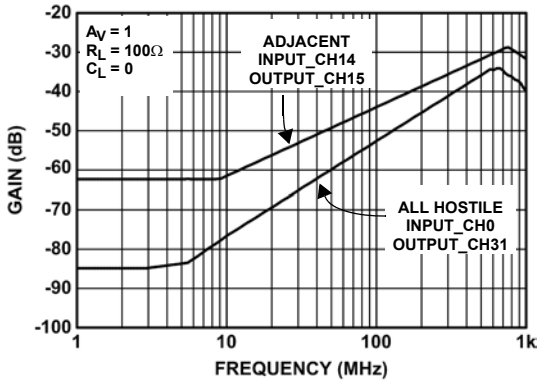


FIGURE 11. CROSSTALK - A_V = 1

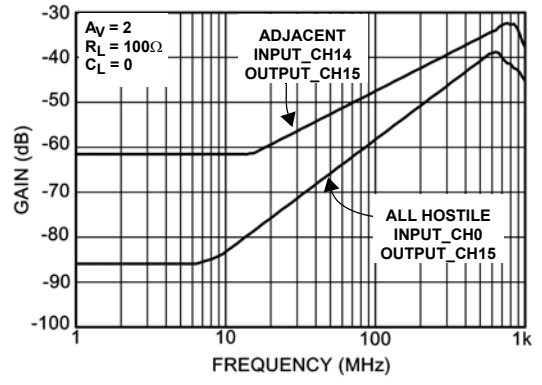


FIGURE 12. CROSSTALK - A_V = 2

Typical Performance Curves (Continued)

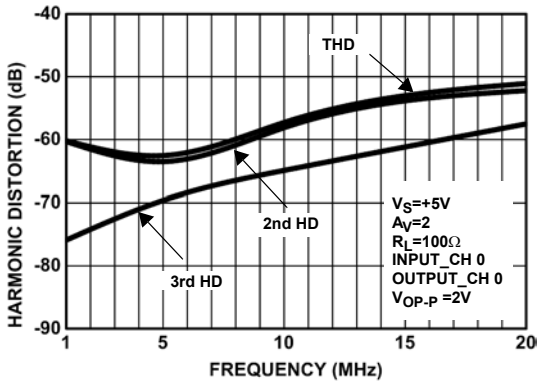


FIGURE 13. HARMONIC DISTORTION vs FREQUENCY

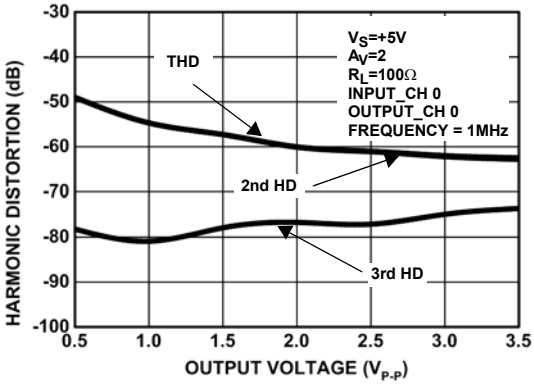


FIGURE 14. HARMONIC DISTORTION vs $V_{OUT\_P\text{-}P}$

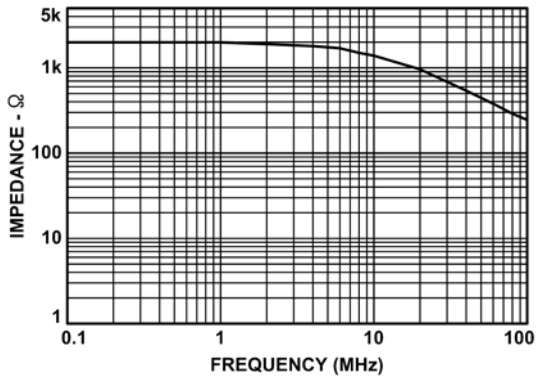


FIGURE 15. DISABLE OUTPUT IMPEDANCE

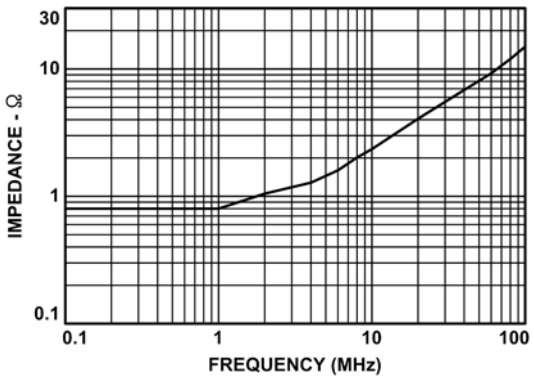


FIGURE 16. ENABLE OUTPUT IMPEDANCE

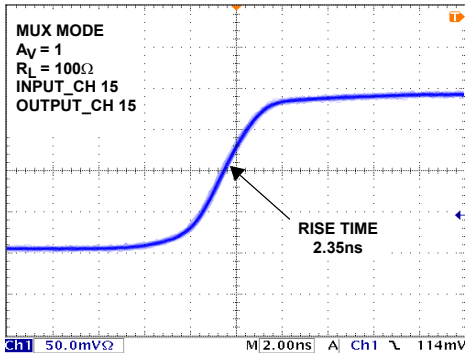


FIGURE 17. RISE TIME - A_V = 1

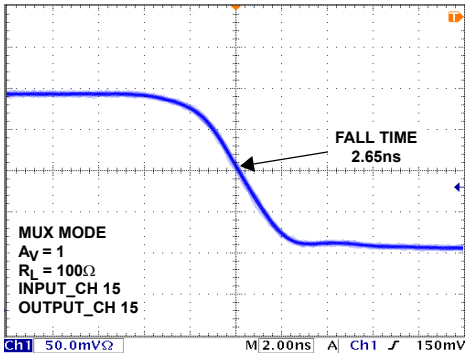


FIGURE 18. FALL TIME - A_V = 1

Typical Performance Curves (Continued)

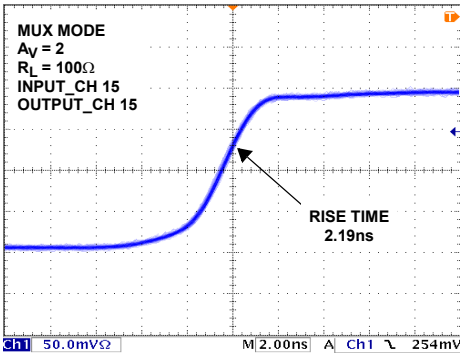


FIGURE 19. RISE TIME - A_V = 2

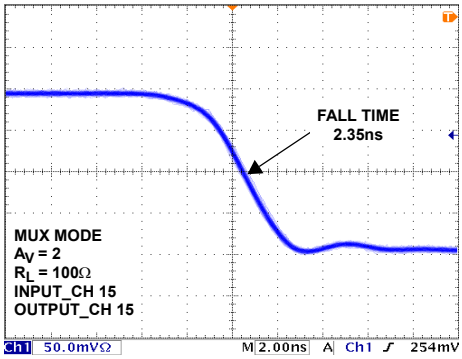


FIGURE 20. FALL TIME - A_V = 2

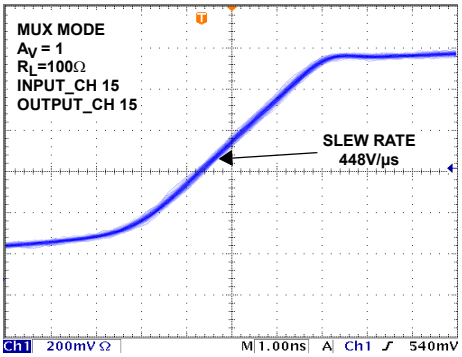


FIGURE 21. RISING SLEW RATE - A_V = 1

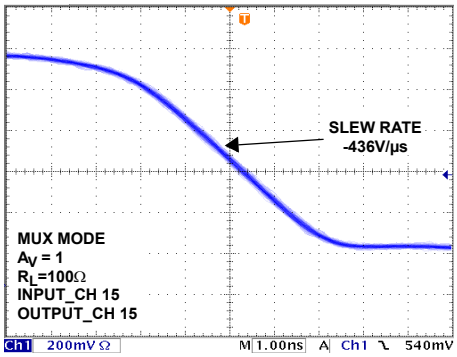


FIGURE 22. FALLING SLEW RATE - A_V = 1

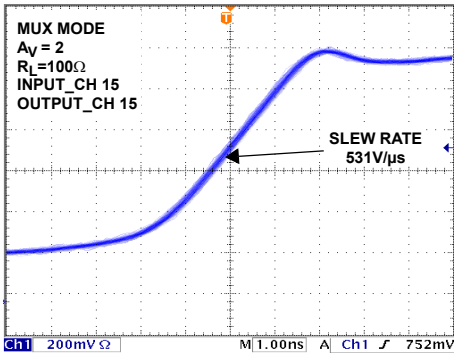


FIGURE 23. RISING SLEW RATE - A_V = 2

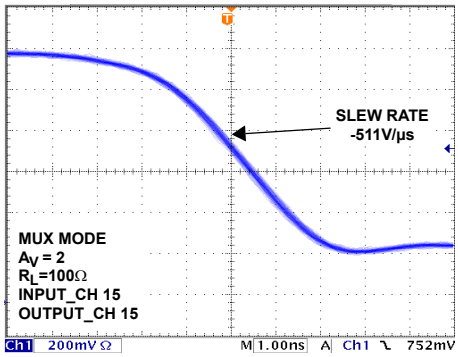


FIGURE 24. FALLING SLEW RATE - A_V = 2

Typical Performance Curves (Continued)

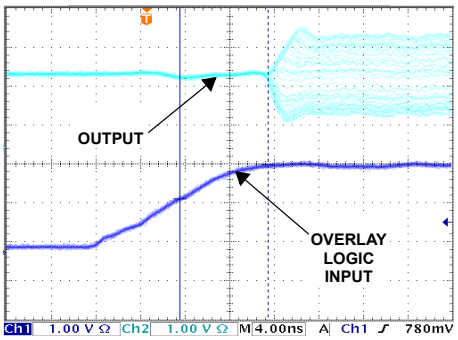


FIGURE 25. OVERLAY SWITCH TURN-ON DELAY TIME

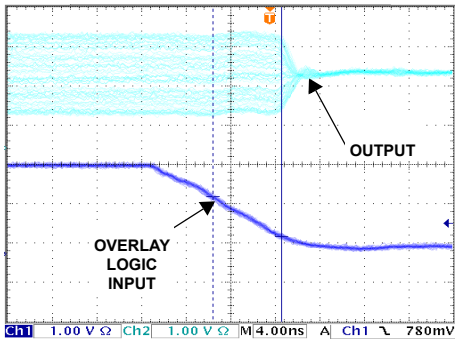


FIGURE 26. OVERLAY SWITCH TURN-OFF DELAY TIME

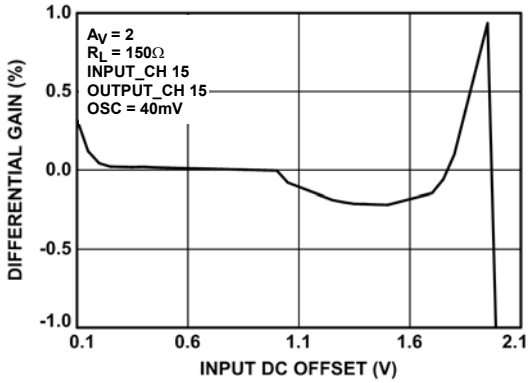


FIGURE 27. DIFFERENTIAL GAIN, A_V = 2

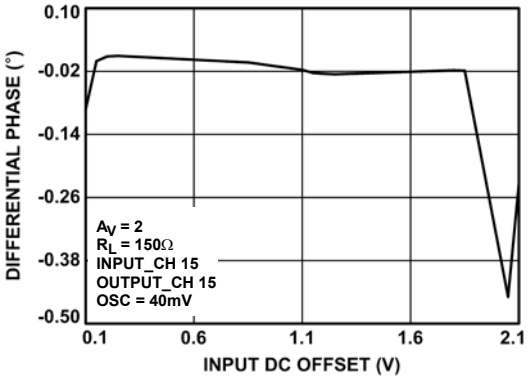


FIGURE 28. DIFFERENTIAL PHASE, A_V = 2

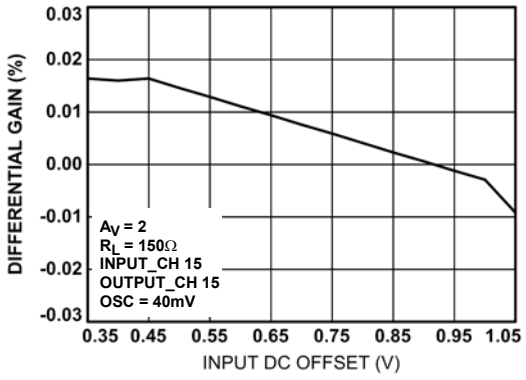


FIGURE 29. DIFFERENTIAL GAIN, A_V = 2

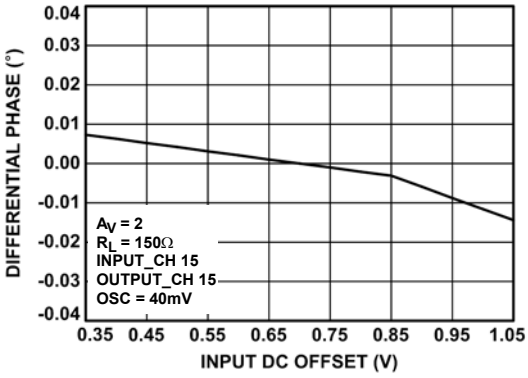


FIGURE 30. DIFFERENTIAL PHASE, A_V = 2

Typical Performance Curves (Continued)

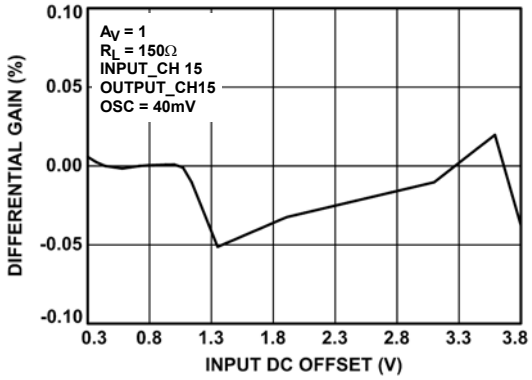


FIGURE 31. DIFFERENTIAL GAIN, A_V = 1

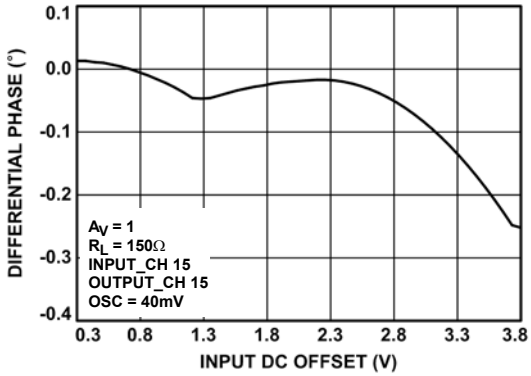


FIGURE 32. DIFFERENTIAL PHASE, A_V = 1

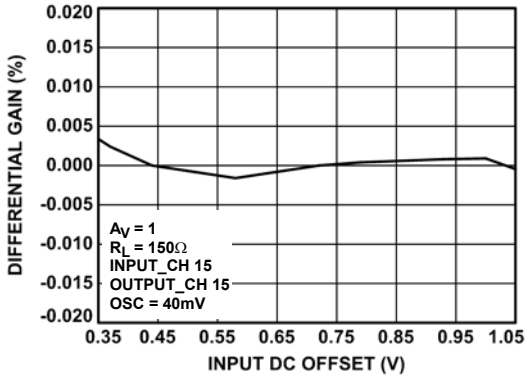


FIGURE 33. DIFFERENTIAL GAIN, A_V = 1

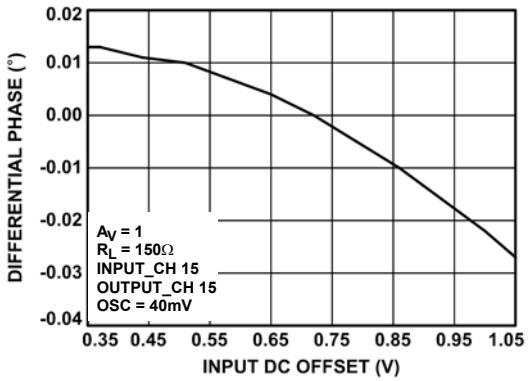


FIGURE 34. DIFFERENTIAL GAIN, A_V = 1

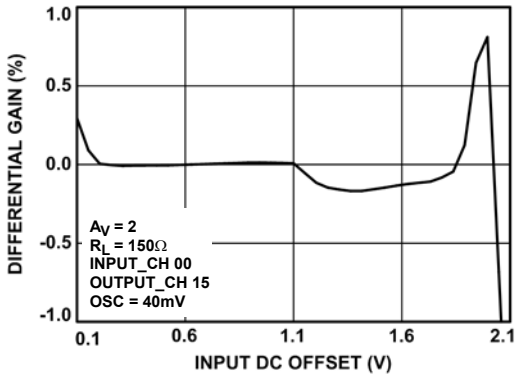


FIGURE 35. DIFFERENTIAL GAIN, A_V = 2

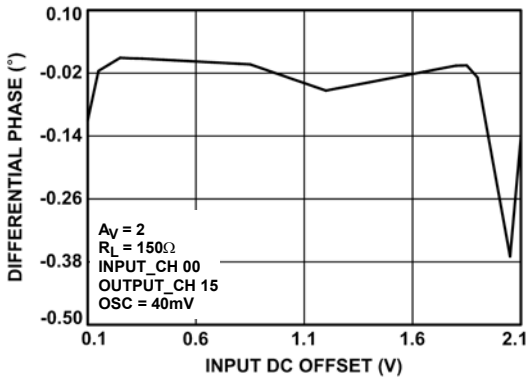


FIGURE 36. DIFFERENTIAL PHASE, A_V = 2

Typical Performance Curves (Continued)

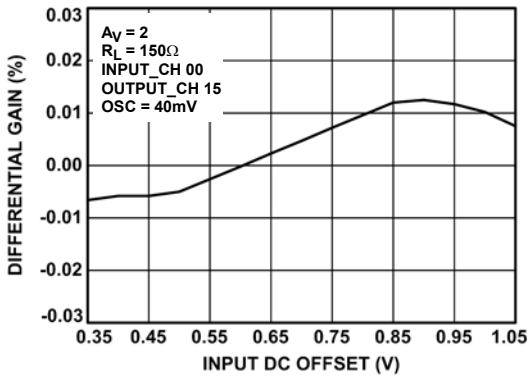


FIGURE 37. DIFFERENTIAL GAIN, A_V = 2

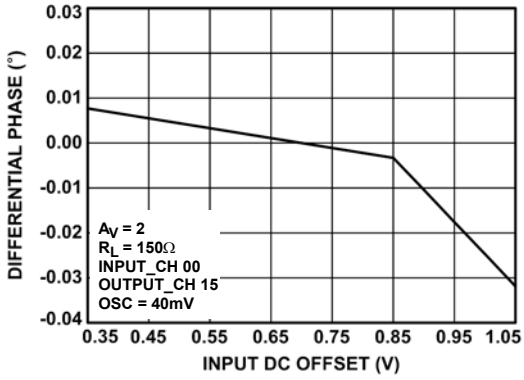


FIGURE 38. DIFFERENTIAL PHASE, A_V = 2

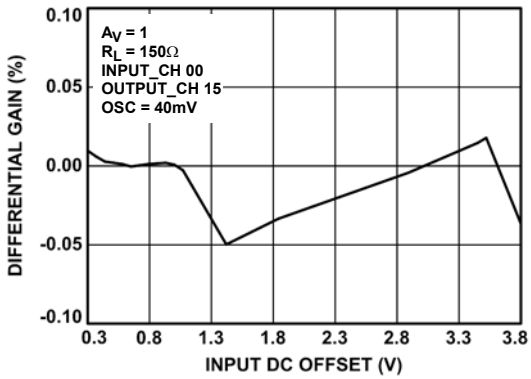


FIGURE 39. DIFFERENTIAL GAIN, A_V = 1

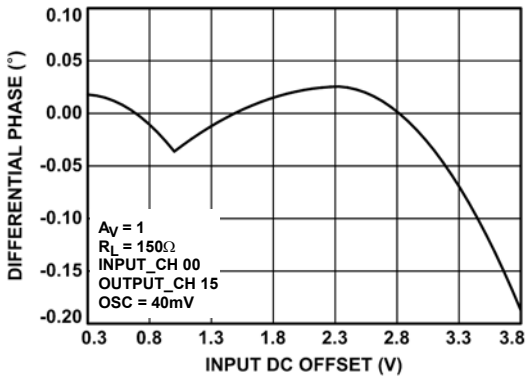


FIGURE 40. DIFFERENTIAL PHASE, A_V = 1

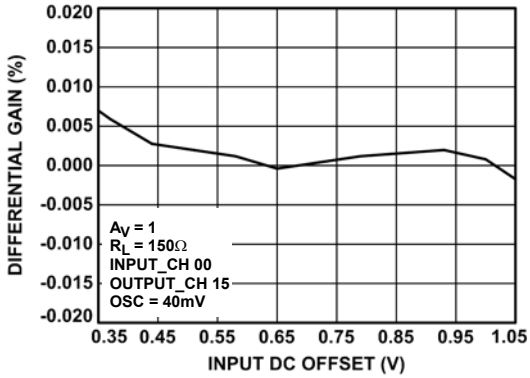


FIGURE 41. DIFFERENTIAL GAIN, A_V = 1

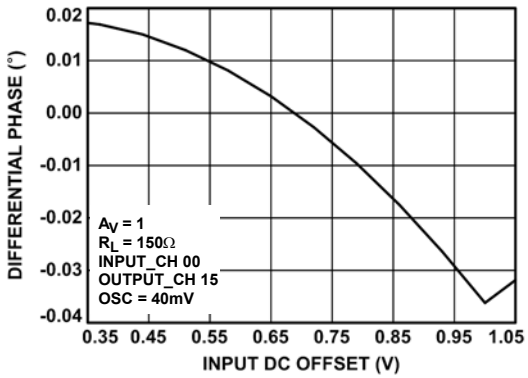


FIGURE 42. DIFFERENTIAL PHASE, A_V = 1

Typical Performance Curves (Continued)

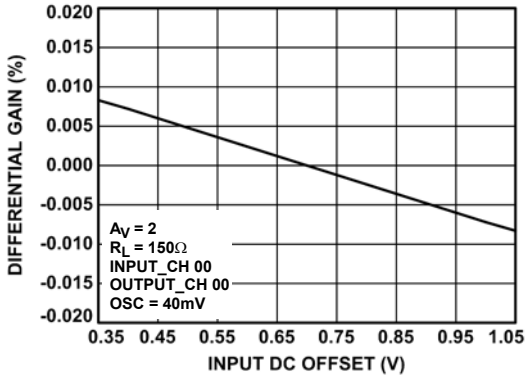


FIGURE 43. DIFFERENTIAL GAIN, OVERLAY, A_V = 2

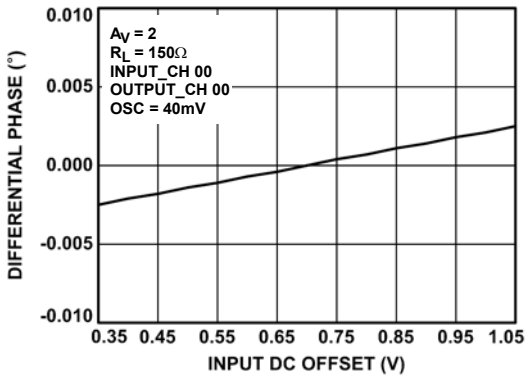


FIGURE 44. DIFFERENTIAL PHASE, OVERLAY, A_V = 2

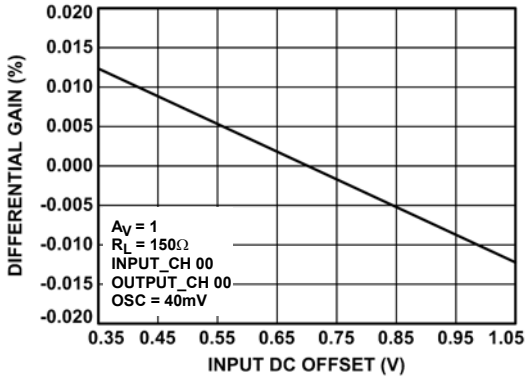


FIGURE 45. DIFFERENTIAL GAIN, OVERLAY, A_V = 1

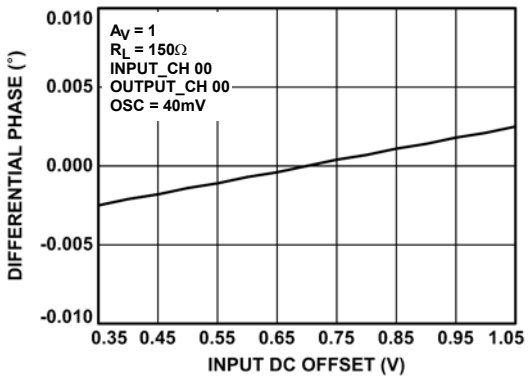


FIGURE 46. DIFFERENTIAL PHASE, OVERLAY, A_V = 1

3dB Bandwidth, MUX Mode, A_V = 1, R_L = 100Ω [MHz]

		INPUT CHANNELS															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
OUTPUT CHANNELS	0	255	229	229	210	222	221	224	190	169	152	233	190	212	189	207	166
	1	244	217						180	168						193	160
	2	257		235					186	171					204		169
	3	264			217				183	175				219			171
	4	255				220			174	177			202				167
	5	253					218		176	177		237					173
	6	247						226	171	178	157						170
	7	253	227	235	218	223	228	230	174	184	163	240	223	219	217	211	178
	8	255	236	240	239	223	236	231	175	187	168	241	242	222	235	213	183
	9	241						210	169	188	165						182
	10	235					236		168	186		230					185
	11	223				207			164	188			225				186
	12	220			209				161	192				205			185
	13	211		214					160	192					224		189
	14	199	212						160	194						197	193
	15	193	217	207	202	185	216	186	222	197	177	225	217	198	223	197	238

3dB Bandwidth, MUX Mode, A_V = 2, R_L = 100Ω [MHz]

		INPUT CHANNELS															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
OUTPUT CHANNELS	0	295	316	290	397	384	405	395	220	288	240	299	250	385	234	396	188
	1	268	290						211	183						291	183
	2	277		300					216	192					289		196
	3	279			408				213	196				392			196
	4	269				391			201	192			402				192
	5	263					407		201	196		298					200
	6	259						404	196	196	283						200
	7	263	411	307	402	387	412	398	201	205	407	307	402	387	413	398	211
	8	262	407	308	402	383	412	394	203	212	411	300	403	385	415	394	216
	9	253						388	194	210	410						214
	10	253					417		194	215		293					216
	11	246				385			187	213			412				217
	12	241			412				184	216				391			225
	13	236		272					182	220					419		225
	14	233	279						178	220						396	230
	15	227	274	244	396	367	407	230	183	223	324	276	400	379	413	385	293

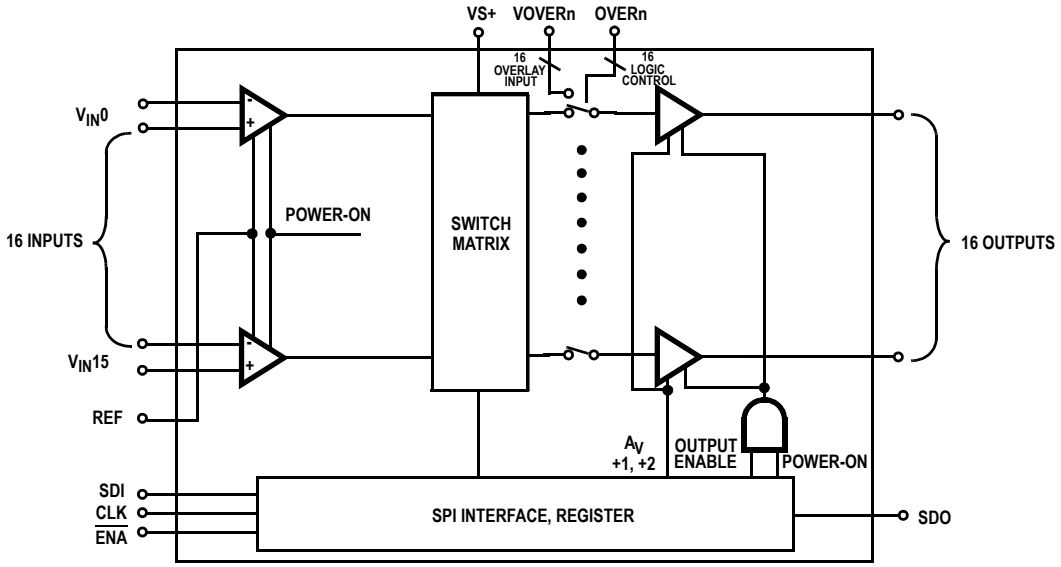
3dB Bandwidth, Broadcast Mode, A_V = 1, R_L = 100Ω [MHz]

		INPUT CHANNELS															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
OUTPUT CHANNELS	0	215	198	195	183	184	188	172	178	151	145	157	145	140	146	144	158
	1	214	195						174	152						144	158
	2	210		188					171	153					147		159
	3	212			178				171	157				143			164
	4	206				174			169	157			150				164
	5	203					177		165	159		161					164
	6	201						156	163	159	151						164
	7	204	187	182	170	170	175	160	167	167	156	168	157	151	158	154	170
	8	204	187	183	172	171	176	161	167	171	160	172	160	155	161	159	175
	9	202						157	164	170	160						174
	10	196					170		160	169		169					178
	11	194				161			157	171			160				174
	12	193			162				156	171				156			178
	13	191		170					151	174					164		178
	14	189	172						151	175						162	178
	15	187	173	167	157	155	161	149	153	178	167	179	167	160	166	164	181

3dB Bandwidth, Broadcast Mode, A_V = 2, R_L = 100Ω [MHz]

		INPUT CHANNELS															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
OUTPUT CHANNELS	0	234	216	209	199	204	205	190	196	169	160	172	162	158	163	161	178
	1	232	215						193	169						161	178
	2	228		204					189	171					164		178
	3	229			196				191	175				163			182
	4	223				193			186	177			168				183
	5	219					192		183	177		177					183
	6	217						174	181	178	167						183
	7	220	204	198	189	190	192	175	183	184	173	184	174	169	174	172	189
	8	220	205	199	190	191	193	177	184	187	178	188	178	173	178	178	193
	9	218						174	181	188	178						193
	10	220					185		176	186		187					192
	11	212				179			174	188			177				192
	12	211			179				174	192				176			195
	13	209		187					170	192					181		195
	14	208	191						167	194						181	196
	15	205	191	184	172	171	176	160	166	197	185	195	184	179	185	182	198

Block Diagram



General Description

The ISL59531 is a 16x16 integrated video crosspoint switch matrix with differential input and output buffers and On-Screen Display (OSD) insertion. This device operates from a single +5V supply. Any output can be switched to any of the 16 input video signal sources and OSD information through an internal, dedicated fast 2:1 mux located before the output buffer. Also, any one input can be broadcast to all 16 outputs.

Each output X is defined as:

Voutx = Avx*(INx-INBx+REF)

Where Avx = 1, or Avx = 2. Note that all REF's are common between channels and must be externally well buffered and/or bypassed.

The ISL59531 offers a -3dB signal bandwidth of 320MHz. The differential gain and differential phase of 0.025% and 0.05° respectively, along with 0.1dB flatness out to 50MHz. The switch matrix configuration and output buffer gain are programmed through an SPI/QSPI™-compatible, three-wire serial interface. The ISL59531 interface is set up to facilitate both fast updates and initialization. On power-up, all facilities are initialized in the disabled state to avoid output conflicts within the user system.

Digital Interface

The ISL59531 uses a simple 3-wire SPI compliant digital interface to program the outputs. The ISL59531 can support the clock rate up to 5MHz.

Serial Interface

The ISL59531 is programmed through a three-wire serial interface. The start and stop conditions are defined by the $\overline{ENA}$ signal. While the $\overline{ENA}$ is low, the data on the SDI (serial data input) pin is shifted into the 16-bit shift register on the positive edge of the SCLK (serial clock) signal. The LSB (bit 0) is loaded first and the MSB (bit 15) is loaded last (see Table 1). After the full 16-bit data has been loaded, the $\overline{ENA}$ is pulled high and the addressed output channel is updated. The SCLK is disabled internally when the $\overline{ENA}$ is high. The SCLK must be low before the $\overline{ENA}$ is pulled low.

The Serial Timing Diagram and parameters table show the timing requirements for three-wire signals.

Serial Timing Diagram

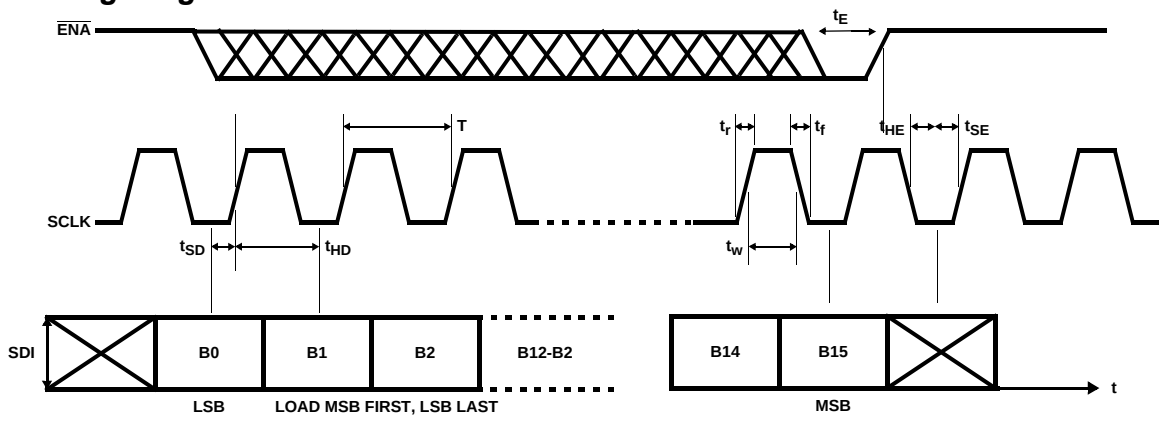


TABLE 1. SERIAL TIMING PARAMETERS

PARAMETER	RECOMMENDED OPERATING RANGE	DESCRIPTION
T	≥200ns	Clock Period
t_{HE}	≥20ns	$\overline{ENA}$ Hold Time
t_{SE}	≥20ns	$\overline{ENA}$ Setup Time
t_{HD}	≥20ns	Data Hold Time
t_{SD}	≥20ns	Data Setup Time
t_W	0.50 * T	Clock Pulse Width

Programming Model

The device has power-on reset that disables outputs, disables test mode, and turns off analog currents. To start up the device the control word is sent:

TABLE 2. CONTROL WORD FORMAT

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	-	-	-	-	0	--0	0	0	0	0	0	Power on	Common output enable

It is important to always program control bits 2-8 as zeros to avoid activating test modes designed for device manufacturing.The clamp bit activates the input clamp and bleed current sink and works only in the single-ended version.

To enable individual outputs, the output enable control word is sent. There are 16 enables to set; this is done with serial words controlling four at a time. The output enable control word format is:

TABLE 3. OUTPUT ENABLE FORMAT

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	0	1	-	-	-	N1	N0	-	O_{n+3}	-	O_{n+2}	-	O_{n+1}	-	O_n

The O_X bits represent output enables of eight individual registers. The N1 and N0 bits represent a two bit binary number which is used in setting $n = 2^{N1N0}$. For instance, to access the control bit of the 5th output enable, we send the word:

TABLE 4. OUTPUT ENABLE WORD OF 2ND GROUP OF OUTPUTS

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	0	1	-	-	-	0	1	-	O_7	-	O_6	-	1	-	O_4

Individual output enables are ended with the control register's common output enable bit and the power on bit.

Gain Setting

The gain of each output may be set to 1 or 2 using the gain set word. It is in the same format as the output enable control word:

TABLE 5. GAIN SET FORMAT

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	1	0	-	-	-	N1	N0	-	G_{n+3}	-	G_{n+2}	-	G_{n+1}	-	G_n

Input to Output Selection

Individual outputs receive their input selection choice using the input/output control word. Its format is:

TABLE 6. INPUT/OUTPUT WORD

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	I_3	I_2	I_1	I_0	0	-	-	-	O_3	O_2	O_1	O_0	0

For a given binarily selected output, as specified by the O's, an input channel is assigned by the binarily selected I's. Sixteen transmissions of the input/output control words will be required to set up all outputs. Note that B8 and B0 must be logic 0.

Broadcast Mode

The broadcast mode routs one input to all 16 outputs. It has a memory bit that remembers its state. The configuration of input/output assignments that existed before setting broadcast mode is kept in memory and when broadcast mode is disabled the previous configuration is restored. The broadcast control word format is:

TABLE 7. BROADCAST WORD

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	1	1	I_3	I_2	I_1	I_0	0	-	-	-	-	-	-	-	EB

EB sets or resets the broadcast mode memory bit. The I's binarily select the input channel to be broadcast to all outputs. Note that B8 must be logic 0.

Bandwidth Considerations

Wide frequency response (high bandwidth) in a video system means better video resolution. Four sets of frequency response curves are shown in Figure 47. Depending on the switch configurations, one can get between 250MHz to 350MHz bandwidth. A short discussion of the trade-offs follows—including matrix configuration, output buffer gain selection, channel selection, and loading.

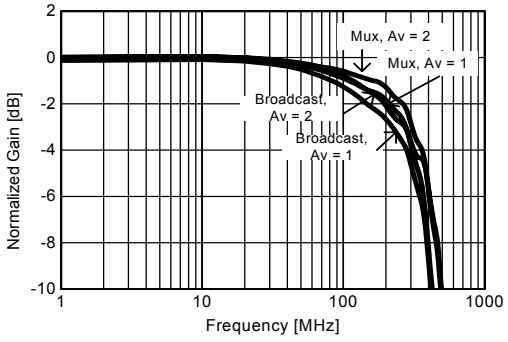


FIGURE 47. FREQUENCY RESPONSE FOR VARIOUS MODES

In multiplexer mode, the input only drives one output channel, while in broadcast mode the same input drives all 16 outputs. The parasitic capacitance of all 16 channels loads down the input and reduces bandwidth in broadcast mode. In addition, output buffer gain of +2 has higher bandwidth than gain of +1 due to internal device compensation. Therefore, the highest bandwidth set-up is multiplexer mode and output buffer gain of +2.

The relative location of the input and output channel also has significant impact on the device bandwidth. Again this is due to the layout of the device. When the input and output channels are further away, there are additional parasitics as a result of the distance and lower bandwidth results.

The bandwidth does not change significantly with resistive loading as shown in figure 3 in the typical performance curves. However, it does change greatly with capacitance loading, Figure 4 in typical performance curves. This is most significant when laying out the PCB. If the PCB trace between the output of the crosspoint switch and the back termination resistor is not minimized, additional parasitic capacitance severely distorts the frequency response.

To emphasize how critical the PCB layout is to performance, let's compare the two boards presented in figures 48 and 49. Figure 48 shows a larger engineering evaluation board where the termination resistor is far away from the device because of the use of a socket. The board in figure 48 is a demoboard without the socket. The parasitic capacitance of the demoboard is about 2.7pF less.

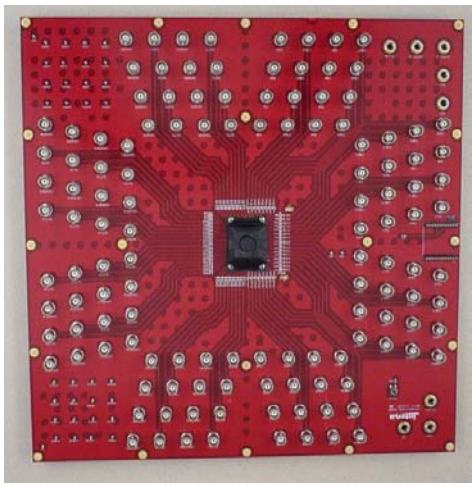


FIGURE 48. ENGINEERING EVALUATION BOARD

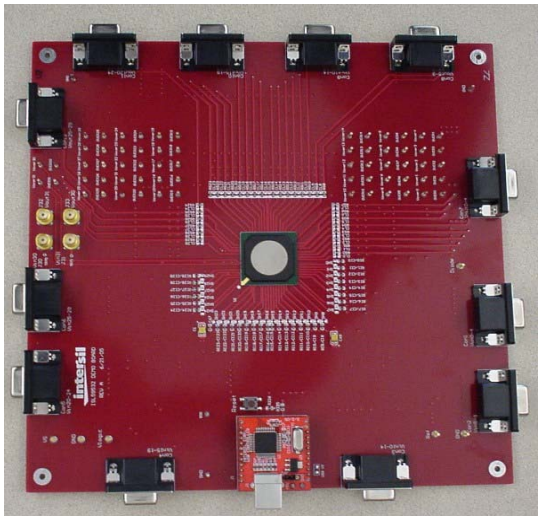


FIGURE 49. CUSTOMER DEMOBOARD

To prove that the parasitic capacitance is the largest contributor to the difference in bandwidth of the two boards, we added 2.7pF at the output of the demoboard. Figure 50 shows the similarity in frequency response of the engineering evaluation board alongside the demoboard piggybacked with 2.7pF.

Linear Operating Region

In addition to bandwidth, one must also be very careful with operating the device at its linear operating region. Figure 50 shows differential gain curve. The ISL59534 is a single supply 5V device with its linear region is between 0.1 and 2V.

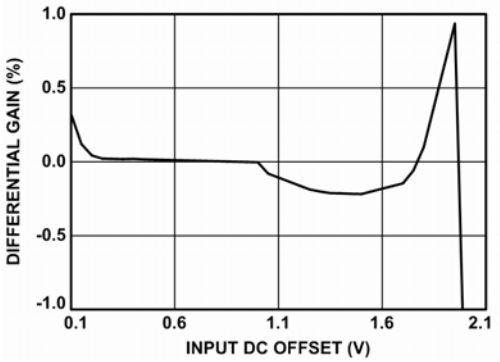


FIGURE 50. DIFFERENTIAL GAIN RESPONSE

Power Dissipation and Thermal Resistance

With a large number of switches, it is possible to exceed the 150°C absolute maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for an application to determine if load conditions or package types need to be modified to assure operation of the crosspoint switch in a safe operating area.

The maximum power dissipation allowed in a package is determined according to:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}}$$

Where:

- T_{JMAX} = Maximum junction temperature = 125°C
- T_{AMAX} = Maximum ambient temperature = 85°C
- θ_{JA} = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or:

$$PD_{MAX} = V_S \times I_{SMAX} + \sum_{i=1}^{n} (V_S - V_{OUTi}) \times \frac{V_{OUTi}}{R_{Li}}$$

Where:

- V_S = Supply voltage = 5V
- I_{SMAX} = Maximum quiescent supply current = 375mA
- V_{OUT} = Maximum output voltage of the application = 2V
- R_{LOAD} = Load resistance tied to ground = 150
- n = 1 to 15 channels

$$PD_{MAX} = V_S \times I_{SMAX} + \sum_{i=1}^{n} (V_S - V_{OUTi}) \times \frac{V_{OUTi}}{R_{Li}} = 2.52W$$

The reqired θ_{JA} to dissipate 2.52W is:

$$\Theta_{JA} = \frac{T_{JMAX} - T_{AMAX}}{PD_{MAX}} = 15.9(°C/W)$$

Table 8 shows θ_{JA} thermal resistance results for various airflows. At the thermal resistance equation shows, the required thermal resistance depends on the maximum ambient temperature.

TABLE 8. θ_{JA} THERMAL RESISTANCE [°C/W]

Airflow [LFM]	0	250	500	750
	18	14.3	13.0	12.6

356 Ld PBGA Package