HDAC52160

ULTRA-HIGH SPEED 16-BIT DAC

FEATURES

- Fast Settling Time - 150 nsec
- Excellent Linearity T. C. -1.5 ppm/°C
- On-Chip Band-Gap Voltage Reference
- On-Chip Application Resistors for Gain Selection
- TTL Compatible Inputs

APPLICATIONS

- High Speed Analog-to-Digital Converters
- Automatic Test Equipment
- Digital Attenuators
- Digital Communication Equipment
- Waveform Generators

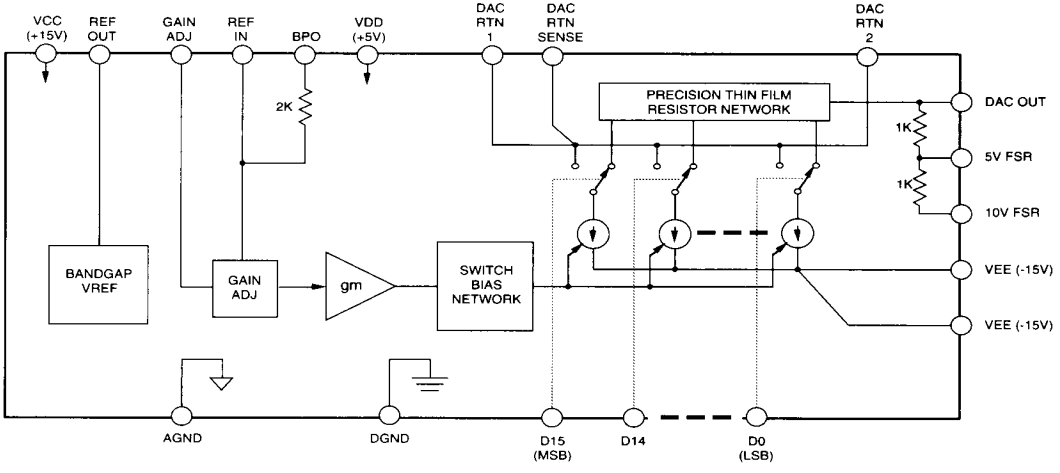
GENERAL DESCRIPTION

The HDAC52160 is a monolithic, high-performance, 16-bit digital-to-analog converter with unmatched speed and accuracy. With its 150 nanosecond settling time it is the highest speed 16-bit DAC in the industry. Unique features include the band-gap voltage reference and precision application resistors which greatly simplify device application. Unlike other high speed DACs, the HDAC52160 can be used in either a current-output or voltage-output mode.

The internal application resistors support output range selections of 0 to +10, 0 to +5, -5 to +5, and -2.5 to +2.5 volts. These internal resistors, used in conjunction with an external op amp, provide current-to-voltage conversion. Because of the high compliance voltage of the DAC output (+/- 2.5 volts), the HDAC52160 can also provide a direct voltage drive into a high impedance load without an external op amp.

The HDAC52160 operates with ±15 volt analog supplies, a separate +5 V digital supply and separate analog and digital grounds to provide maximum noise immunity. All logic input levels are TTL and 5 volt CMOS compatible. Laser-trimmed thin film technology ensures accuracy over time and environmental changes.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Beyond which damage may occur) 25 °C (1)

Supply Voltages

V_{CC} to AGND ..... +18 V
V_{EE} to AGND ..... -18 V
V_{DD} to DGND ..... +6 V
AGND to DGND Differential ..... +0.5 V

Input Voltages

All Digital Inputs to DGND ..... -0.3 V to (V_{DD} +0.3 V)
REF IN to AGND ..... 0 to +10 V

Temperature

Temperature, Ambient ..... 0 to 70 °C
case ..... -60 to +140 °C
junction ..... +150 °C
Lead Temperature (soldering 10 seconds) ..... +300 °C
Storage Temperature ..... -65 to +100 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A = 0 to +70 °C, V_{CC} = 15 V, V_{DD} = 5 V, V_{EE} = -15 V, unless otherwise specified. Minimum air flow is 50 LPM.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HDAC52160B MIN	HDAC52160B TYP	HDAC52160B MAX	HDAC52160C MIN	HDAC52160C TYP	HDAC52160C MAX	UNIT
ACCURACY SPECIFICATIONS									
Integral Linearity Error	T_A=25 °C	I		±.0015	±.003		±.0015	±.003	%FSR
Integral Linearity Error	T_A=0 to 70 °C	I		±.0045	±.006		±.006	±.012	%FSR
Integral Linearity Drift	Drift	IV		±1.5			±2.0		PPM/°C
Differential Linearity Error	T_A=25 °C	I		±.003	±.006		±.003	±.006	%FSR
Differential Linearity Error	T_A=0 to 70 °C	I		±.009	±.012		±.012	±.024	%FSR
Differential Linearity Drift	Drift	IV		±2.5			±4.0		PPM/°C
Gain Error	T_A=25°C	I		±.03	±.15		±.03	±.15	%FSR
Gain Error		I		±.08	±.25		±.08	±.25	%FSR
Gain Error Drift		IV		±20			±20		PPM/°C
Unipolar Offset Error	T_A=25°C	I		±.02	±.1		±.02	±.1	%FSR
Unipolar Offset Error		I		±.02	±.3		±.02	±.3	%FSR
Bipolar Offset Error	T_A=25°C	I		±2.5	±10		±2.5	±10	mV
Bipolar Offset Error		I		±5	±15		±5	±15	mV
DAC OUTPUT SPECIFICATIONS									
I_{OUT}		V		5			5		mA
R_{OUT}		V		1k			1k		Ω
C_{OUT}	See Fig. 1	V		12			12		pF
Output Compliance[2]		V		±2.5			±2.5		V
Output Noise	BW = 1 MHz	V		40			40		µV RMS

Note 1: Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.
Note 2: Accuracy is not guaranteed beyond this limit.

4755 Forge Road, Co. Springs, CO 80907
PH: (719) 528-2300; Fax: (719) 528-2370 SPT

ELECTRICAL SPECIFICATIONS

T_A = 0 to +70 °C, V_{CC} = 15 V, V_{DD} = 5 V, V_{EE} = -15 V, unless otherwise specified. Minimum air flow is 50 LPM.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HDAC52160B MIN	HDAC52160B TYP	HDAC52160B MAX	HDAC52160C MIN	HDAC52160C TYP	HDAC52160C MAX	UNIT
DYNAMIC SPECIFICATIONS									
Settling Time	to .0015%	V		150			150		ns
LOGIC SPECIFICATIONS									
V_{IH} 2		I	3.75			3.75			V
V_{IL} 2		I			1.5			1.5	V
I_{IH}		I		2	20		2	20	µA
I_{IL}		I		1	10		1	10	µA
REFERENCE									
Reference Output Voltage	T_A=25 °C	I	4.99	5	5.01	4.99	5	5.01	V
Reference Output Voltage		I	4.98	5	5.02	4.98	5	5.02	V
Max. Reference Output Load3	Total Current	V		8			8		mA
Output Noise4	BW = 1 MHz	V		40			40		µV RMS
POWER SUPPLIES									
V_{CC} Supply		I	14.25	15.00	15.75	14.25	15.00	15.75	V
V_{EE} Supply		I	-14.25	-15.00	-15.75	-14.25	-15.00	-15.75	V
V_{DD} Supply		I	4.75	5.00	5.25	4.75	5.00	5.25	V
V_{CC} Supply Current		I		4	6		4	6	mA
V_{EE} Supply Current		I		20	35		20	35	mA
V_{DD} Supply Current		I		6	9		6	9	mA
Power Dissipation		I		450	660		450	660	mW
PSRR, V_{CC}	+15 V±5%	V		.001			.001		%G/%PS
PSRR, V_{EE}	-15 V±5%	V		.01			.01		%G/%PS
PSRR, V_{DD}	+5 V±5%	V		.001			.001		%G/%PS

Note 3: Reference Load: REF IN = 1 mA BPO = 2.5 mA
Note 4: Reference decoupled as shown in Figure 6.

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

TERMINOLOGY

INTEGRAL LINEARITY ERROR

Integral linearity error is a measure of the maximum deviation from a straight line passing through the end points of the DAC transfer function. It is measured after adjusting for zero offset error and zero gain error.

DIFFERENTIAL LINEARITY ERROR

Differential linearity error is the difference between the measured change and the ideal 1 LSB change between two adjacent codes. A specified differential nonlinearity of <1 LSB ensures monotonicity and no missing codes.

OFFSET ERROR AND GAIN ERROR

Offset error is the absolute difference between actual and theoretical output voltage at code all 1s.

Gain error will be the difference between the measured and ideal full scale output range (after offset has been adjusted to zero) expressed as a percent of the ideal output level. The actual full scale output contains both the gain error and the offset error. Both offset and gain errors are adjustable to zero using the external trim network shown in Figures 4 and 5 respectively.

OUTPUT COMPLIANCE

Output compliance is the allowable range of voltage swing for pin DAC OUT. Other specifications, such as integral nonlinearity, are not guaranteed beyond the specified output compliance voltage.

GENERAL CIRCUIT DESCRIPTION

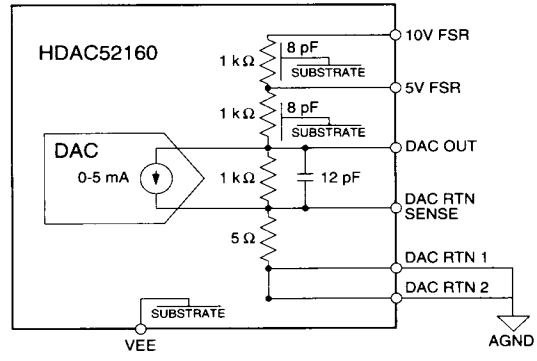
The HDAC52160 uses a unique design approach to set a new standard in monolithic DAC performance. It delivers exceptional 16-bit accuracy and stability over temperature and, at the same time, exhibits an extremely fast 150 ns settling time. On chip support functions include a stable band-gap voltage reference and application resistors for output scaling. Inclusion of these functions reduces the external analog component requirements and further increases accuracy. Digital circuitry on the chip is kept to a minimum (limited to the digital inputs), thus minimizing internal noise generation and providing interface flexibility.

DAC CIRCUITRY

The HDAC52160 uses current source segmentation for the most significant bits and an R-2R ladder for the least significant bits. The ladder, which consists of a resistor network, successively divides the (remaining) reference current to produce a binary weighted current division. In other words, in moving down the ladder, each 2R resistor leg has half the current flow of the previous leg. Each 2R resistor leg is connected to a current source that is trimmed during manufacturing to provide the 16-bit accuracy. Bipolar switches within each leg are controlled by the respective data bits (pins D0 through D15). When the controlling data bit is low, the 2R resistor leg current is steered to pin DAC OUT. When the data bit is high, the leg current is steered to the DAC RTN pins (DAC RTN 1, and DAC RTN 2), which are externally connected to analog ground.

Figure 1 illustrates the equivalent output circuit of the HDAC52160 showing on-chip application resistors and parasitic capacitances.

Figure 1 - Equivalent HDAC52160 Output Circuit



APPLICATION INFORMATION

ACTIVE CURRENT - TO - VOLTAGE CONVERSION

In many DAC applications the output current needs to be converted into a usable voltage signal. The most common current-to-voltage configuration for the HDAC52160 output is shown in Figure 2. Here, an external op amp in conjunction with the internal feedback resistor(s) is used for current-to-voltage (I-to-V) conversion. The op amp provides both a buffered Vout and maintains DAC OUT at a virtual ground. This way, Vout can provide up to a 10 volt output swing (using internal feedback resistors) and the Output Compliance specification (±2.5 volts maximum) is met.

Vout swing is determined by the feedback resistance. For a 5 volt Vout swing, the op amp's output is connected to pin 5 V FSR ("Full Scale Range") which provides an internal 1 kΩ feedback resistance. A 10 volt Vout swing is derived by connecting the op amp output to pin 10 V FSR. This feedback

4755 Forge Road, Co. Springs, CO 80907
PH: (719) 528-2300; Fax: (719) 528-2370

connection option is illustrated by the dotted line in Figure 2. Properly trimmed (as discussed later), the connections of Figure 2 as indicated, would result in the ideal output values as listed in Table I.

Figure 2 - Connection of External OP AMP for Active Current-to-Voltage Conversion

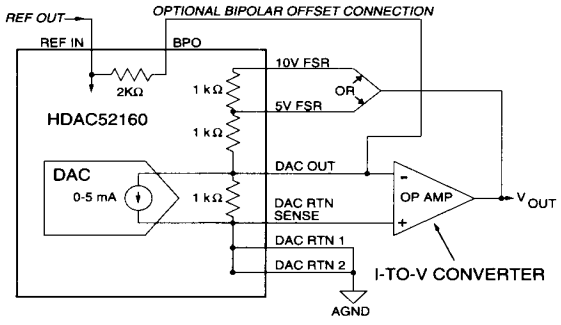


Table I - Normalized voltage values for programmable Output Ranges. (Using Figure 6)

INPUT CODE	OUTPUT VOLTAGE RANGES			
	UNIPOLAR		BIPOLAR	
	5 VOLT	10 VOLT	5 VOLT	10 VOLT
1111 1111 1111 1111	0	0	- 2.50 V	- 5.00 V
1111 1111 1111 1110	+ 76.3 μ V	+ 152.6 μ V	- 2.499924 V	- 4.999846 V
0111 1111 1111 1111	+ 2.500 V	+ 5.00 V	0.00 V	0.00 V
0000 0000 0000 0000	+4.999924 V	+ 9.999846 V	+2.499924 V	+ 4.999846 V

To configure the bipolar output range as indicated in Table I, the BPO pin is connected to DAC OUT. This connection option is illustrated in Figure 2; this offsets the output range by half of the full scale range, so that a half-scale digital input value results in a output current value of zero.

The pin connections for the active I-to-V ranges supported by the internal application resistors are summarized in Table II.

OPERATIONAL AMPLIFIER SELECTION

Selection of the external op amp involves understanding the final system performance requirements in terms of both speed and accuracy. To maintain the 16-bit accuracy provided by DAC OUT at Vout shown in Figure 2, the op amp open loop gain (Avol) must be 96 dB minimum. Any gain lower than this will contribute an error in the I-to-V conversion circuit. To maintain the 150 ns settling time capability provided by DAC OUT at Vout, the op amp must have a minimum gain bandwidth of 50 MHz and settling time of less than 100 ns to 0.0015% of full scale.

Table II - Device Pin Connection Summary for Output Range Programming. (Active I-to-V Conversion Only)

DEVICE PINS	OUTPUT VOLTAGE RANGES			
	UNIPOLAR		BIPOLAR	
	5 VOLT	10 VOLT	5 VOLT	10 VOLT
BPO	NOT CONNECTED	NOT CONNECTED	CONNECTED TO DAC OUT	CONNECTED TO DAC OUT
5V FSR	CONNECTED TO OP AMP OUTPUT	NOT CONNECTED	CONNECTED TO OP AMP OUTPUT	NOT CONNECTED
10V FSR	NOT CONNECTED	CONNECTED TO OP AMP OUTPUT	NOT CONNECTED	CONNECTED TO OP AMP OUTPUT

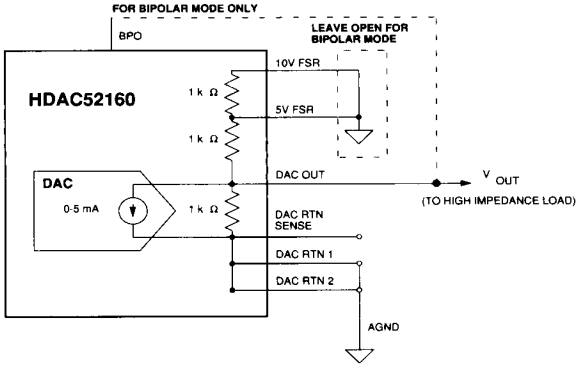
PASSIVE CURRENT-TO-VOLTAGE CONVERSION

Because of the HDAC52160's high voltage compliance, a voltage output can be derived directly at DAC OUT in a method suitable for some applications. By driving a load resistor directly with the current from DAC OUT, a voltage drop results producing Vout. An example of this implementation is shown in Figure 3, where an internal feedback resistor is used as the load 10 V FSR is grounded to optimize settling time). By utilizing all internal resistors, this circuit offers optimized stability and matching.

Output current from the DAC ranges between 0 and 5 mA, which corresponds to an input code of all 1s and all 0s, respectively. For unipolar mode, the net 500 Ω load of Figure 3 results in a -2.5 to 0 volt output range. For bipolar mode, the output voltage range is from +1.67 V to -1.67 V (typical). Both output ranges are within the specified output compliance limits. An external load resistor could also be used with this circuit, however there are difficulties with this arrangement; thermal tracking is not optimum, and the gain adjustment required to overcome the absolute internal resistance and DAC output current errors is beyond the correction range provided by the trim circuit, which is described later.

Note that the input resistance of the circuit driven by Vout will be placed in parallel with the load resistor. This hence limits the application of Figure 3 to high impedance loads. Also note that if a buffer (or other active circuit) is used at Vout in Figure 3, that circuit's CMRR must be at least 100 dB to maintain the DAC's accuracy. This is an advantage of the active current-to-voltage configuration shown in Figure 2, where the input of the op amp is always at virtual ground.

Figure 3 - Connection of Internal Load Resistors for Passive Unipolar/Bipolar Current-to-Voltage Conversion

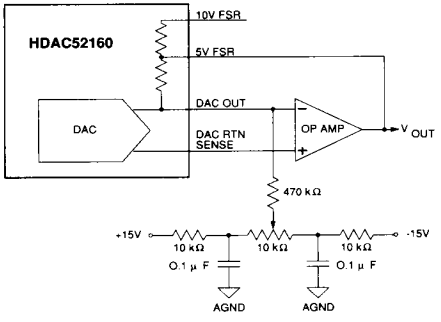


OUTPUT OFFSET COMPENSATION

Although the zero offset error of the HDAC52160 is within ±0.1% of the full scale range, some applications require better accuracy. The offset trim network of Figure 4, shown connected to DAC OUT, will allow offset adjustment in excess of ±0.2 %. This trim network can be used for the active I-to-V conversion network of Figure 2 or the passive circuit of Figure 3. When using an external op amp as in Figure 2, optimum offset stability may be achieved by using the nulling network recommended by the op amp's manufacturer.

Although accuracy of the offset network components is not important, temperature tracking of the resistor and potentiometer values will affect offset trim stability. The resistors and potentiometer should have a low temperature coefficient and the potentiometer should be a high quality, multi-turn component to ensure minute adjustability and stability over time and temperature. The 0.1 µF capacitors shown (typically ceramic) are used to decouple power supply noise from the DAC output circuit.

Figure 4 - Offset Compensation



LOGIC INTERFACE

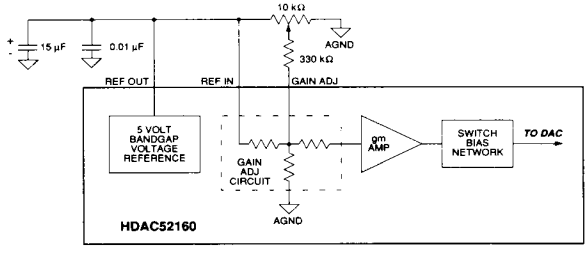
Because of the low logic input current specification, most TTL families will adequately drive the HDAC52160, even though minimum VIH is specified at 3.75 volts, a figure relatively high by TTL standards. Non-adherence to the VIH spec can result in a less than specified DAC accuracy. High-Speed CMOS logic (HC) or High-Speed CMOS logic with TTL compatible inputs (HCT) are directly compatible with the HDAC52160 logic inputs.

GAIN ADJUSTMENT

With the gain error of the HDAC52160 pre-trimmed to within ±0.15% of full scale accuracy, many applications require external gain adjustments. Configuration of the external gain adjustment network is shown is Figure 5. The adjustment potentiometer is connected between two low noise voltage sources, REF OUT and AGND, as shown. The two bypass capacitors shown further help to eliminate noise. Because of the voltage source asymmetry in relationship to the potentiometer wiper, the adjustment range is an asymmetric -0.6% to +1%. This adjustment range does sufficiently compensate for the error of the device, and the network will work for any type of output configuration. The adjustment range can be made larger and symmetrical by using a circuit similar to the offset compensation network as shown in Figure 4, but with the consequence of introducing power supply noise (and power supply variations) into the vital voltage reference circuit.

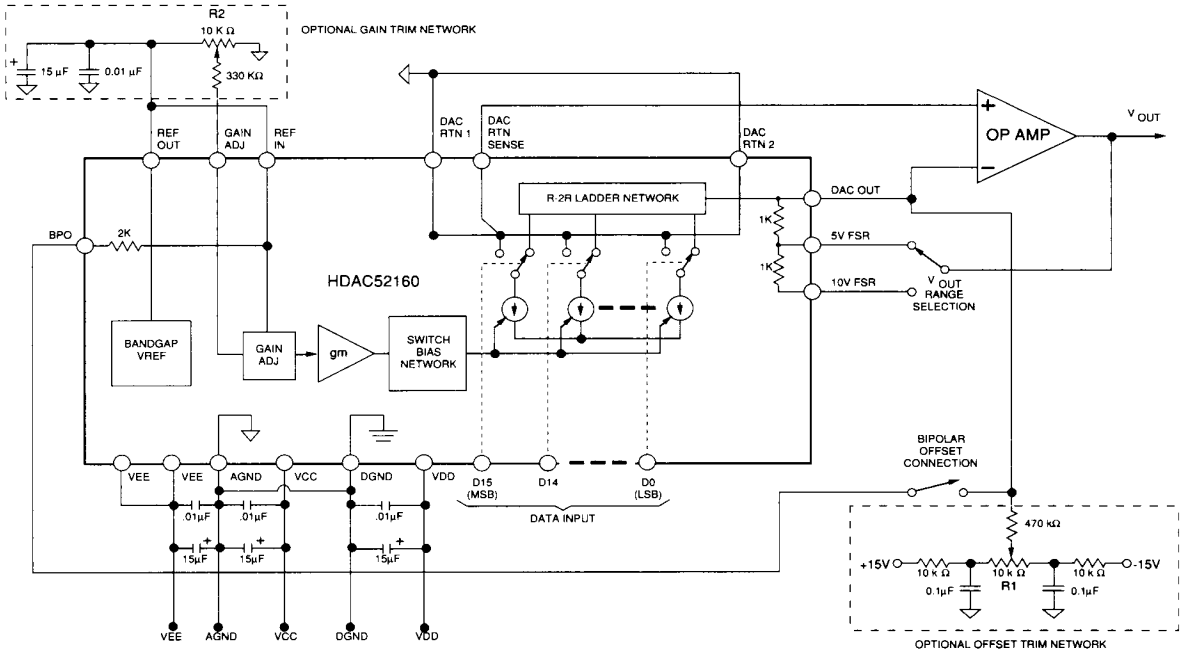
The selection criteria for the gain adjustment network components is similar to those described for the offset compensation network: accuracy is not as important as temperature stability.

Figure 5 - Gain Trim Network Suitable for All Output Configurations



4755 Forge Road, Co. Springs, CO 80907
PH: (719) 528-2300; Fax: (719) 528-2370 SPT

Figure 6 - Typical HDAC52160 Application Circuit



OFFSET AND GAIN CALIBRATION PROCEDURE

This calibration procedure is only applied to the I-to-V applications as shown in Figure 6.

The calibration consists of adjusting the "Vout" most negative voltage to its ideal value for the offset adjustment and adjusting the most positive "Vout" to its ideal value for gain adjustment. The offset and gain errors listed in the specifications for both Unipolar and Bipolar operation, may be adjusted to zero using R1 and R2 (see Figure 6) respectively. All components in the "optional offset trim network" and "optional gain trim network" shown in Figure 6 should have a low temperature coefficient. The potentiometers (R1 and R2) should be multi-turn components to insure minute adjustability.

If the adjustment is not needed, remove the "optional offset trim network" from the circuit.

Unipolar

The first step is offset adjustment. Set the input code to 1111 1111 1111 1111 and adjust R1 until Vout reads zero volts for either 5 V FSR operation or 10 V FSR operation.

Next is the gain adjustment. Set the input code to 0000 0000 0000 0000 and adjust R2 until Vout reads +4.999924 Volts for 5 V FSR operation or +9.999846 Volts for 10 V FSR operation.

Bipolar

For the Bipolar mode of operation, the calibration will start by adjusting the offset. Set the input code to 1111 1111 1111 1111 and adjust R1 until Vout reads -2.50000 Volts for 5 V FSR or -5.00000 Volts for 10 V FSR operation. The gain error calibration is done by setting the input code to 0000 0000 0000 0000 and adjusting R2 until Vout reads +2.499924 Volts for 5 V FSR operation or +4.999848 Volts for 10 V FSR operation.

CIRCUIT LAYOUT CONSIDERATIONS

In any analog system design, care must be taken in the circuit layout process. The design of a high-speed, 16-bit analog system offers an exceptional challenge. The integrity of the system's power supply and grounding is critical, and as with any precision analog component, good decoupling is needed directly at the device. Analog signal traces must be routed in a manner to minimize coupling from potential noise sources. With a 5 volt full-scale output voltage range, a mere 38 μVp-p noise level is equivalent to 1/2 LSB. Low amplitude noise such as this is virtually impossible to eliminate without totally shielding the analog circuit portion.

The power supply must be a well-regulated, noise-free analog voltage source. As with any analog device, the PSRR performance of the HDAC52160 degrades with higher frequency components. Logic noise in the supply or ground line contains high frequency components, so separate supplies and ground returns are recommended for the analog and logic portions of the system. Radiated noise from digital signal traces and power supply traces must also be avoided. Completely shield the analog circuit portion from digital circuitry and digital power supplies and ground. A separate analog ground plane near the device should be used to shield the digital data lines going into the device; this plane should have a trace that completely surrounds the digital inputs, if possible. If an analog ground plane is used with the device for shielding, keep the space between the digital ground plane and analog ground plane wide to prevent capacitive coupling. The best analog ground plane is one with the least resistance, i.e., the minimum total "squares" of surface area, regardless of size. All device grounding should be to the analog ground plane, except for the GND RTN pins which should be tied to the plane at one connection point only.

Figure 6 shows the implementation of decoupling devices (0.01 μF and 15 μF in parallel) at pin REF OUT. These devices should be connected to the analog ground and their incorporation will minimize the overall D/A conversion noise.

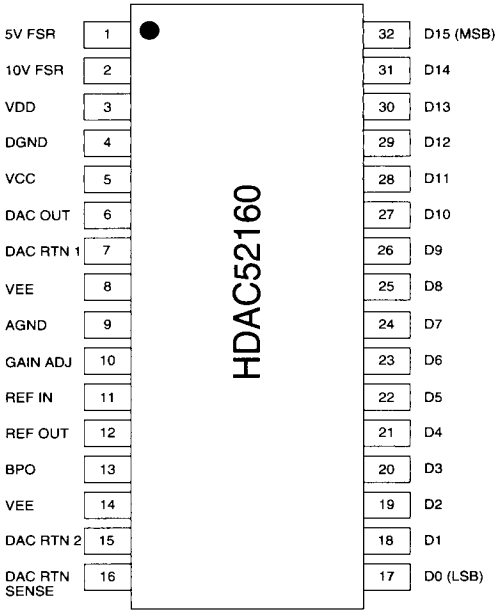
Since virtually all the interfacing to the HDAC52160 is analog in nature (the logic inputs are actually analog current switches), DGND and AGND should be tied together at the device and treated as an analog ground. This analog ground and the systems digital ground should be inter-tied only at a single point which has a low impedance path back to the system's power supplies. This will prevent modulation of the analog ground by digital power supply currents as well as digital noise injection.

The external components should be connected to the HDAC52160 with minimum length leads to help prevent noise coupling. The inputs of the external op amp are especially sensitive, so they should have short traces and be well shielded.

To the circuit driven by the HDAC52160, a voltage drop in the common analog ground will appear as a voltage offset. To avoid this, the HDAC52160 has provided a DAC SENSE pin which can be used for remote ground potential sensing.

4755 Forge Road, Co. Springs, CO 80907
PH: (719) 528-2300; Fax: (719) 528-2370 SPT

PIN ASSIGNMENT



PIN FUNCTIONS

NAME	FUNCTION
5 V FSR	Output range scaling application resistor
10 V FSR	Output range scaling application resistor
VDD	+5 volt power supply connection
DGND	Digital ground connection
VCC	+15 volt power supply connection
DAC OUT	Analog current output of DAC
DAC RTN 1	DAC ground current return path
VEE	-15 volt power supply connection
AGND	Analog ground connection
Gain ADJ	Input reference trim adjustment
REF IN	Input for internal or external reference
REF OUT	Output of internal reference
BPO	Output offsetting application resistor
VEE	-15 volt power supply connection
DAC RTN 2	DAC ground current return path
DAC RTN SENSE	DAC ground current sense connection
D0	Input data bit 0 (LSB)
D1-14	Input data bit 1-14
D15	Input data bit 15 (MSB)