CYM1841

CYPRESS SEMICONDUCTOR 256K x 32 Static RAM Module

Features

- **High-density 8-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 20 ns**
- **Low active power**
  - **5.3W (max.) at 25 ns**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of 0.58 in.**
- **JEDEC-compatible pinout**
- **Available in ZIP, SIMM, and angled SIMM footprint**
- **72-pin SIMM version compatible with 1M x 32 (CYM1851)**

Functional Description

The CYM1841 is a high-performance 8-megabit static RAM module organized as 256K words by 32 bits. This module is constructed from eight 256K x 4 SRAMs in SOJ packages mounted on an epoxy laminate board with pins. Four chip selects ($\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$, $\overline{CS}_4$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

Writing to each byte is accomplished when the appropriate chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input/output pins (I/O) is written into the memory location specified on the address pins (A_0 through A_{17}).

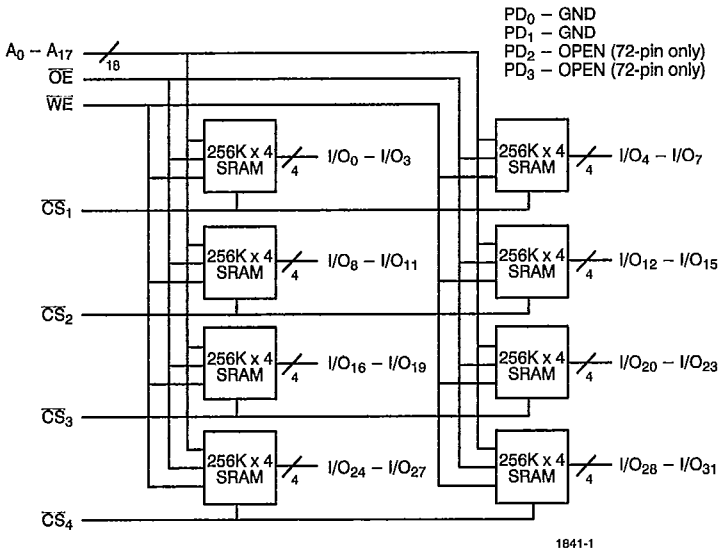
Reading the device is accomplished by taking the chip select ($\overline{CS}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the data input/output pins (I/O).

The data input/output pins stay at the high-impedance state when write enable is LOW or the appropriate chip selects are HIGH.

Two pins (PD_0 and PD_1) are used to identify module memory density in applications where alternate versions of the JEDEC-standard modules can be interchanged.

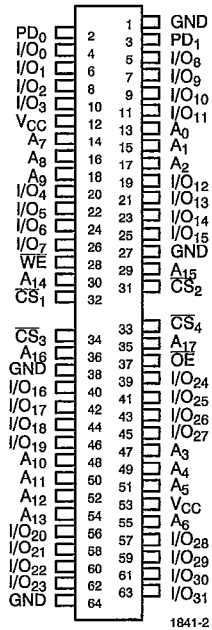
A 72-pin SIMM is offered for compatibility with future density generations. This version is socket upgradable to the CYM1851.

Logic Block Diagram



Pin Configurations

ZIP/SIMM
Top View



Selection Guide

	1841–20	1841–25	1841–30	1841–35	1841–45	1841–55
Maximum Access Time (ns)	20	25	30	35	45	55
Maximum Operating Current (mA)	1120	960	960	960	960	960
Maximum Standby Current (mA)	480	480	480	480	480	480

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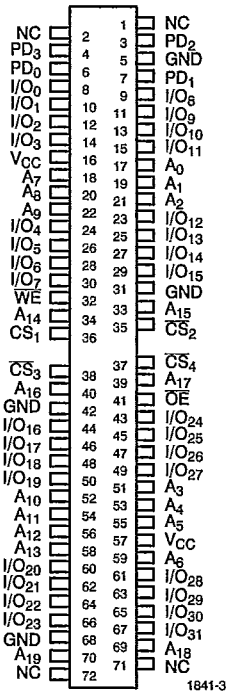
Pin Configurations (continued)

SIMM
Top View



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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 55°C to +125°C

Ambient Temperature with Power Applied ..... − 10°C to +85°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	1841−20		1841−25, 30, 35, 45, 55		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		− 0.5	0.8	− 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	− 16	+16	− 16	+16	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	− 10	+10	− 10	+10	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		1120		960	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		480		480	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V, or V_{IN} ≤ 0.2V		16		16	mA

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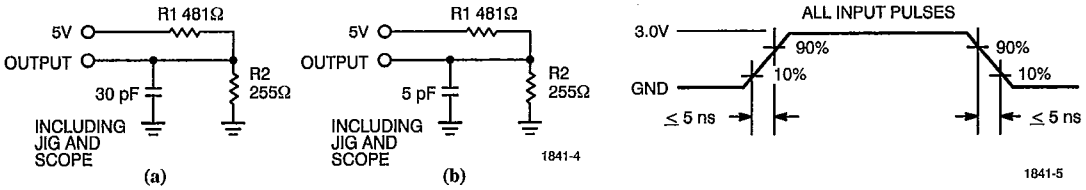
Capacitance[2]

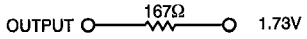
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	70	pF
C_{OUT}	Output Capacitance		20	pF

Notes:
1. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
2. Tested on a sample basis.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3]

Parameter	Description	1841–20		1841–25		1841–30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	20		25		30		ns
t_{AA}	Address to Data Valid		20		25		30	ns
t_{OHA}	Output Hold from Address Change	5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		20		25		30	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		13		15		20	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		15		15		15	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[4]	10		10		10		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4, 5]		20		20		20	ns
WRITE CYCLE[6]								
t_{WC}	Write Cycle Time	20		25		30		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	18		20		25		ns
t_{AW}	Address Set-Up to Write End	18		20		25		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	2		2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	15		20		25		ns
t_{SD}	Data Set-Up to Write End	13		15		15		ns
t_{HD}	Data Hold from Write End	2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5]	0	15	0	15	0	15	ns

Switching Characteristics Over the Operating Range (continued)[3]

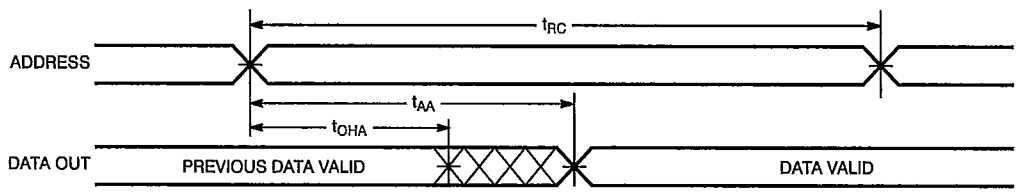
Parameter	Description	1841–35		1841–45		1841–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	35		45		55		ns
t_{AA}	Address to Data Valid		35		45		55	ns
t_{OHA}	Data Hold from Address Change	3		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		35		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		25		30		35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ LOW to High Z		15		15		15	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[4]	10		10		10		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4, 5]		20		20		20	ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		35		45		55	ns
WRITE CYCLE[6]								
t_{WC}	Write Cycle Time	35		45		55		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	30		40		50		ns
t_{AW}	Address Set-Up to Write End	30		40		50		ns
t_{HA}	Address Hold from Write End	2		2		2		ns
t_{SA}	Address Set-Up to Write Start	2		2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	30		35		45		ns
t_{SD}	Data Set-Up to Write End	20		25		35		ns
t_{HD}	Data Hold from Write End	2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5]	0	15	0	15	0	15	ns

Notes:

3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed and not 100% tested.
5. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
6. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

Read Cycle No. 1[7, 8]



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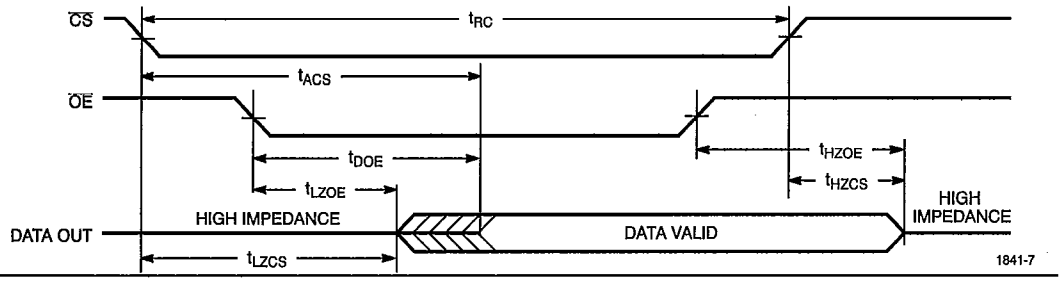
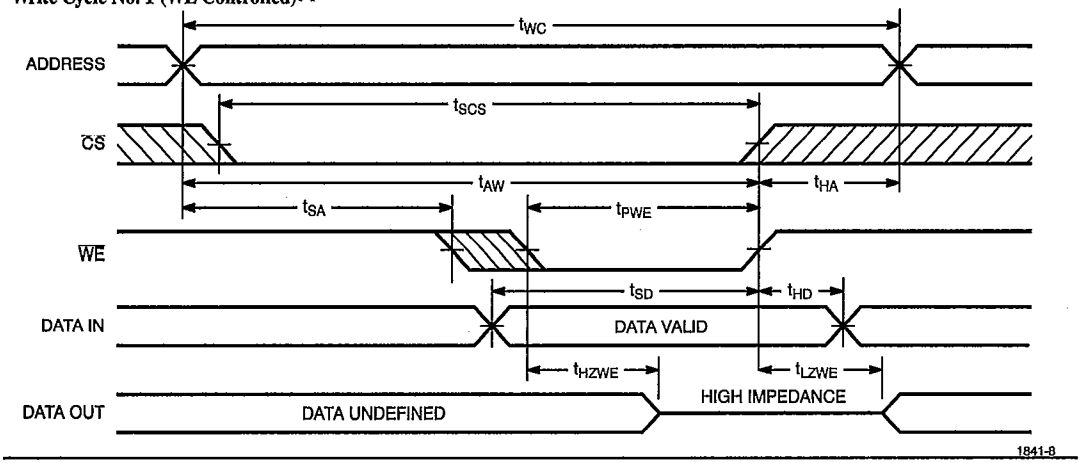
Switching Waveforms (continued)

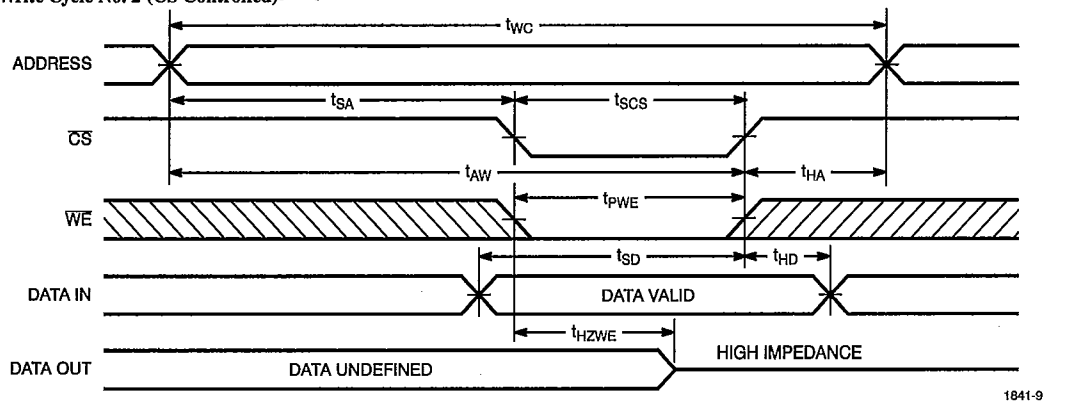
Read Cycle No. 2[7, 9]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[6]



Write Cycle No. 2 ($\overline{CS}$ Controlled)[6, 10]



Notes:

7. $\overline{WE}$ is HIGH for read cycle.
8. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{OE}$= V_{IL}.
9. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
10. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CYM1841PM–20C	PM02	64-Pin Plastic SIMM Module	Commercial
	CYM1841P7–20C	PM04	72-Pin Plastic SIMM Module	
	CYM1841PN–20C	PN02	64-Pin Plastic Angled SIMM Module	
	CYM1841PZ–20C	PZ03	64-Pin Plastic ZIP Module	
25	CYM1841PM–25C	PM02	64-Pin Plastic SIMM Module	Commercial
	CYM1841P7–25C	PM04	72-Pin Plastic SIMM Module	
	CYM1841PN–25C	PN02	64-Pin Plastic Angled SIMM Module	
	CYM1841PZ–25C	PZ03	64-Pin Plastic ZIP Module	
30	CYM1841PM–30C	PM02	64-Pin Plastic SIMM Module	Commercial
	CYM1841P7–30C	PM04	72-Pin Plastic SIMM Module	
	CYM1841PN–30C	PN02	64-Pin Plastic Angled SIMM Module	
	CYM1841PZ–30C	PZ03	64-Pin Plastic ZIP Module	
35	CYM1841PM–35C	PM02	64-Pin Plastic SIMM Module	Commercial
	CYM1841P7–35C	PM04	72-Pin Plastic SIMM Module	
	CYM1841PN–35C	PN02	64-Pin Plastic Angled SIMM Module	
	CYM1841PZ–35C	PZ03	64-Pin Plastic ZIP Module	
45	CYM1841PM–45C	PM02	64-Pin Plastic SIMM Module	Commercial
	CYM1841P7–45C	PM04	72-Pin Plastic SIMM Module	
	CYM1841PN–45C	PN02	64-Pin Plastic Angled SIMM Module	
	CYM1841PZ–45C	PZ03	64-Pin Plastic ZIP Module	
55	CYM1841PM–55C	PM02	64-Pin Plastic SIMM Module	Commercial
	CYM1841P7–55C	PM04	72-Pin Plastic SIMM Module	
	CYM1841PN–55C	PN02	64-Pin Plastic Angled SIMM Module	
	CYM1841PZ–55C	PZ03	64-Pin Plastic ZIP Module	

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