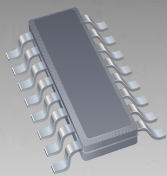


\*RoHS COMPLIANT



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## Features

- RoHS Compliant\*
- ESD protection >40k V
- Protects 2 lines
- Low capacitance - 15 pF

## Applications

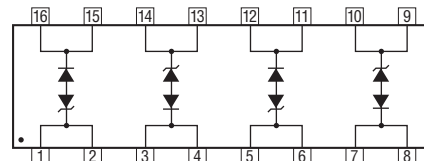
- T1/E1 Ports
- Ethernet Ports
- Wireless LANs
- xDSL Equipment

# CDNBS16-PLC05-6 – Low Capacitance TVS Diode Array

## General Information

The CDNBS16-PLC05-6 device provides ESD, EFT and Surge protection for external ports meeting IEC 61000-4-2 (ESD), IEC 61000-4-4 (EFT) and IEC 61000-4-5 (Surge) requirements.

The Transient Voltage Suppressor offers a choice of Working Peak Reverse Voltage of 5 V and Minimum Breakdown Voltage of 6 V. The device is available in a JEDEC SO-16 package and intended to be mounted directly onto an FR4 printed circuit board.



## Absolute Maximum Ratings (@ T<sub>A</sub> = 25 °C Unless Otherwise Noted)

Parameter	Symbol	Value	Unit
Peak Pulse Power (t <sub>p</sub> = 8/20 μs)	P <sub>PK</sub>	3600	W
Peak Pulse Power (t <sub>p</sub> = 10/1000 μs) <sup>NOTE 1</sup>	P <sub>PK</sub>	600	W
Storage Temperature	T <sub>STG</sub>	-55 °C to 150 °C	°C
Operating Temperature	T <sub>OPR</sub>	-55 °C to 150 °C	°C

## Electrical Characteristics (@ T<sub>A</sub> = 25 °C Unless Otherwise Noted)

Parameter	Symbol	Value	Unit
Minimum Breakdown Voltage @ 1 mA	V <sub>BR</sub>	6	V
Maximum Working Peak Voltage	V <sub>WM</sub>	5	V
Maximum Leakage Current @ V <sub>WM</sub> = 5 V	I <sub>D</sub>	300	μA
Maximum Clamping Voltage @ I <sub>P</sub> = 5 A	V <sub>C</sub>	9.6	V
Typical Junction Capacitance @ 0 V, 1 MHz	C <sub>D</sub>	15	pF
ESD Protection: Per IEC 61000-4-2 Standard			
Minimum Contact Discharge		±8	kV
Minimum Air Discharge		±15	kV
EFT Protection: Per IEC61000-4-4 Standard @ 5/50 ns		40	A
Surge Protection: Per IEC 61000-4-5 Standard @ 8/20 μs			
L3 (Line - Ground)		95	A
L4 (Line - Line)		48	A
L1 (Power)		83	A

Notes:

1. See Peak Pulse Power vs. Pulse Time.



### Asia-Pacific:

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### Europe:

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[www.bourns.com](http://www.bourns.com)

\*RoHS Directive 2002/95/EC Jan 27 2003 including Annex.

Specifications are subject to change without notice.

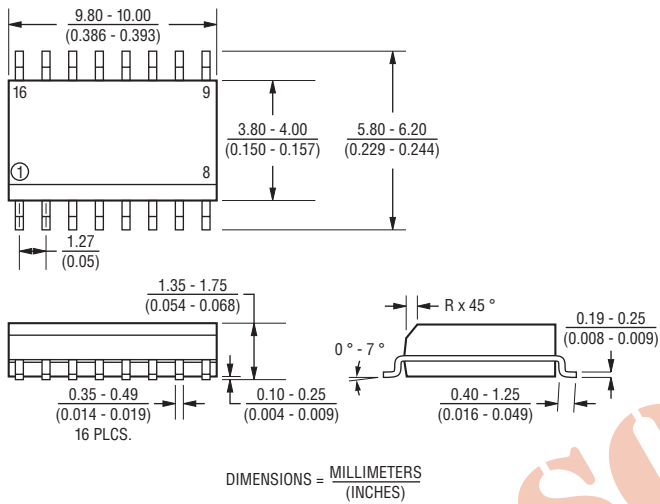
Customers should verify actual device performance in their specific applications.

# CDNBS16-PLC05-6 – Low Capacitance TVS Diode Array

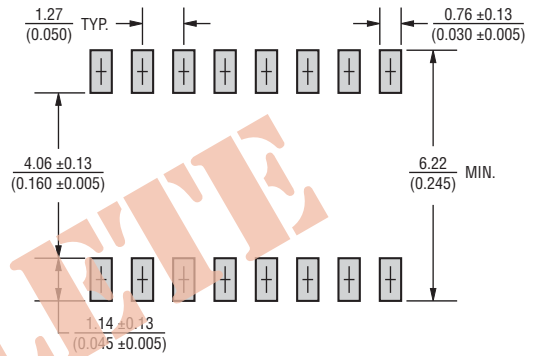


## Product Dimensions

This is a molded JEDEC SO-16 package with 100% Sn plating on the terminations. It weighs approximately 150 mg and has a flammability rating of UL 94V-0.



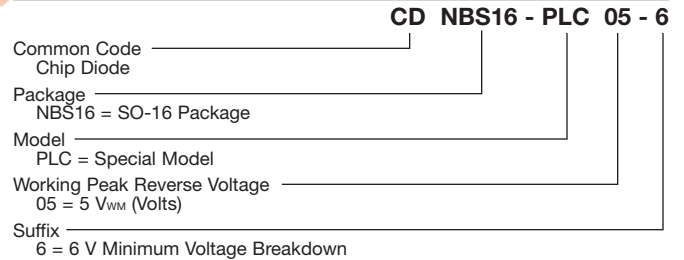
## Recommended Footprint



## Typical Part Marking

CDNBS16-PLC05-6..... **PLC05-6**

## How To Order

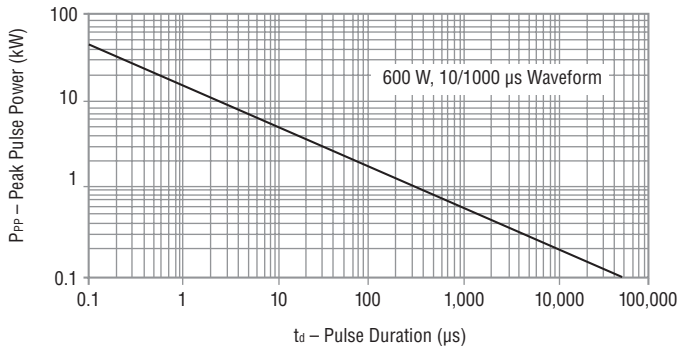


# CDNBS16-PLC05-6 – Low Capacitance TVS Diode Array

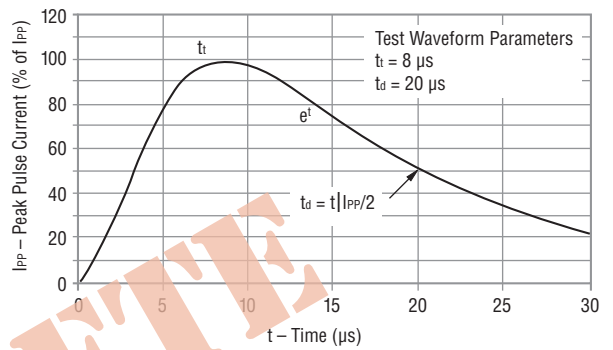


## Performance Graphs

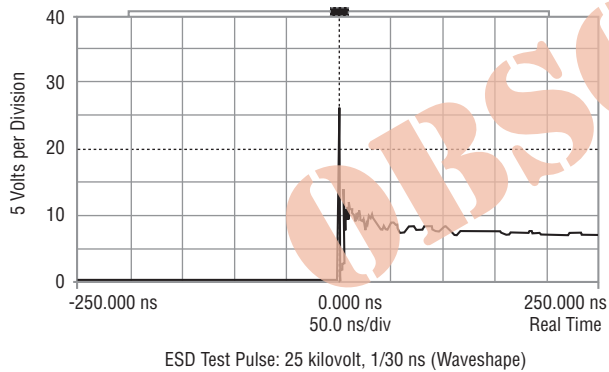
### Peak Pulse Power vs Pulse Time



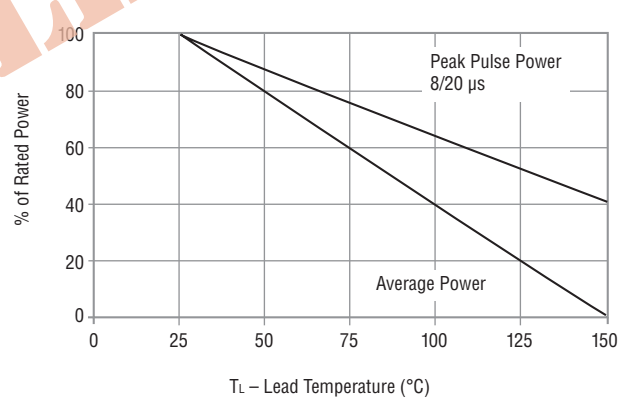
### Pulse Wave Form



### ESD Pulse Response



### Power Derating Curve

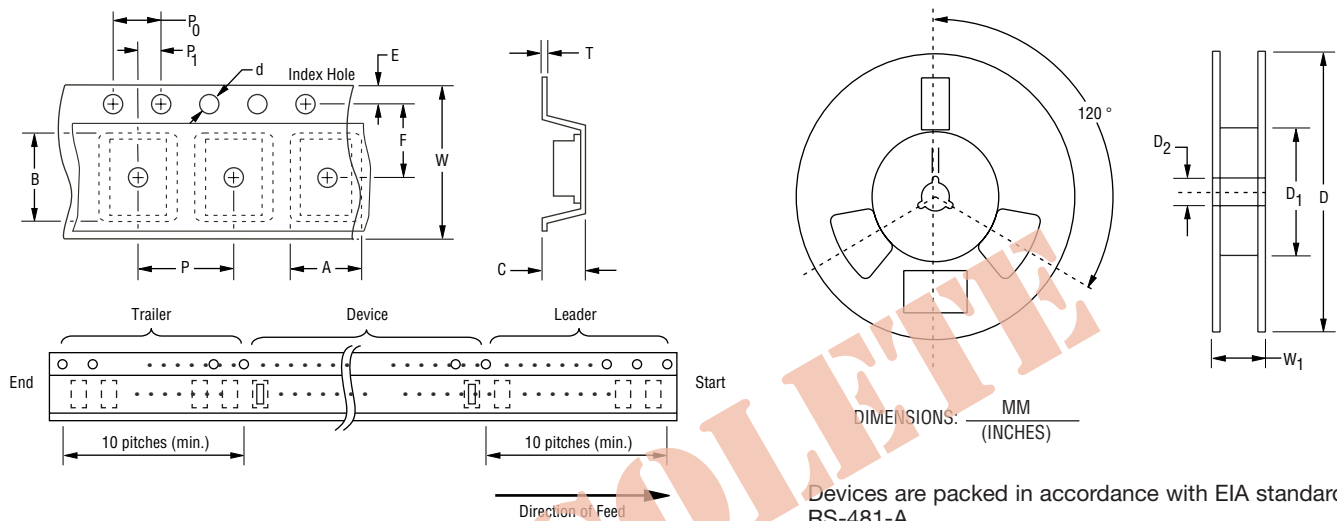


# CDNBS16-PLC05-6 – Low Capacitance TVS Diode Array

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## Packaging Specifications

The product will be dispensed in Tape and Reel format (see diagram below).



Devices are packed in accordance with EIA standard RS-481-A.

Item	Symbol	NSOIC 16L
Carrier Width	A	$\frac{6.7 \pm 0.10}{(0.264 \pm 0.004)}$
Carrier Length	B	$\frac{10.5 \pm 0.10}{0.413 \pm 0.004}$
Carrier Depth	C	$\frac{2.10 \pm 0.10}{0.083 \pm 0.004}$
Sprocket Hole	d	$\frac{1.55 \pm 0.05}{(0.061 \pm 0.002)}$
Reel Outside Diameter	D	$\frac{330}{(12.992)}$
Reel Inner Diameter	D <sub>1</sub>	$\frac{80.0}{(3.1500)}$ MIN.
Feed Hole Diameter	D <sub>2</sub>	$\frac{13.0 \pm 0.20}{(0.512 \pm 0.008)}$
Sprocket Hole Position	E	$\frac{1.75 \pm 0.10}{(0.069 \pm 0.004)}$
Punch Hole Position	F	$\frac{3.50 \pm 0.05}{(0.138 \pm 0.002)}$
Punch Hole Pitch	P	$\frac{8.00 \pm 0.10}{(0.315 \pm 0.004)}$
Sprocket Hole Pitch	P <sub>0</sub>	$\frac{4.00 \pm 0.10}{(0.157 \pm 0.004)}$
Embossment Center	P <sub>1</sub>	$\frac{2.00 \pm 0.05}{(0.079 \pm 0.002)}$
Overall Tape Thickness	T	$\frac{0.20 \pm 0.10}{(0.008 \pm 0.004)}$
Tape Width	W	$\frac{16.00 \pm 0.20}{(0.630 \pm 0.008)}$
Reel Width	W <sub>1</sub>	$\frac{18.4}{(0.724)}$ MAX.
Quantity per Reel	-	2500

REV. 09/09

Specifications are subject to change without notice.  
Customers should verify actual device performance in their specific applications.