

# Quad 2-input AND gate

# 74LVC08A

## FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- In accordance with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels

## DESCRIPTION

The 74LVC08A is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.

The 74LVC08A provides the 2-input AND function.

## QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25°C; t<sub>r</sub> = t<sub>f</sub> ≤ 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t <sub>PHL</sub> /t <sub>PLH</sub>	Propagation delay nA, nB to nY	C <sub>L</sub> = 50 pF; V <sub>CC</sub> = 3.3 V	2.6	ns
C <sub>I</sub>	Input capacitance		5.0	pF
C <sub>PD</sub>	Power dissipation capacitance per gate	Notes 1 and 2	28	pF

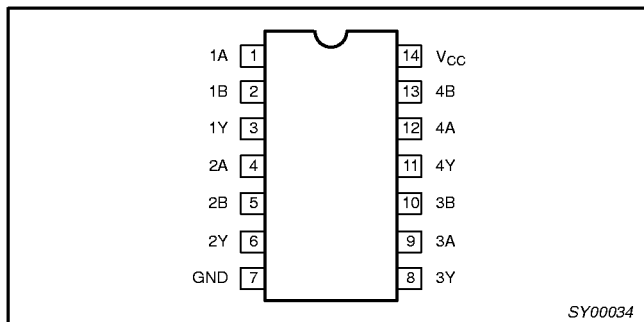
### NOTES:

- C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW)  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 f<sub>i</sub> = input frequency in MHz; C<sub>L</sub> = output load capacity in pF;  
 f<sub>o</sub> = output frequency in MHz; V<sub>CC</sub> = supply voltage in V;  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.
- The condition is V<sub>I</sub> = GND to V<sub>CC</sub>.

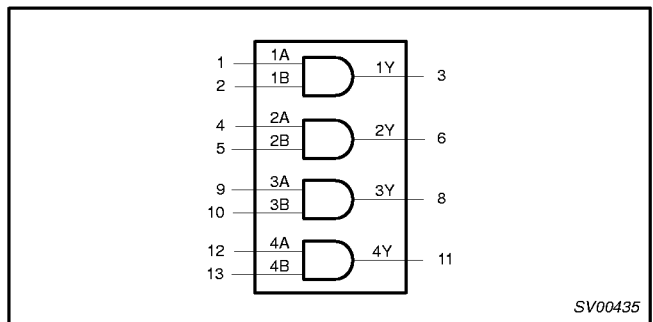
## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic SO	-40°C to +85°C	74LVC08A D	74LVC08A D	SOT108-1
14-Pin Plastic SSOP Type II	-40°C to +85°C	74LVC08A DB	74LVC08A DB	SOT337-1
14-Pin Plastic TSSOP Type I	-40°C to +85°C	74LVC08A PW	74LVC08APW DH	SOT402-1

## PIN CONFIGURATION



## LOGIC SYMBOL



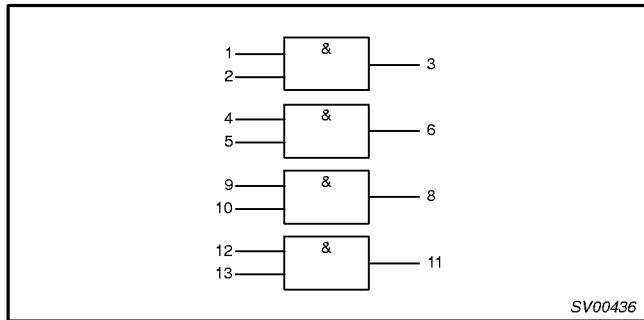
## PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A – 4A	Data inputs
2, 5, 10, 13	1B – 4B	
3, 6, 8, 11	1Y – 4Y	Data outputs
7	GND	Ground (0 V)
14	V <sub>CC</sub>	Positive supply voltage

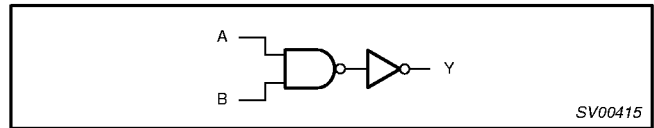
# Quad 2-input AND gate

74LVC08A

## LOGIC SYMBOL (IEEE/IEC)



## LOGIC DIAGRAM (ONE GATE)



## FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	L
L	H	L
H	L	L
H	H	H

**NOTES:**  
 H = HIGH voltage level  
 L = LOW voltage level

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
$V_{CC}$	DC supply voltage (for max. speed performance)		2.7	3.6	V
$V_{CC}$	DC supply voltage (for low-voltage applications)		1.2	3.6	V
$V_I$	DC input voltage range		0	5.5	V
$V_O$	DC output voltage range; output HIGH or LOW state		0	$V_{CC}$	V
$T_{amb}$	Operating ambient temperature range in free-air		-40	+85	°C
$t_r, t_f$	Input rise and fall times	$V_{CC} = 1.2$ to $2.7V$ $V_{CC} = 2.7$ to $3.6V$	0	20	ns/V
			0	10	

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

In accordance with the Absolute Maximum Rating System (IEC 134).  
 Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 to +6.5	V
$I_{IK}$	DC input diode current	$V_I < 0$	-50	mA
$V_I$	DC input voltage	Note 2	-0.5 to +6.5	V
$I_{OK}$	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	± 50	mA
$V_O$	DC output voltage; output HIGH or LOW state	Note 2	-0.5 to $V_{CC} + 0.5$	V
$I_O$	DC output source or sink current	$V_O = 0$ to $V_{CC}$	± 50	mA
$I_{GND}, I_{CC}$	DC $V_{CC}$ or GND current		± 100	mA
$T_{stg}$	Storage temperature range		-65 to +150	°C
$P_{TOT}$	Power dissipation per package - plastic mini-pack (SO) - plastic shrink mini-pack (SSOP and TSSOP)	above +70°C derate linearly with 8 mW/K	500	mW
		above +60°C derate linearly with 5.5 mW/K	500	

### NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

# Quad 2-input AND gate

# 74LVC08A

## DC CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP <sup>1</sup>	MAX	
V <sub>IH</sub>	HIGH level Input voltage	V <sub>CC</sub> = 1.2V	V <sub>CC</sub>			V
		V <sub>CC</sub> = 2.7 to 3.6V	2.0			
V <sub>IL</sub>	LOW level Input voltage	V <sub>CC</sub> = 1.2V			GND	V
		V <sub>CC</sub> = 2.7 to 3.6V			0.8	
V <sub>OH</sub>	HIGH level output voltage	V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -12mA	V <sub>CC</sub> - 0.5			V
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -100µA	V <sub>CC</sub> - 0.2	V <sub>CC</sub>		
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -18mA	V <sub>CC</sub> - 0.6			
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -24mA	V <sub>CC</sub> - 0.8			
V <sub>OL</sub>	LOW level output voltage	V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12mA			0.40	V
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100µA			0.20	
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 24mA			0.55	
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = 5.5V or GND		±0.1	±5	µA
I <sub>CC</sub>	Quiescent supply current	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0		0.1	20	µA
ΔI <sub>CC</sub>	Additional quiescent supply current per input pin	V <sub>CC</sub> = 2.7V to 3.6V; V <sub>I</sub> = V <sub>CC</sub> - 0.6V; I <sub>O</sub> = 0		5	500	µA

**NOTE:**

1. All typical values are at V<sub>CC</sub> = 3.3V and T<sub>amb</sub> = 25°C.

## AC CHARACTERISTICS

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> ≤ 2.5 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS							UNIT
			V <sub>CC</sub> = 3.3V ±0.3V			V <sub>CC</sub> = 2.7V			V <sub>CC</sub> = 1.2V	
			MIN	TYP <sup>1</sup>	MAX	MIN	TYP	MAX	TYP	
t <sub>PHL</sub> / t <sub>PLH</sub>	Propagation delay nA, nB to nY	1, 2	1.5	2.6	5.4	1.5	3.0	6.4	16	ns

**NOTE:**

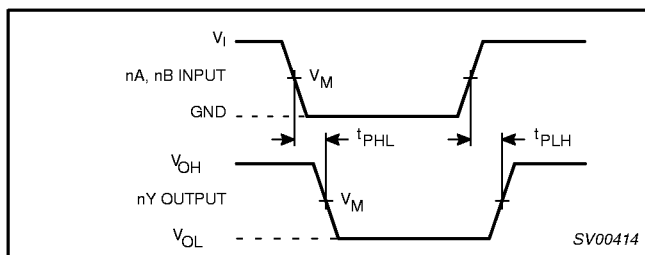
1. These typical values are at V<sub>CC</sub> = 3.3V and T<sub>amb</sub> = 25°C.

## AC WAVEFORMS

V<sub>M</sub> = 1.5 V at V<sub>CC</sub> ≥ 2.7 V

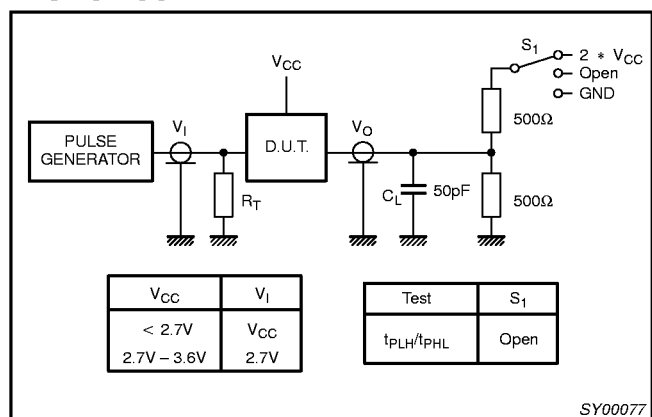
V<sub>M</sub> = 0.5 • V<sub>CC</sub> at V<sub>CC</sub> < 2.7 V

V<sub>OL</sub> and V<sub>OH</sub> are the typical output voltage drop that occur with the output load.



Waveform 1. Input (nA, nB) to output (nY) propagation delays.

## TEST CIRCUIT



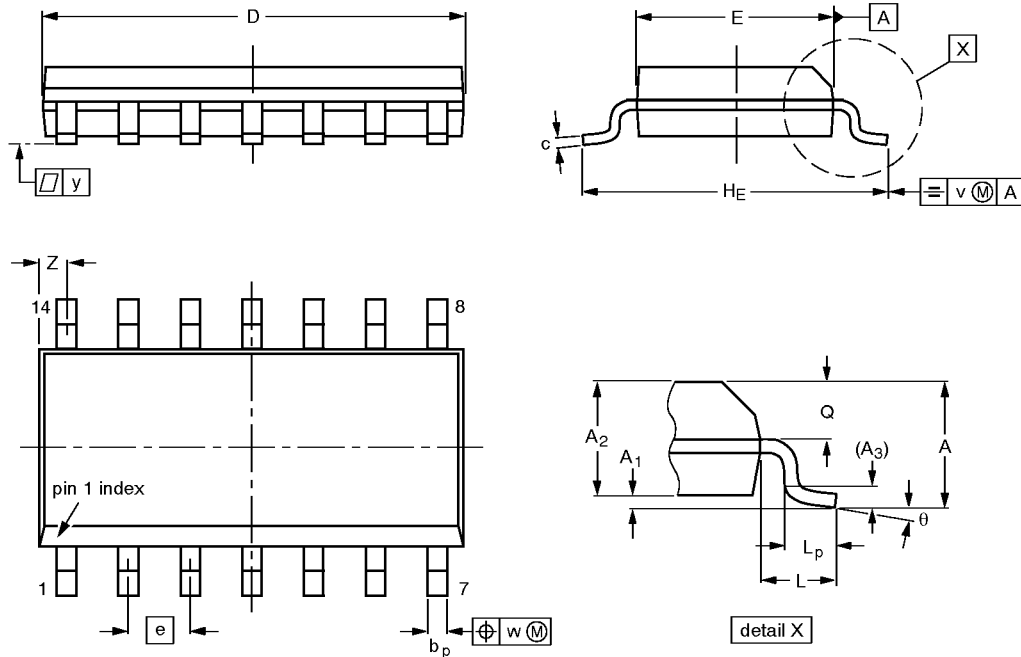
Waveform 2. Load circuitry for switching times.

# Quad 2-input AND gate

# 74LVC08A

**SO14: plastic small outline package; 14 leads; body width 3.9 mm**

**SOT108-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.35 0.34	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

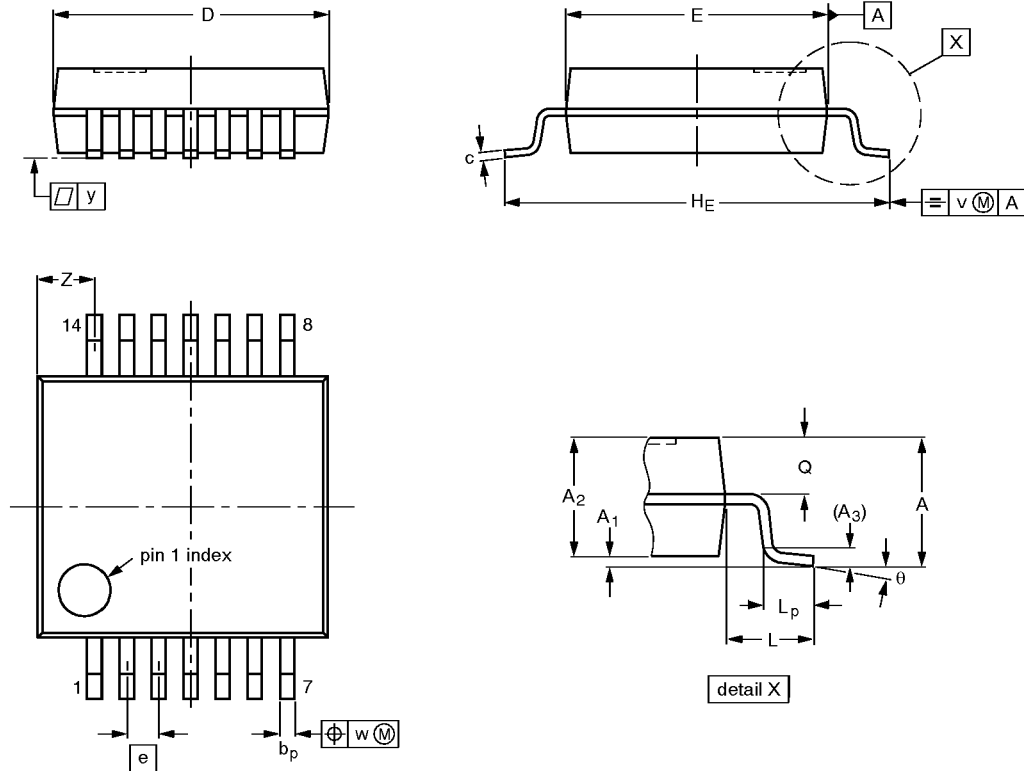
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT108-1	076E06S	MS-012AB			91-08-13 95-01-23

# Quad 2-input AND gate

## 74LVC08A

**SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm**

**SOT337-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

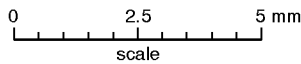
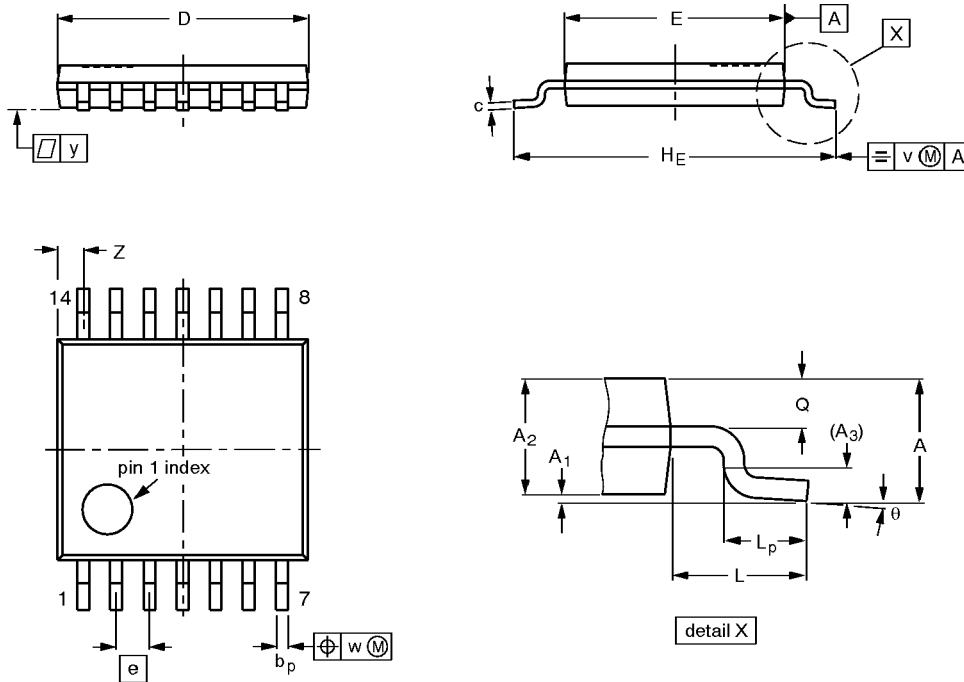
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT337-1		MO-150AB				<del>95-02-04</del> 96-01-18

# Quad 2-input AND gate

# 74LVC08A

**TSSOP14:** plastic thin shrink small outline package; 14 leads; body width 4.4 mm

**SOT402-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT402-1		MO-153				94-07-12 95-04-04