

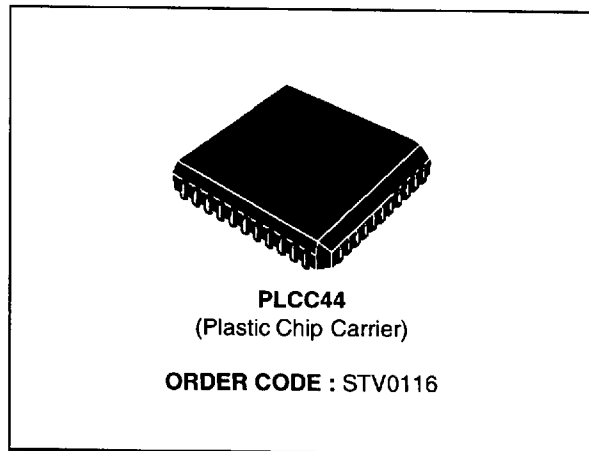
PAL/NTSC DIGITAL ENCODER

ADVANCE DATA

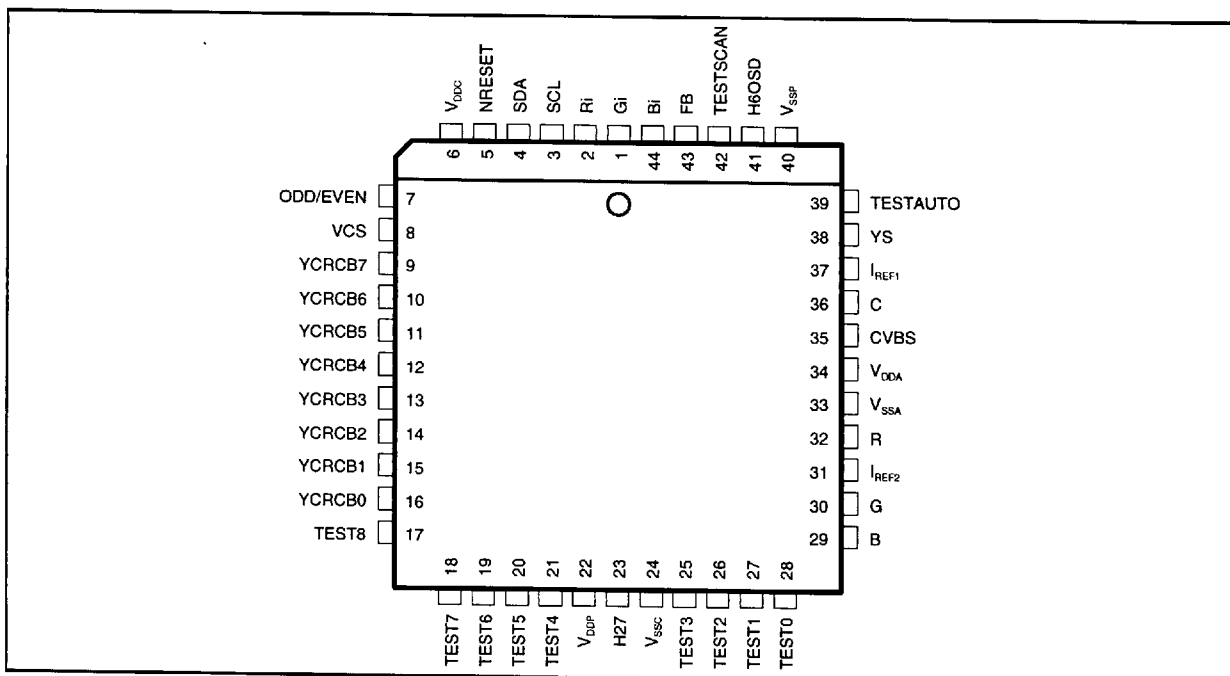
- BOTH 625 & 525 LINES MULTIPLEXED 8 BIT DIGITAL INPUT ACCORDING TO CCIR 601-2 AND REC 656
- NTSC M, PAL M, PAL B, D, G, H, I, PAL N (ARGENTINA) PROGRAMMABLE OUTPUT
- COMPOSITE OR LINE SYNCHRONISM OUTPUT
- CVBS, Y, C ANALOG OUTPUTS THROUGH 9 BIT DACs
- RGB ANALOG OUTPUTS THROUGH 8 BIT DACs
- OSD INSERTION WITH CLUT AND 6.75MHz OUTPUT CLOCK REFERENCE
- TRUE 27MHz MODULATOR
- TRUE NTSC ENCODING WITH I, Q AXIS
- OVERSAMPLING TO 27MHz FOR EASY OUTPUT FILTERING
- ODD/EVEN SYNCHRONISM INPUT/OUTPUT
- ON CHIP TEST PATTERN GENERATOR
- I²C BUS CONTROLLED
- EASY CONFIGURATION TO ANY STANDARD WITH ONE REGISTER LOADING

DESCRIPTION

The STV0116 converts the digital output of a Video MPEG decoder into a standard analog base band NTSC/PAL signal, with a modulated subcarrier. Both composite and SVHS format video signals are simultaneously delivered to 3 analog outputs. The STV0116 includes additionally three analog RGB outputs to be used for the SCART plug.



PIN CONNECTIONS



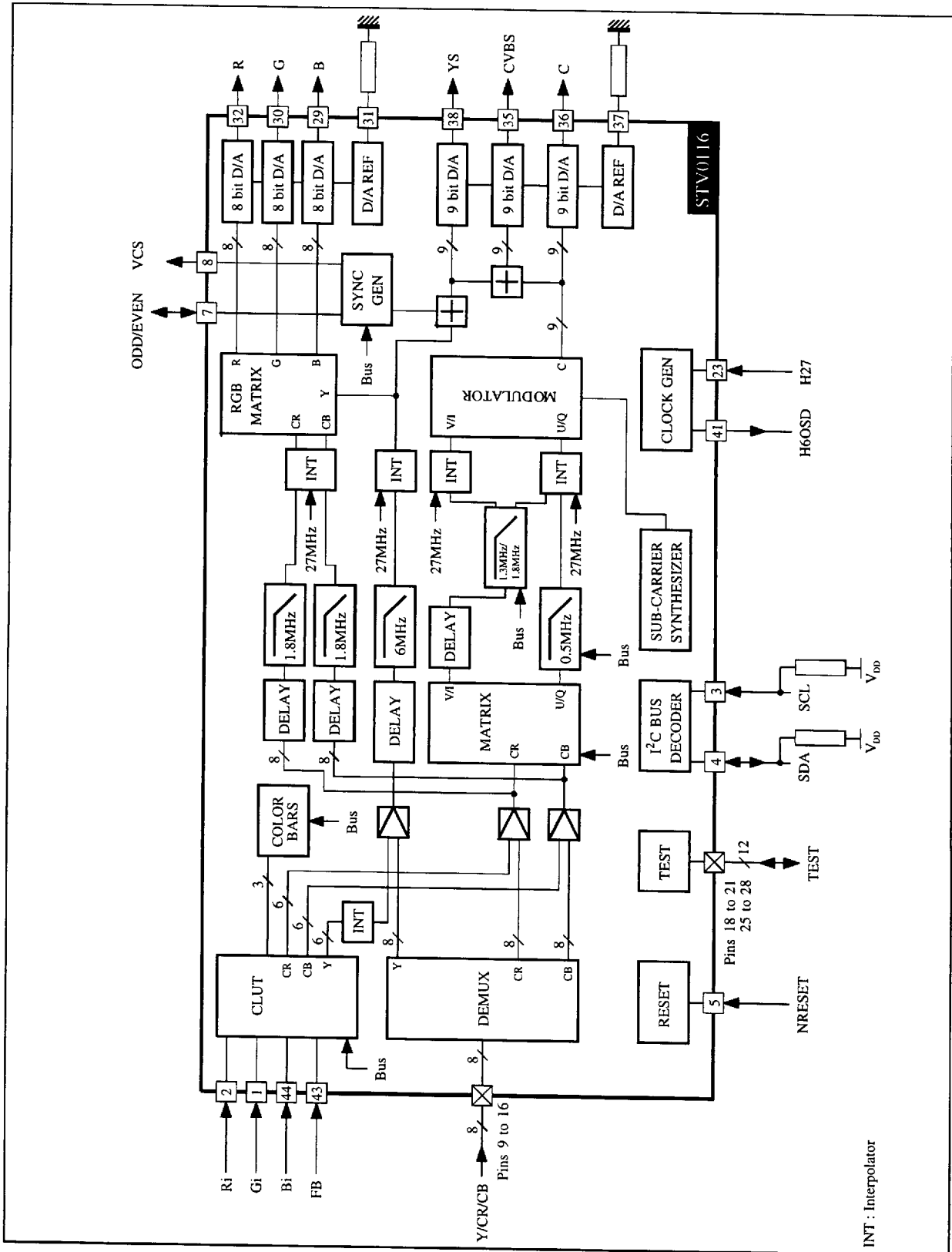
0116-01.EPS

PIN DESCRIPTION

| Pin N° | Symbol | Type | Function |
|--------------|-------------------------------------|------|---|
| 23 | H27 | I | 27MHz input clock reference. LOW/HIGH ratio : 50%. FALL and RISE time : 5ns Max. The rising edge is the reference for HOLD and SETUP time of all inputs. The duration of High/Low level is in accordance with REC656 (18.5ns \pm 3ns with less than 3ns of jitter). |
| 7 | ODD/EVEN | I/O | ODD/EVEN frame input (slave mode by ODD/EVEN), output (master mode or slave mode by EAV). The synchronism reference is the rising edge of H27. Default polarity : odd field = LOW level, even field = HIGH level. |
| 5 | NRESET | I | The hard reset is active low. It has priority on software reset. FALL and RISE time of hard NRESET < 20ns. Hold time of hard NRESET > 80ns. No synchronism of hard NRESET is necessary. NRESET Imposes default states. |
| 3 | SCL | I | Serial interface with microcontroller. Spread of frequency : 0 to 400kbit/s. Level 0 > 200ns. |
| 4 | SDA | I/O | Trigger pads to ensure a low frequency input. Maximum capacitance for each bus line (400pF). Chip address (hex) : b0 (write mode), b1 (read mode). |
| 9 to 16 | YCRCB [7:0] | I | Time multiplexed 4:2:2 luminance and color difference input as defined in CCIR Rec 601_2 and Rec 656 (TTL levels inputs). 525 lines/60Hz or 625 lines/50Hz. Timing (Rec 656 part II). A line length is 1716 or 1728 periods of 27MHz for 525 or 625 line systems respectively. |
| 2 - 1 - 44 | Ri, Gi, Bi | I | OSD serial inputs. OSD_Pixel minimum width is 148ns (i.e. 6.75MHz). Ri, Gi, Bi transcoded to Y, CR, CB according to CLUT (8 colors among 262144). CLUT tint programmable |
| 43 | FB | I | Fast blanking is minimum 1 OSD_pixel large. FB synchronous to H27. OSD active when FB is HIGH. |
| 41 | H6OSD | O | 6.75MHz clock output for the reference of an OSD input signal. |
| 8 | VCS | O | Composite synchronization or horizontal line synchronization output. Polarity (default : positive). The synchronism reference is the rising edge of H27. |
| 37 | I _{REF1} | I | Reference current source of the triple 9 bit DAC for CVBS, YS and C. For a reference load of 1.8k Ω : 1.7 < I _{REF1} (mA) < 2.1. |
| 35 | CVBS | O | Current analog video composite output. |
| 38 | YS | O | Current analog luminance output with composite synchronization, SVHS compatible. |
| 36 | C | O | Current analog chrominance output, SVHS compatible. |
| 32 - 30 - 29 | R, G, B | O | Current analog outputs synchronise with CVBS. |
| 31 | I _{REF2} | I | Reference current source of the triple 8 bit DAC for R, G, B. For a reference load of 1.8k Ω : 1.7 < I _{REF2} (mA) < 2.1. |
| 40 - 22 | V _{SSP} - V _{DDP} | | 0V-5V supply for pads. |
| 24 - 6 | V _{SSC} - V _{DDC} | | 0V-5V supply for core. |
| 33 - 34 | V _{SSA} - V _{DDA} | | 0V-5V supply for DACs. |

0116-01.TBL

BLOCK DIAGRAM



0116-02.EPS

ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|-------------------|----------------------------|-----------------------|------|
| V _{DD} | Supply Voltage | 7 | V |
| V _{IN} | Digital Inputs | V _{DD} + 0.3 | V |
| V _{OUT} | Digital and Analog Outputs | 0, V _{DD} | V |
| T _{oper} | Operating Temperature | 0, +70 | °C |
| T _{stg} | Storage Temperature | -20, +150 | °C |

0116-02.TBL

ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|--------|-----------|-----------------|------|------|------|------|
|--------|-----------|-----------------|------|------|------|------|

DC (V_{DDA} = V_{DDP} = V_{DDC} = 5V, T_{amb} = 0 to 70°C, unless otherwise specified)

| Supply | | | | | | |
|------------------|---|---|-----------------|----|-----------------------|------|
| V _{DDA} | Analog Supply Voltage | | 4.75 | 5 | 5.25 | V |
| I _{DDA} | Analog Supply Current | I _{REF1} = I _{REF2} = 3mA R _L = 400Ω | | 30 | | mA |
| V _{DDP} | Output Buffer Supply Voltage | | 4.75 | 5 | 5.25 | V |
| I _{DDP} | Output Buffer Supply Current | Autotest mode | | 30 | | mA |
| V _{DDC} | Core Supply Voltage | | 4.75 | 5 | 5.25 | V |
| I _{DDC} | Core Supply Current | Autotest mode | | 20 | | mA |
| Digital Inputs | | | | | | |
| V _L | Input Voltage LOW (SDA, SCL) | | -0.50 | | 1.50 | V |
| V _H | Input Voltage HIGH (SDA, SCL) | | 3 | | 7 | V |
| V _{IL} | Input Voltage LOW (any others are TTL compatible) | | -0.50 | | 0.80 | V |
| V _{IH} | Input Voltage HIGH (any others are TTL compatible) | | 2 | | V _{DD} + 0.5 | V |
| I _L | Input Leakage Current | V _{ILmin} or V _{IHmax} | | | 10 | μA |
| C _L | Input Capacitance (all inputs) | | | | 10 | pF |
| Digital Outputs | | | | | | |
| V _{OL} | Output Voltage LOW | I _{OL} = 1mA | V _{SS} | | 0.60 | V |
| V _{OH} | Output Voltage HIGH | I _{OH} = -1mA | 2.40 | | V _{DD} | V |
| DACs | | | | | | |
| RES1 | Resolution (YS, C, CVBS) | | 9 | | | Bits |
| RES2 | Resolution (R, G, B) | | 8 | | | Bits |
| ILE | Integral Linearity Error | I _{REF} = 3mA, V _{DDA} = 5V, R _L = 400Ω | | | ±2 | LSB |
| DLE | Differential Linearity Error | I _{REF} = 3mA, V _{DDA} = 5V, R _L = 400Ω | | | ±1 | LSB |
| I _G | Current Gain | | | 2 | | |
| G _E | Gain Error | | | 3 | | % |

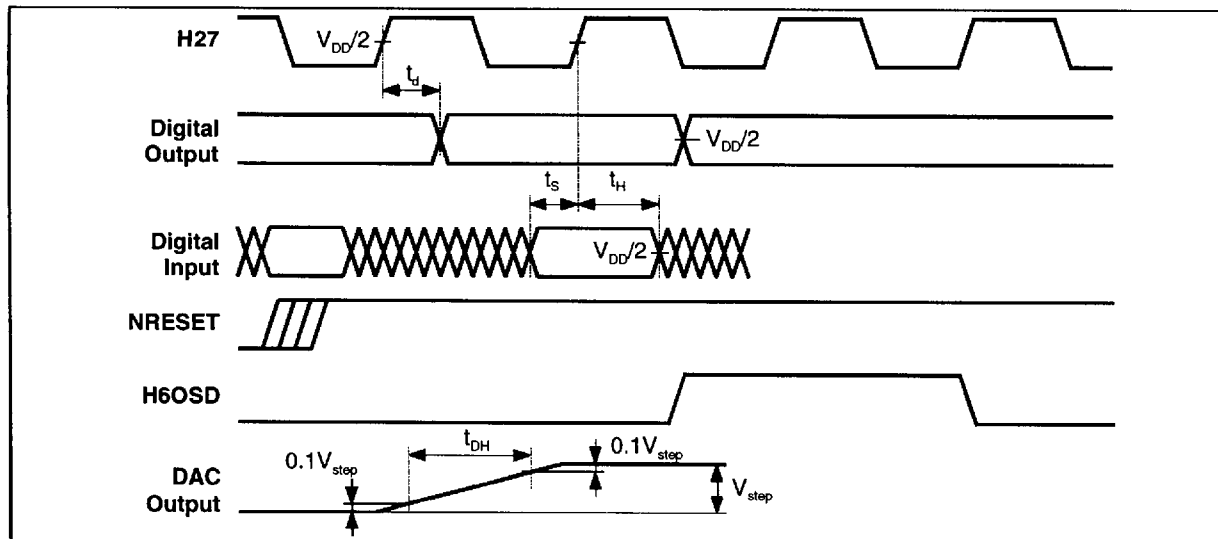
0116-04.TBL

ELECTRICAL CHARACTERISTICS (continued)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|-----------------------------------|---|------|------|------|------|
| AC ($V_{DDA} = V_{DDP} = V_{DDC} = 5V$, $T_{amb} = 0$ to $70^{\circ}C$, $C_L = 20pF$, unless otherwise specified) | | | | | | |
| Digital Inputs | | | | | | |
| t_s | Input Data Set-up Time | | 5 | | | ns |
| t_H | Input Data Hold Time | | 10 | | | ns |
| Digital Outputs | | | | | | |
| t_d | Output Delay Time | $C_L = 10pF$ | | | 29 | ns |
| ph0 | Output Phase of H6OSD After Reset | | | H27 | | |
| Fmi | Frequency of SCL | | | | 2 | MHz |
| Clock Input | | | | | | |
| t_c | Clock Cycle Time | | | 27 | | MHz |
| t_D | Clock Duty Factor | | | 50 | | % |
| t_R | Clock Rise Time | | | | 5 | ns |
| t_F | Clock Fall Time | | | | 5 | ns |
| DAC Output | | | | | | |
| t_{DH} | Output Delay Time | 32 LSB max step 9 bit dac 16 LSB max step 8 bit dac $I_{REF} = 3mA$, $R_L = 400\Omega$, $C_L = 10pF$ | | | 29 | ns |

0116-04.TBL

Figure 1



0116-21.EPS

CIRCUIT DESCRIPTION

The STV0116 can operate either in master mode or in slave mode receiving a vertical parity synchronism signal from MPEG IC.

An I²C Bus allows to control the main functions :

- Selection of the standard,
- Synchronisation mode and polarity,
- Color killing,
- Reset of the synchronism and oscillator,
- Test mode,
- By-pass of the chroma filters,
- Sub-carrier phase and frequency adjustment,
- OSD CLUT.

Pixel Input Format

The digital input is a time multiplexed YCBCR 8 bit stream.

The samples represent a succession of CB/Y/CR/Y component values and are latched on the rising edge of H27 (27MHz clock). This input is fully compatible with SGS-THOMSON MPEG decoder IC's outputs.

Video Timing

The STV0116 outputs interlaced video to conform to the NTSC or PAL timing specifications. Non standard line counts in PAL or NTSC modes are not supported.

The 8 field (for PAL) and 4 field (for NTSC) burst sequences are internally generated, using the 27MHz clock as reference.

Rise and fall times of sync, blanking interval, and the burst envelope are internally controlled according to the composite video specification (see Figures 6 and 7).

Only lines 1 to 9, 264 to 272 for 525 and 624 to 5, 311 to 318 for 625 lines system respectively are blanked. The others can be used for data encoding.

Master Mode

After a software reset, the sync generator starts counting 27MHz clock pulses and provides a complete composite sync pulse sequence of 4 fields to the NTSC encoder.

For PAL, the combination with the ODD/EVEN line sequence gives the 8 field sequence for the color burst insertion. At the end of a sequence the counter is automatically reset and a new sequence can start. In the same time an ODD/EVEN frame pulse is output to control the MPEG decoder.

Slave Mode

After a software reset, the sync counter waits for the falling edge of the ODD/EVEN pulse sent to the

ODD/EVEN Pin selected as an input. Then a sequence identical to the one in master mode can start and is reset by the next falling edge of the field pulse (see Figure 2).

If no ODD/EVEN pulse is present after a full 3 frames sequence, the IC can either regenerate itself the next sequences in "free running" using the 27MHz clock, or switch on the internal test bar pattern, or blank the outputs, after reading status register.

Alternatively the STV0116 can be set to extract the synchronization directly from the Y/CR/CB input data sequence (see Figure 3).

These different modes are selectable by the I²C Bus.

Chrominance Encoding

The demultiplexed CR, CB samples feed a chroma I/Q matrix for NTSC and a U/V matrix for PAL. The U/V or I/Q chroma signals are then band limited according to the CCIR 624 recommendations and interpolated at a 27MHz pixel rate. This process makes easier the filtering for the D/A conversion and allows a more accurate encoding.

A Discrete Time Oscillator, using a 22 bit phase accumulator, generates the color sub-carrier. This signal feeds a quadrature modulator which modulates the baseband chroma signals.

The phase and the frequency of the sub-carrier can be adjusted if needed or reset by software.

Luminance Processing

The demuxed Y samples are band limited and interpolated at 27MHz samples rate.

Then a gain and offset compensation is applied to the luma signal before inserting the synchronism pulses.

The interpolation filter compensates for the sinX/X attenuation provided by the D/A conversion, and greatly simplifies the output filtering.

A delay is inserted in the luma path to transmit correctly picture transition.

CVBS and SVHS Outputs

Each digital signal drives a 9 bit D/A converter operating at 27MHz.

The outputs are current sources and are proportional to the current reference value. For 3mA reference current and 400Ω load, the levels are such that a PNP emitter follower is enough to drive the SCART plug (1V from sync tip to white level). The integrated over sampling filters make the external antialiasing low pass filter simpler.

CIRCUIT DESCRIPTION (continued)

Reset Procedure

A hard reset is performed by grounding the reset pin. This will set the IC in PAL BDGHI and slave mode.

The "software reset" configure the IC according to the configuration fixed by register 0 (that isn't reseted itself). The sync generator is then ready for a new sequence. This will be initialized either by the next clock pulse in master mode, or by the next field pulse in slave mode.

R, G, B Outputs

After demux, CR/CB data feed a 4 times interpolation filter at 27MHz sample rate. Then the chroma base-band signal is band limited at 1.8MHz and matrixed with Y. Three 8 bit D/A converters generate R, G, B outputs at 27MHz.

H6OSD Output

This 6.75Mhz clock signal is intended to trig the OSD input data. It is synchronous with the H27 clock reference.

Master/Slave Functionality

T = 1 period of H27. Duration of active line is 1440T.

R, G, B, FB OSD Inputs

These are logic inputs for OSD insertion. FB (fast blanking) is used to switch from the main video input to the RGB inputs. FB and RGB inputs must be locked to the H27 clock. They are latched on the rising edge of 6.75MHz clock signal.

The RGB inputs allow 8 color combinations. The internal CLUT (color look up table) affects for each of these 8 values a color chosen among 643 preset for Y, CR, CB components. As CLUT performs the matrixing into Y, CR and CB, the resulting signals take benefit of the oversampling filters in the main path. Additionally the Y signal is interpolated. Inserted OSD rate is 6.75Mbit/s.

Signal Quality Detector

It is active if the timing reference synchronization data of the input data stream is present.

By use of Hamming decoding in video Y/CR/CB (EAV, SAV), the IC generates a bit (HOK). This bit indicates multiple errors of the hamming decoding. It can be read by the microcontroller.

Figure 2 : Slave 1 (Slave by ODD/EVEN)

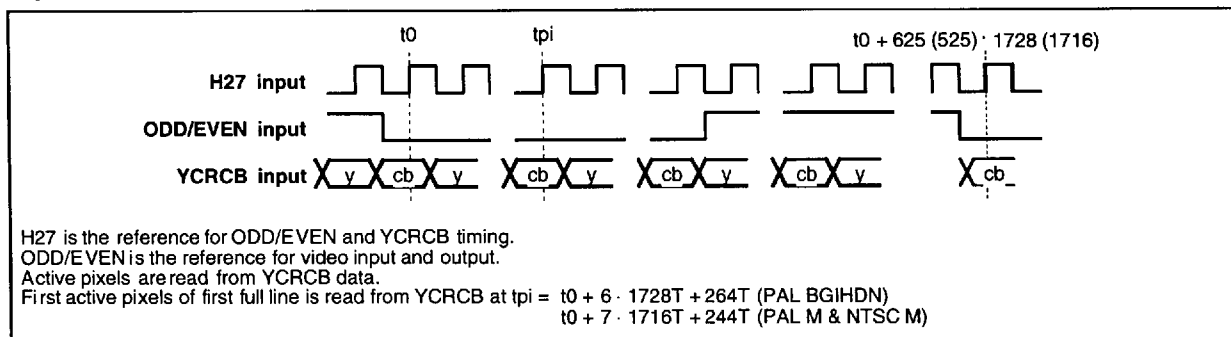


Figure 3 : Slave 2 (Slave by EAV, End of Active Video, taken on YCRCB)

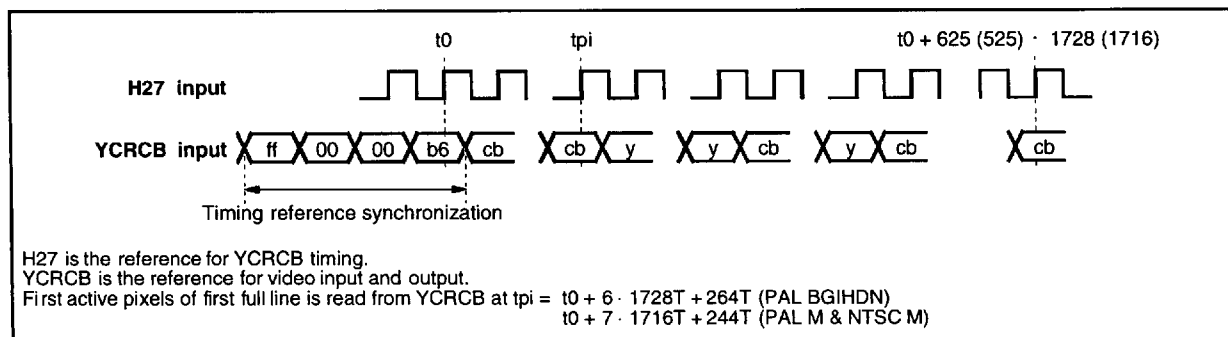
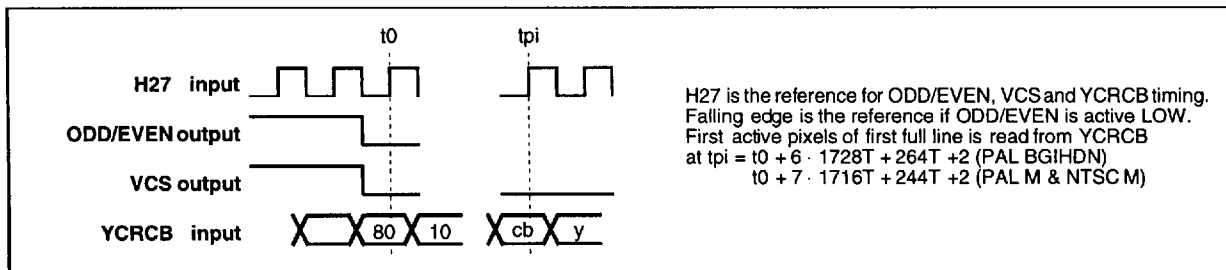


Figure 4 : Master Mode



0116-06.EPS

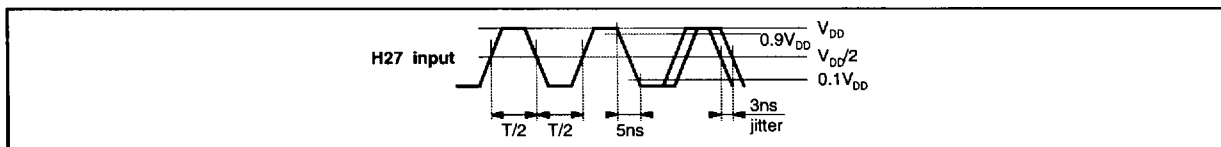
Freerun and SLAVE Mode

If freerun is allowed and the vertical synchronism is lost, all the video signals are generated with the picture sampled on YCRCB. VCS is still available. If freerun is not allowed VCS is stopped and YS, C, CVBS, R, G, B are at BLACK level.

Synchronization Signals

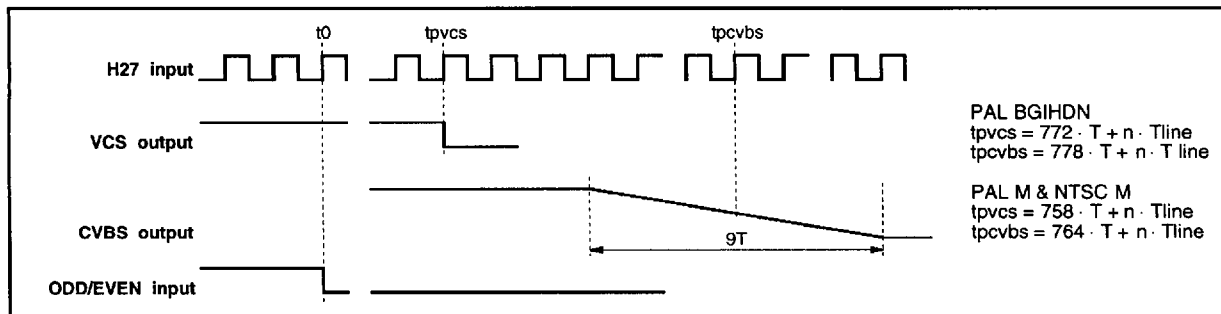
$T = 37.037ns = 1$ period of H27 (27MHz).

Figure 5 : H27 Input Maximum Acceptance



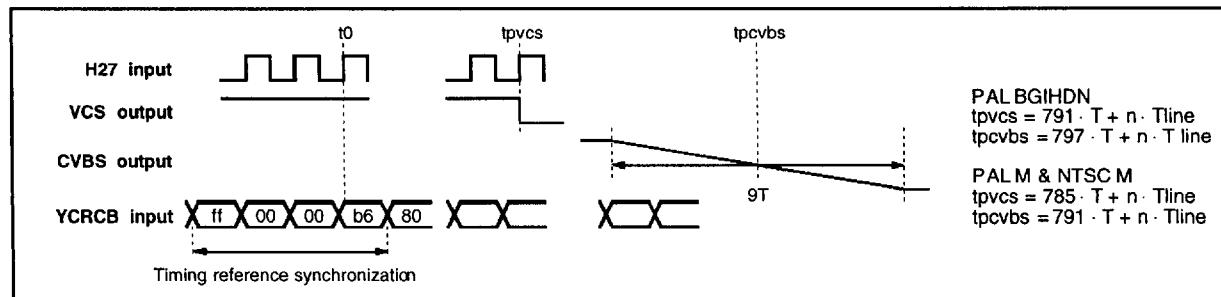
0116-07.EPS

Figure 6 : Logic and Analog Synchronisms



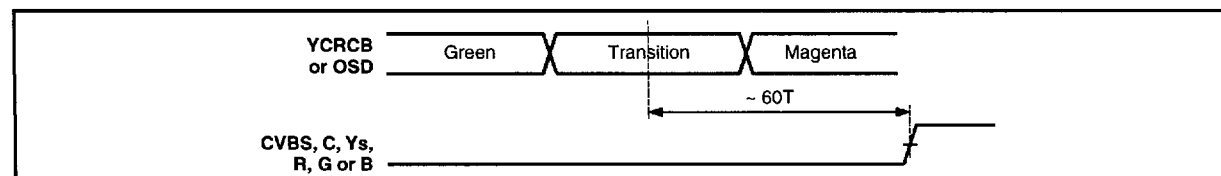
0116-08.EPS

Figure 7 : Logic and Analog Synchronisms (Slave by EAV synchro only)



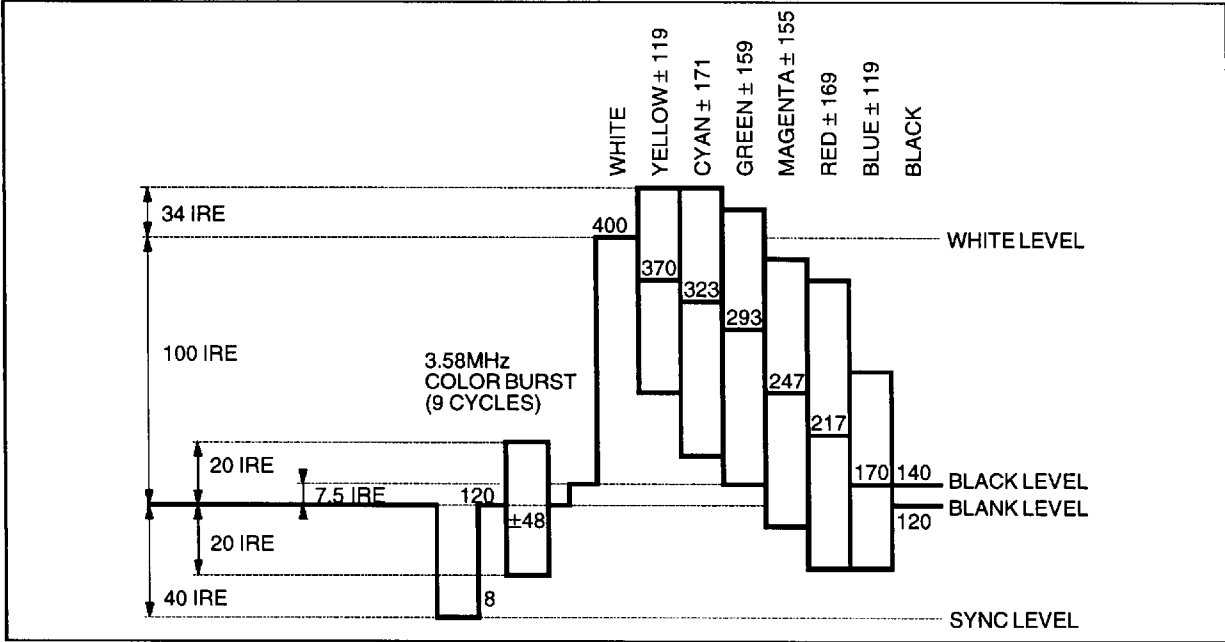
0116-09.EPS

Figure 8 : YCRCB and OSD Delay to Analog Output



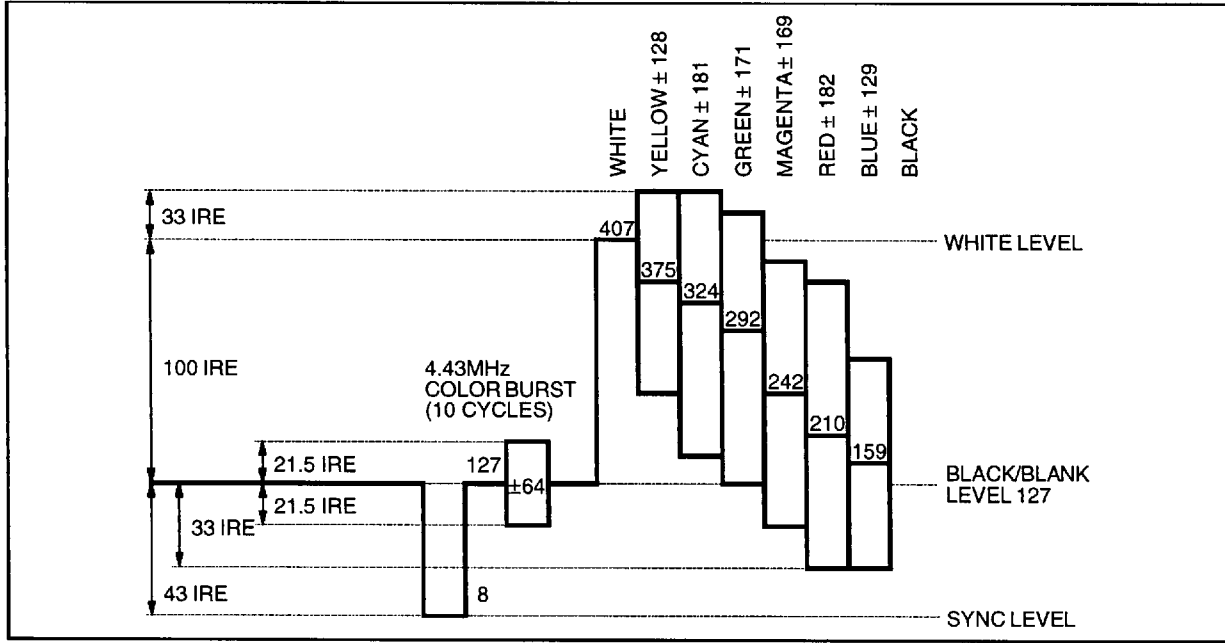
0116-22.EPS

Figure 9 : M Composite NTSC Output (100% Saturation, 100% Amplitude Colour Bars)



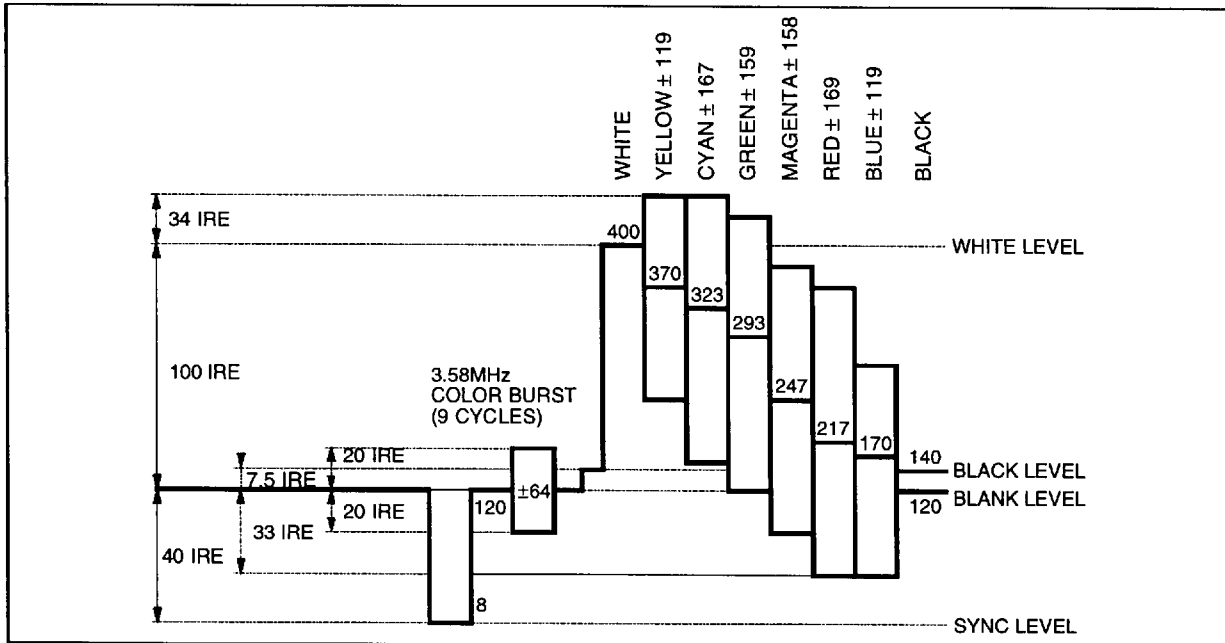
0116-10.EPS

Figure 10 : Composite PAL BGDHIN Output (100% Saturation, 100% Amplitude Bars)



0116-11.EPS

Figure 11 : Composite PAL M Output (100% Saturation, 100% Amplitude Bars)



0116-12.EPS

Figure 12 : Luma Filter

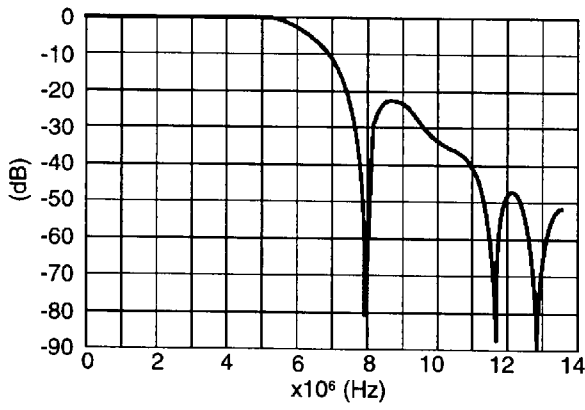


Figure 12a : Luma Filter

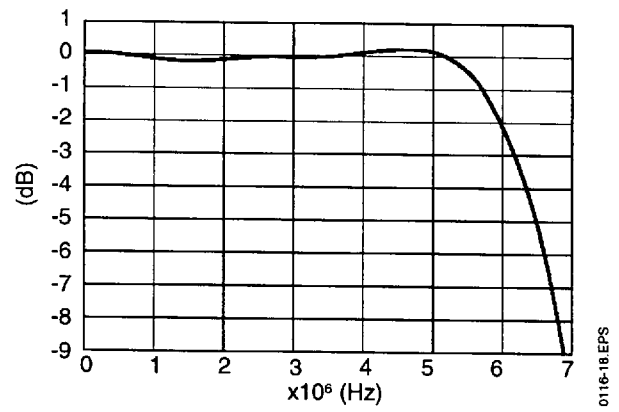


Figure 13 : Chroma Q Filter

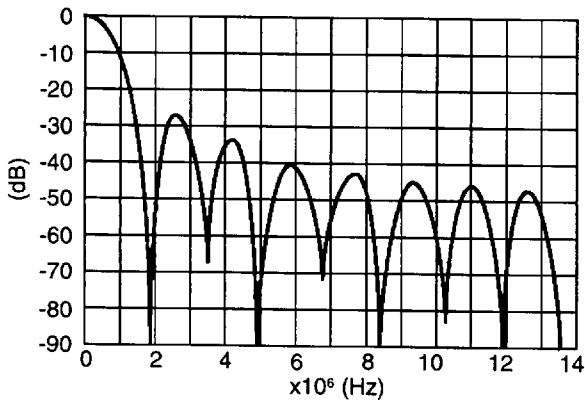


Figure 13a : Chroma Q Filter

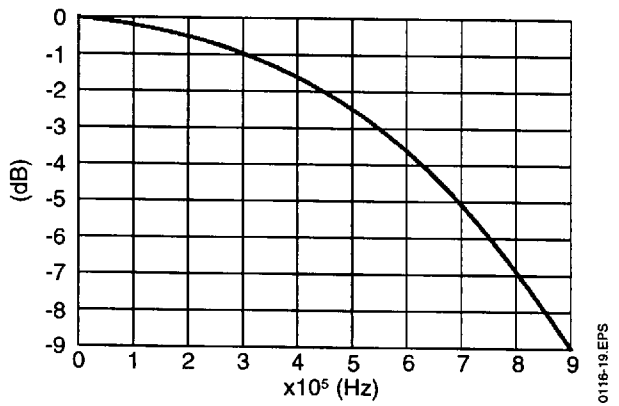


Figure 14 : Chroma Filters

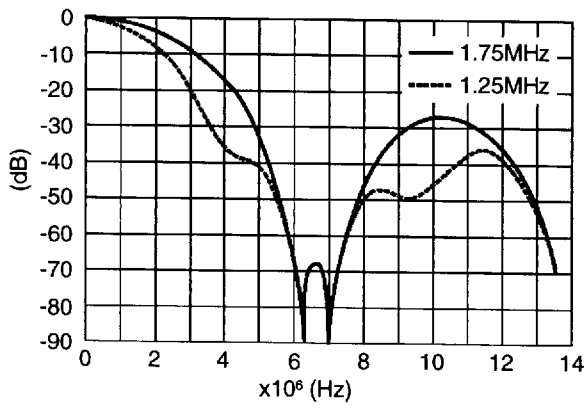
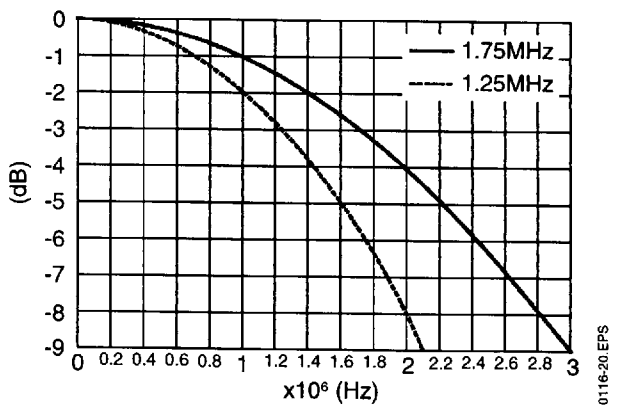


Figure 14a : Chroma Filters



Note : Those filter curves include the sinc/x attenuation of DACs.

I²C REGISTERS DESCRIPTION

The IC is controlled by an I²C Bus and internal registers can be read or written by an external microcontroller.

Encoder addresses are :

- Write 10110000 (b0 hex).
- Read 10110001 (b1 hex).

Registers are organized as follows :

- Reg 0 : Sync mode selection, standard selection, sync polarity selection
- Reg 1 : Color killer, chroma filter selection, sync output selection
- Reg 2, 3 : Sync delay
- Reg 4 to 9 : Sub-carrier frequencies
- Reg 10 to 17 : Y clut for RiGiBi input encoding
- Reg 18 to 25 : CR clut for RiGiBi input encoding
- Reg 26 to 33 : CB clut for RiGiBi input encoding
- Reg 34 : Test (not to be used)
- Reg 35 : Status
- Reg 36 to 38 : Line forcing

I²C FORMAT

Write Mode (all registers except STATUS)

| | | | | | | | | | | | |
|---|---------------|---|---|-------------|---|--------|---|-----|--------|---|---|
| S | Slave address | W | A | Sub-address | A | Data 0 | A | ... | Data N | A | P |
|---|---------------|---|---|-------------|---|--------|---|-----|--------|---|---|

- S Start condition
- Slave address 1011000
- W = '0' Write flag
- A Acknowledge, generated by slave (STV0116) when OK A = '0' else '1'
- Sub-address Sub-address register (content is made of one byte)
- Data 0 First data byte
- Data N Continued data bytes (address is automatically incremented) and A's
- P Stop condition

Read Mode (all registers)

| | | | | | | |
|---|---------------|---|----|---------------|----|---|
| S | Slave address | W | AC | Sub-address N | AC | P |
|---|---------------|---|----|---------------|----|---|

Then :

| | | | | | | | | |
|---|---------------|---|----|--------|----|----------|----|---|
| S | Slave address | R | AC | Data N | AM | Data N+1 | AM | P |
|---|---------------|---|----|--------|----|----------|----|---|

- S Start condition
- Slave address 7 bit address for STV0116: 1011000
- W = '0' Write flag
- AC Acknowledge, generated by slave (STV0116) when OK, AC = '0' else '1'
- R = '1' Read flag
- Sub-address 8 bit sub-address register
- Data N Data byte of register N, sent by STV0116
- Data N+1 Data byte of register N+1 (address automatically incremented)
- AM Acknowledge, generated by the microcontroller AM = '0' when acknowledge is OK else '1'
- P Stop condition (when last AM = '1')

Remarks

Writing of a register :

Registers 0, 1, ..., 34 can be loaded sequentially with only one start/stop condition followed by the sub-address of the first register desired.

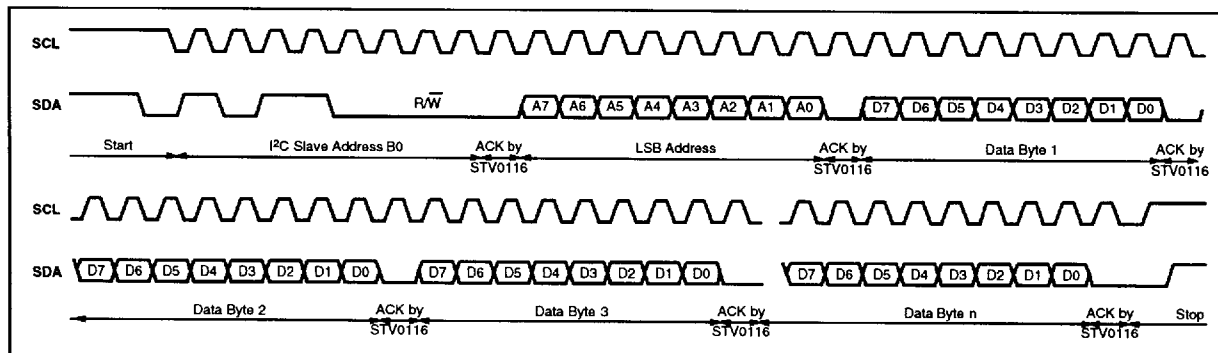
Example : Start followed by address b0 and sub-address 1 and then 3 bytes of data and stop : the cfg register will be loaded with the first byte and delay register will be loaded with the 2 others bytes.

Reading of a register :

Example 1 : Reading of register 35 (STATUS) : start followed by address b0 hex, AC = '0', then sub-address 35, AC = '0' and stop. Then start, address b1, AC = '0' and then data of register 35, AM = '1' and stop condition.

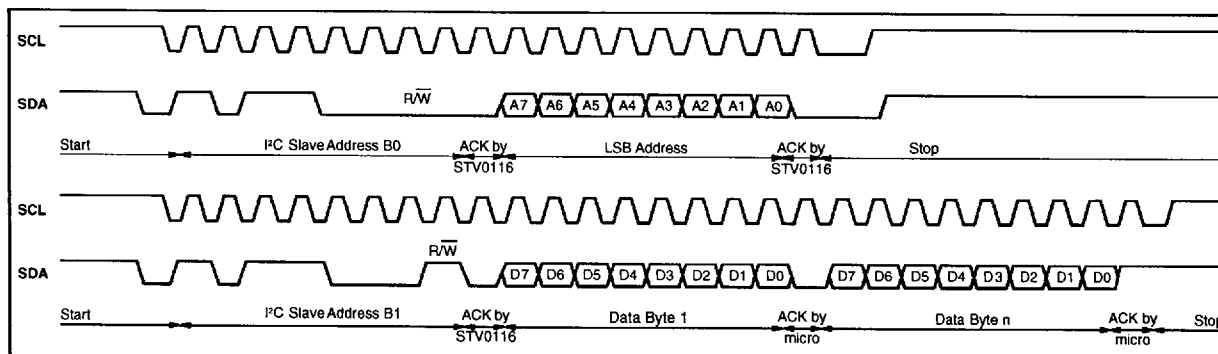
Example 2 : Reading of registers 0 to 3 : start followed by address b0 hex, AC = '0', and sub-address 0, AC = '0' and stop. Then start, address b1, AC = '0' and then first byte of register 0, AM = '0', second byte from register 1, AM = '0', third byte of register 2, AM = '0', fourth byte from register 3, AM = '1' and stop condition.

Figure 15 : STV0116/I²C Write Operation



0116-16.AI

Figure 16 : STV0116/I²C Read Operation



0116-17.EPS

REGISTERS MAPPING AND DESCRIPTION

(*) default mode on hard NRESET.

(**) default mode on TESTAUTO.

Register 0 Control (Read/Write)

| | | MSB | | | | | | LSB | |
|------------|------|---|--------------------|------|------|------|------|------|------|
| | | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 |
| Register 0 | | std1 | std0 | sym1 | sym0 | sys1 | sys0 | mod1 | mod0 |
| | std1 | std0 | Standard selection | | | | | | |
| (*) | 0 | 0 | PAL BDGHI | | | | | | |
| | 0 | 1 | PAL N Argentina | | | | | | |
| | 1 | 0 | NTSC M | | | | | | |
| | 1 | 1 | PAL M | | | | | | |
| | sym1 | Freerun | | | | | | | |
| (*) | 0 | Disable | | | | | | | |
| | 1 | Enable : free-run is active even if ODD/EVEN is incorrectly positioned (with a time constant of 3 consecutive lost frames) in slave mode. | | | | | | | |
| | sym0 | Frame synchronization source in slave mode | | | | | | | |
| (*) | 0 | ODD/EVEN input | | | | | | | |
| | 1 | YCRCB (extraction of F from EAV) | | | | | | | |
| | sys1 | Synchro : VCS polarity | | | | | | | |
| (*) | 0 | Positive | | | | | | | |
| | 1 | Negative | | | | | | | |
| | sys0 | Frame synchro : ODD/EVEN polarity (as input (slave) or as output (slave : synchro from EAV or master)) | | | | | | | |
| (*) | 0 | Synchro on ODD/EVEN falling edge | | | | | | | |
| | 1 | Synchro on ODD/EVEN rising edge | | | | | | | |
| | mod1 | No reset | | | | | | | |
| (*) | 0 | No reset | | | | | | | |
| | 1 | Software reset | | | | | | | |
| | mod0 | Slave | | | | | | | |
| (*) | 0 | Slave | | | | | | | |
| (**) | 1 | Master (freerun forced) | | | | | | | |

Note : Software reset is automatically disabled at I²C stop condition. Reset is active during 4 H27 periods.

REGISTERS MAPPING AND DESCRIPTION (continued)

Register 1 Cfg (Read/Write)

| | | MSB | | | | | | LSB | |
|------------|---------|---|---------|------|--------|------|----|-----|----|
| | | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 |
| Register 1 | | hsnvc | rstddfs | flt1 | syncok | coki | - | - | - |
| | hsnvc | Output signal selection on VCS | | | | | | | |
| (*) | 0 | Composite synchro | | | | | | | |
| | 1 | Horizontal synchro | | | | | | | |
| | rstddfs | Reset of DDFS (Direct Digital Frequency Synthesizer) | | | | | | | |
| | 0 to 1 | Transition generates a pulse reset for oscillator | | | | | | | |
| | 0 | | | | | | | | |
| | flt1 | Chroma pass band filter | | | | | | | |
| (*) | 1 | 1.3MHz, 0.45MHz for Q only | | | | | | | |
| | 0 | 1.8MHz | | | | | | | |
| | syncok | Synchro availability in case of no free-run active | | | | | | | |
| (*) | 0 | Synchro OFF | | | | | | | |
| | 1 | Synchro available (if sym1 = 0) | | | | | | | |
| | coki | Color kill | | | | | | | |
| (*) | 0 | Color ON | | | | | | | |
| | 1 | Color suppressed on C and CVBS (on CVBS only in next release) | | | | | | | |

Note : FOUR FILTERS FOR ENCODING NEEDS.
 Luma passband filter (6.3MHz (BW = 5.75MHz with sinX/X D/A conversion))
 Chroma passband filter (1.3MHz/1.8MHz : U/V and I, 1.8MHz/0.45MHz : Q, 1.8MHz : CR, CB for R, G, B encoding)
 (chroma BW becomes 1.2MHz/1.7MHz, 0.45MHz, 1.7MHz with sinX/X DAC).

Register 2 Delay_msb (Read/Write)

| | | MSB | | | | | | LSB | |
|------------|--|-----|----|----|----|----|----|-----|----|
| | | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 |
| Register 2 | | d10 | d9 | d8 | d7 | d6 | d5 | d4 | d3 |

Register 3 Delay_lsb

| | | MSB | | | | | | LSB | |
|---------------------|--|-----|----|----|----------|----------|----------|----------|----------|
| | | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 |
| <i>Read Mode :</i> | | | | | | | | | |
| Register 3 | | d2 | d1 | d0 | Reg2, d4 | Reg2, d3 | Reg2, d2 | Reg2, d1 | Reg2, d0 |
| <i>Write Mode :</i> | | | | | | | | | |
| Register 3 | | d2 | d1 | d0 | xx | xx | xx | xx | xx |

d[10:0] sample polynomial counter at 27MHz
 Sample polynomial counter $(1 + x^2 + x^{11})$ value on which falling edge of F (ODD/EVEN signal) is detected on YCRCB (F is extracted from EAV word)

1st byte : 21 (hex 15), 2nd byte : 128 (hex 80) for PAL BDGHIN (625 lines)
 1st byte : 201 (hex c9), 2nd byte : 128 (hex 80) for M (525 lines)

Sample polynomial counter value on which falling edge of ODD/EVEN is detected

(*) 1st byte : 0, 2nd byte : 32 (hex 20) for PAL BDGHIN (625 lines)
 1st byte : 0, 2nd byte : 32 (hex 20) for M (525 lines)

Note : Delay register should be loaded before Control register for synchro on YCRCB cross table of sample polynomial counter is given cech.txt file.

REGISTERS MAPPING AND DESCRIPTION (continued)

Register Increment for ddfs (Digital Frequency Synthesizer) (Read/Write)

| | MSB | | | | | | | LSB (see Note) |
|------------|-----|-----|-----|-----|-----|-----|-----|-------------------|
| | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 |
| Register 4 | xx | xx | d21 | d20 | d19 | d18 | d17 | d16 |
| Register 5 | d15 | d14 | d13 | d12 | d11 | d10 | d9 | d8 |
| Register 6 | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 |

- (*) Reset value depends on standard chosen in register 0
- xx0010000111110000011111NTSC M $f = 3.5795452\text{MHz}$ error = +0.2Hz
 $f_{th} = 3579545 \pm 10\text{Hz}$
 - xx0010101000001001100011PALBGHI $f = 4.4336206\text{MHz}$ error = +1.85Hz
 $f_{th} = 4433618.75 \pm 5\text{Hz}$
 - xx0010000111110110100101PALN $f = 3.5820558\text{MHz}$ error = -0.45Hz
 $f_{th} = 3582056.25 \pm 5\text{Hz}$
 - xx0010000111100110111100PALM $f = 3.5756120\text{MHz}$ error = +0.51Hz
 $f_{th} = 3575611.49 \pm 5\text{Hz}$

Note : 1 LSB = 6.43Hz

Register Phase Offset for ddfs (Digital Frequency Synthesizer) (Read/Write)

| | MSB | | | | | | | LSB |
|------------|-----|-----|-----|-----|-----|-----|-----|-----|
| | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 |
| Register 7 | xx | xx | o21 | o20 | o19 | o18 | o17 | o16 |
| Register 8 | o15 | o14 | o13 | o12 | o11 | o10 | o9 | o8 |
| Register 9 | o7 | o6 | o5 | o4 | o3 | o2 | o1 | o0 |

- (*) Reset value depends on standard chosen in register 0

REGISTERS MAPPING AND DESCRIPTION (continued)**Register Palety** (Read/Write)

| | MSB | | | | | | | LSB |
|--------------------|----------|----------|-----|-----|-----|-----|-----|-----|
| | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 |
| <i>Read Mode :</i> | | | | | | | | |
| Register 10 | Reg10,d5 | Reg10,d5 | y75 | y74 | y73 | y72 | y71 | y70 |
| Register 11 | Reg11,d5 | Reg11,d5 | y65 | y64 | y63 | y62 | y61 | y60 |
| Register 12 | Reg12,d5 | Reg12,d5 | y55 | y54 | y53 | y52 | y51 | y50 |
| Register 13 | Reg13,d5 | Reg13,d5 | y45 | y44 | y43 | y42 | y41 | y40 |
| Register 14 | Reg14,d5 | Reg14,d5 | y35 | y34 | y33 | y32 | y31 | y30 |
| Register 15 | Reg15,d5 | Reg15,d5 | y25 | y24 | y23 | y22 | y21 | y20 |
| Register 16 | Reg16,d5 | Reg16,d5 | y15 | y14 | y13 | y12 | y11 | y10 |
| Register 17 | Reg17,d5 | Reg17,d5 | y05 | y04 | y03 | y02 | y01 | y00 |

Write Mode :

| | | | | | | | | |
|-----------------------------------|----|----|-----|-----|-----|-----|-----|-----|
| Register 10 | xx | xx | y75 | y74 | y73 | y72 | y71 | y70 |
| Register 11 | xx | xx | y65 | y64 | y63 | y62 | y61 | y60 |
| Register 12 | xx | xx | y55 | y54 | y53 | y52 | y51 | y50 |
| Register 13 | xx | xx | y45 | y44 | y43 | y42 | y41 | y40 |
| Register 14 | xx | xx | y35 | y34 | y33 | y32 | y31 | y30 |
| Register 15 | xx | xx | y25 | y24 | y23 | y22 | y21 | y20 |
| Register 16 | xx | xx | y15 | y14 | y13 | y12 | y11 | y10 |
| Register 17 NTSC | xx | xx | y05 | y04 | y03 | y02 | y01 | y00 |
| Register 17 PAL (to be loaded) | xx | xx | 0 | 0 | 0 | 1 | 0 | 0 |

8 x 6 bit words for Y component.

| Default Value : | R0, B0, C0 | Y(hexa) | Color | (100% white to black) |
|-----------------|------------|---------|---------|-----------------------|
| | 111 | 3B | white | y7x |
| | 110 | 28 | yellow | y6x |
| | 101 | 14 | magenta | y5x |
| | 100 | 10 | red | y4x |
| | 011 | 21 | cyan | y3x |
| | 010 | 1D | green | y2x |
| | 001 | 09 | blue | y1x |
| | 000 | 04 | black | y0x |

REGISTERS MAPPING AND DESCRIPTION (continued)**Register Paletcr** (Read/Write)

| | MSB | | | | | | | LSB |
|---------------------|----------|----------|------|------|------|------|------|------|
| | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 |
| <i>Read Mode :</i> | | | | | | | | |
| Register 18 | Reg18,d5 | Reg18,d5 | cr75 | cr74 | cr73 | cr72 | cr71 | cr70 |
| Register 19 | Reg19,d5 | Reg19,d5 | cr65 | cr64 | cr63 | cr62 | cr61 | cr60 |
| Register 20 | Reg20,d5 | Reg20,d5 | cr55 | cr54 | cr53 | cr52 | cr51 | cr50 |
| Register 21 | Reg21,d5 | Reg21,d5 | cr45 | cr44 | cr43 | cr42 | cr41 | cr40 |
| Register 22 | Reg22,d5 | Reg22,d5 | cr35 | cr34 | cr33 | cr32 | cr31 | cr30 |
| Register 23 | Reg23,d5 | Reg23,d5 | cr25 | cr24 | cr23 | cr22 | cr21 | cr20 |
| Register 24 | Reg24,d5 | Reg24,d5 | cr15 | cr14 | cr13 | cr12 | cr11 | cr10 |
| Register 25 | Reg25,d5 | Reg25,d5 | cr05 | cr04 | cr03 | cr02 | cr01 | cr00 |
| <i>Write Mode :</i> | | | | | | | | |
| Register 18 | xx | xx | cr75 | cr74 | cr73 | cr72 | cr71 | cr70 |
| Register 19 | xx | xx | cr65 | cr64 | cr63 | cr62 | cr61 | cr60 |
| Register 20 | xx | xx | cr55 | cr54 | cr53 | cr52 | cr51 | cr50 |
| Register 21 | xx | xx | cr45 | cr44 | cr43 | cr42 | cr41 | cr40 |
| Register 22 | xx | xx | cr35 | cr34 | cr33 | cr32 | cr31 | cr30 |
| Register 23 | xx | xx | cr25 | cr24 | cr23 | cr22 | cr21 | cr20 |
| Register 24 | xx | xx | cr15 | cr14 | cr13 | cr12 | cr11 | cr10 |
| Register 25 | xx | xx | cr05 | cr04 | cr03 | cr02 | cr01 | cr00 |

8 x 6 bit words for CR component.

| Default Value : | R0, B0, C0 | CR(hexa) | Color | (75% white to black) |
|-----------------|------------|----------|---------|----------------------|
| | 111 | 20 | white | cr7x |
| | 110 | 23 | yellow | cr6x |
| | 101 | 31 | magenta | cr5x |
| | 100 | 35 | red | cr4x |
| | 011 | 0B | cyan | cr3x |
| | 010 | 0E | green | cr2x |
| | 001 | 1C | blue | cr1x |
| | 000 | 20 | black | cr0x |

REGISTERS MAPPING AND DESCRIPTION (continued)**Register Paletcb** (Read/Write)

| | MSB | | | | | | | LSB |
|---------------------|----------|----------|------|------|------|------|------|------|
| | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 |
| <i>Read Mode :</i> | | | | | | | | |
| Register 26 | Reg26,d5 | Reg26,d5 | cb75 | cb74 | cb73 | cb72 | cb71 | cb70 |
| Register 27 | Reg27,d5 | Reg27,d5 | cb65 | cb64 | cb63 | cb62 | cb61 | cb60 |
| Register 28 | Reg28,d5 | Reg28,d5 | cb55 | cb54 | cb53 | cb52 | cb51 | cb50 |
| Register 29 | Reg29,d5 | Reg29,d5 | cb45 | cb44 | cb43 | cb42 | cb41 | cb40 |
| Register 30 | Reg30,d5 | Reg30,d5 | cb35 | cb34 | cb33 | cb32 | cb31 | cb30 |
| Register 31 | Reg31,d5 | Reg31,d5 | cb25 | cb24 | cb23 | cb22 | cb21 | cb20 |
| Register 32 | Reg32,d5 | Reg32,d5 | cb15 | cb14 | cb13 | cb12 | cb11 | cb10 |
| Register 33 | Reg33,d5 | Reg33,d5 | cb05 | cb04 | cb03 | cb02 | cb01 | cb00 |
| <i>Write Mode :</i> | | | | | | | | |
| Register 26 | xx | xx | cb75 | cb74 | cb73 | cb72 | cb71 | cb70 |
| Register 27 | xx | xx | cb65 | cb64 | cb63 | cb62 | cb61 | cb60 |
| Register 28 | xx | xx | cb55 | cb54 | cb53 | cb52 | cb51 | cb50 |
| Register 29 | xx | xx | cb45 | cb44 | cb43 | cb42 | cb41 | cb40 |
| Register 30 | xx | xx | cb35 | cb34 | cb33 | cb32 | cb31 | cb30 |
| Register 31 | xx | xx | cb25 | cb24 | cb23 | cb22 | cb21 | cb20 |
| Register 32 | xx | xx | cb15 | cb14 | cb13 | cb12 | cb11 | cb10 |
| Register 33 | xx | xx | cb05 | cb04 | cb03 | cb02 | cb01 | cb00 |

8 x 6 bit words for CB component.

| Default Value : | R0, B0, C0 | CB(hexa) | Color | (75% white to black) |
|-----------------|------------|----------|---------|----------------------|
| | 111 | 20 | white | cb7x |
| | 110 | 0B | yellow | cb6x |
| | 101 | 2E | magenta | cb5x |
| | 100 | 19 | red | cb4x |
| | 011 | 27 | cyan | cb3x |
| | 010 | 12 | green | cb2x |
| | 001 | 35 | blue | cb1x |
| | 000 | 20 | black | cb0x |

REGISTERS MAPPING AND DESCRIPTION (continued)**Register 35 Status** (Read)

| | | MSB | | | | | | LSB | |
|-------------|------|--|--------------------|------|------|------|------|------|------|
| | | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 |
| Register 35 | | hok | atfr | std1 | std0 | sym1 | sym0 | sys1 | sys0 |
| | hok | Hamming decoding of ODD/EVEN signal from YCRCB | | | | | | | |
| | 0 | Multiple errors | | | | | | | |
| | 1 | 0 or 1 error | | | | | | | |
| | atfr | Frame synchronization flag | | | | | | | |
| | 0 | Encoder not synchronized | | | | | | | |
| | 1 | In slave mode : encoder synchronized | | | | | | | |
| | std1 | std0 | Standard selection | | | | | | |
| (*) | 0 | 0 | PAL BDGHI | | | | | | |
| | 0 | 1 | PALN (Argentina) | | | | | | |
| | 1 | 0 | NTSC M | | | | | | |
| | 1 | 1 | PALM | | | | | | |
| | sym1 | Freerun | | | | | | | |
| (*) | 0 | Disable | | | | | | | |
| | 1 | Enable : free-run is active in case of ODD/EVEN suppression (with a time constant of 3 consecutive lost of frame) and slave mode | | | | | | | |
| | sym0 | Frame synchronization source in slave mode | | | | | | | |
| (*) | 0 | ODD/EVEN input | | | | | | | |
| | 1 | YCRCB (extraction of F from EAV) | | | | | | | |
| | sys1 | Synchro : VCS polarity | | | | | | | |
| (*) | 0 | Positive | | | | | | | |
| | 1 | Negative | | | | | | | |
| | sys0 | Frame synchro : ODD/EVEN polarity | | | | | | | |
| (*) | 0 | Synchro on ODD/EVEN falling edge | | | | | | | |
| | 1 | Synchro on ODD/EVEN rising edge | | | | | | | |

Note : SIGNAL QUALITY DETECTOR by use of hamming decoding on EAV, SAV in YCRCB input.

Register Compression (Read/Write)

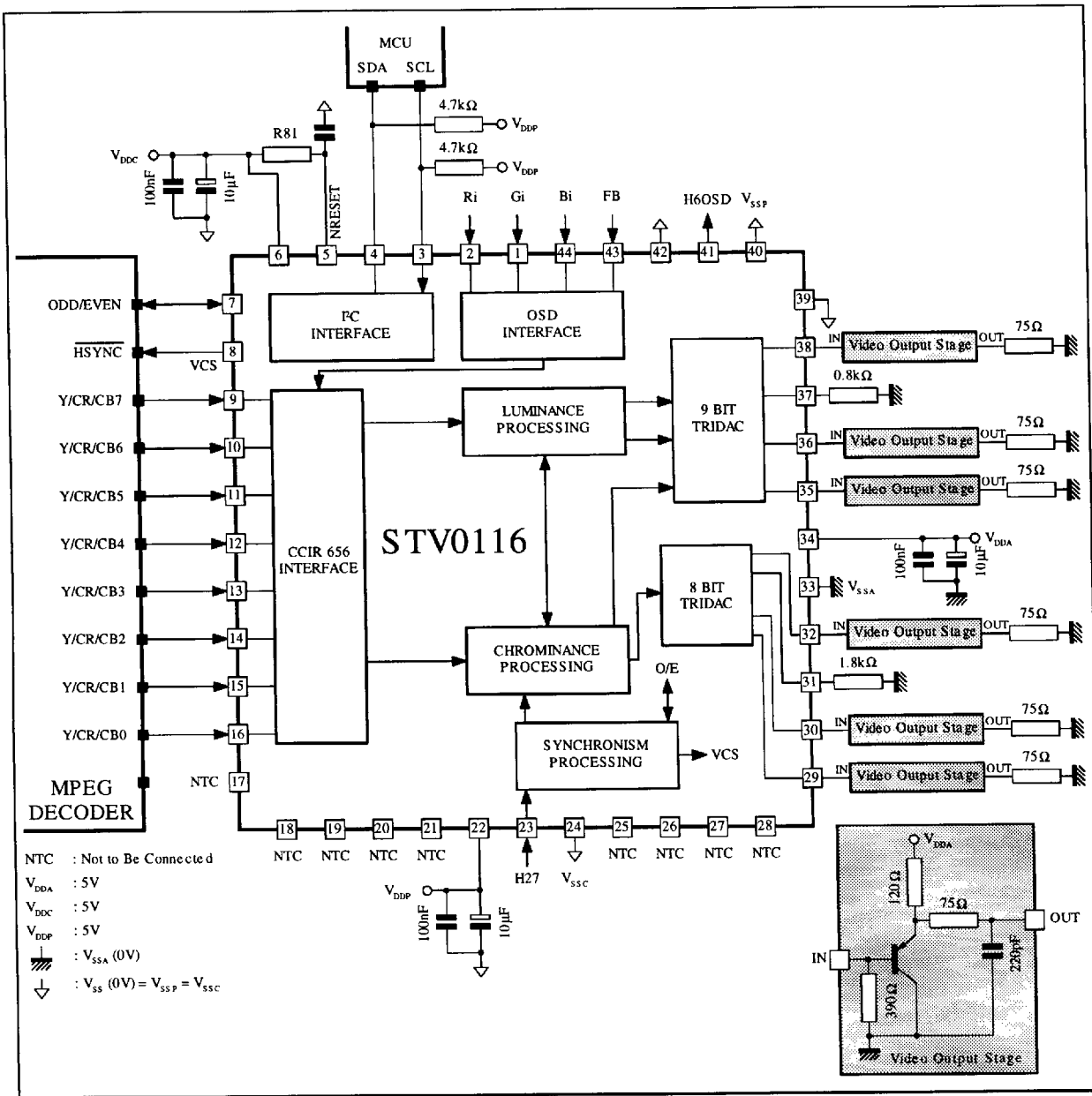
| | | MSB | | | | | | LSB | |
|---------------------|--|-----|-----|-----|-----|-----|-----|-----|-----|
| | | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 |
| <i>Read Mode :</i> | | | | | | | | | |
| Register 36 | | lf9 | lf8 | lf7 | lf6 | lf5 | lf4 | lf3 | lf2 |
| Register 37 | | lf1 | lf0 | lc9 | lc8 | lc7 | lc6 | lc5 | lc4 |
| Register 38 | | lc3 | lc2 | lc1 | lc0 | 0 | 0 | 0 | 0 |
| <i>Write Mode :</i> | | | | | | | | | |
| Register 36 | | lf9 | lf8 | lf7 | lf6 | lf5 | lf4 | lf3 | lf2 |
| Register 37 | | lf1 | lf0 | lc9 | lc8 | lc7 | lc6 | lc5 | lc4 |
| Register 38 | | lc3 | lc2 | lc1 | lc0 | x | x | x | x |

It is used to compress on line fonctionnal patterns.

"lc" is the line number value* on which the polynomial line counter ($1 + x^3 + x^{10}$) is forced (when it occurs) with 'lf' value.

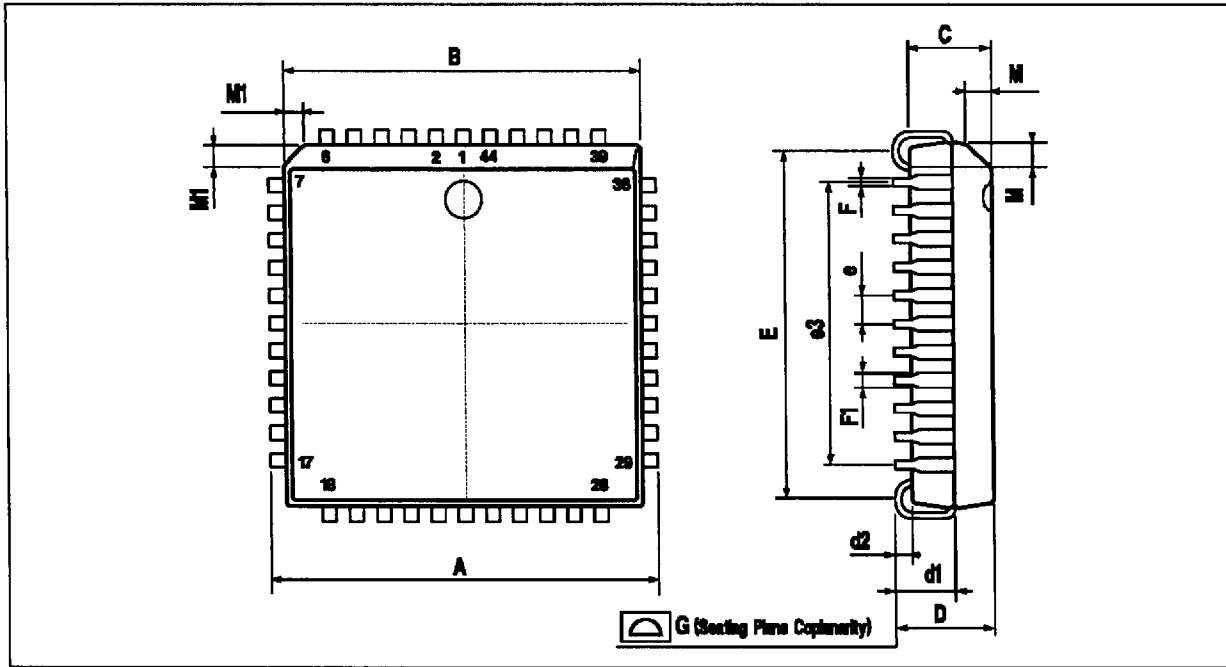
- (*) On reset 'lf' = 001, 'lc' = 000 (line counter never goes to 000 value)
1st byte : 00, 2nd byte : 40 hex, 3rd byte : 00

APPLICATION DIAGRAM



0116-03 EPS

PACKAGE MECHANICAL DATA
44 PINS - PLASTIC CHIP CARRIER



PMPLCC44.EPS

| Dimensions | Millimeters | | | Inches | | |
|------------|-------------|------|-------|--------|-------|-------|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 17.4 | | 17.65 | 0.685 | | 0.695 |
| B | 16.51 | | 16.65 | 0.650 | | 0.656 |
| C | 3.65 | | 3.7 | 0.144 | | 0.146 |
| D | 4.2 | | 4.57 | 0.165 | | 0.180 |
| d1 | 2.59 | | 2.74 | 0.102 | | 0.108 |
| d2 | | 0.68 | | | 0.027 | |
| E | 14.99 | | 16 | 0.590 | | 0.630 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 12.7 | | | 0.500 | |
| F | | 0.46 | | | 0.018 | |
| F1 | | 0.71 | | | 0.028 | |
| G | | | 0.101 | | | 0.004 |
| M | | 1.16 | | | 0.046 | |
| M1 | | 1.14 | | | 0.045 | |

PLCC44.TBL

Information furnished is believed to be accurate and reliable. However, SGS-THOMSON Microelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No licence is granted by implication or otherwise under any patent or patent rights of SGS-THOMSON Microelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. SGS-THOMSON Microelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of SGS-THOMSON Microelectronics.

© 1996 SGS-THOMSON Microelectronics - All Rights Reserved

Purchase of μ C Components of SGS-THOMSON Microelectronics, conveys a license under the Philips μ C Patent. Rights to use these components in a μ C system, is granted provided that the system conforms to the μ C Standard Specifications as defined by Philips.

SGS-THOMSON Microelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - France - Germany - Hong Kong - Italy - Japan - Korea - Malaysia - Malta - Morocco
The Netherlands - Singapore - Spain - Sweden - Switzerland - Taiwan - Thailand - United Kingdom - U.S.A.