MX23C8111

8M-BIT MASK ROM (8/16 BIT OUTPUT)

FEATURES

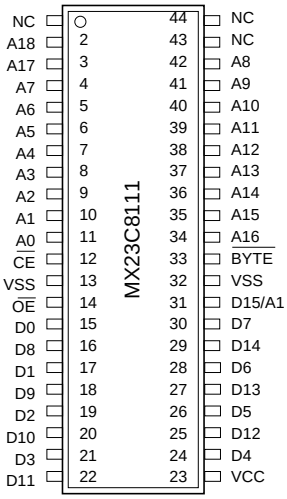
- Bit organization
  - 1M x 8 (byte mode)
  - 512K x 16 (word mode)
- Fast access time
  - Random access: 95ns (max.)
  - Page access: 50ns (max.)
- Current
  - Operating: 60mA
  - Standby: 100uA
- Supply voltage
  - 5V±10%
- Package
  - 44 pin SOP (500mil)
  - 42 pin PDIP (600mil)

ORDER INFORMATION

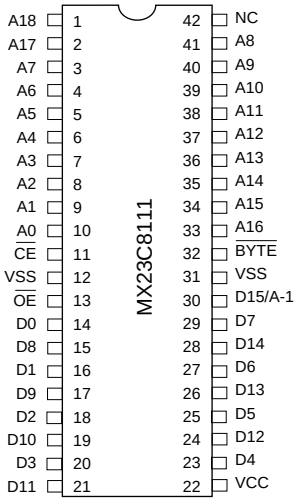
Part No.	Access Time	Page Access Time	Package
MX23C8111MC-95	95ns	50ns	44 pin SOP
MX23C8111MC-10	100ns	50ns	44 pin SOP
MX23C8111MC-12	120ns	60ns	44 pin SOP
MX23C8111PC-95	95ns	50ns	42 pin PDIP
MX23C8111PC-10	100ns	50ns	42 pin PDIP
MX23C8111PC-12	120ns	60ns	42 pin PDIP

PIN CONFIGURATION

44 SOP



42 PDIP



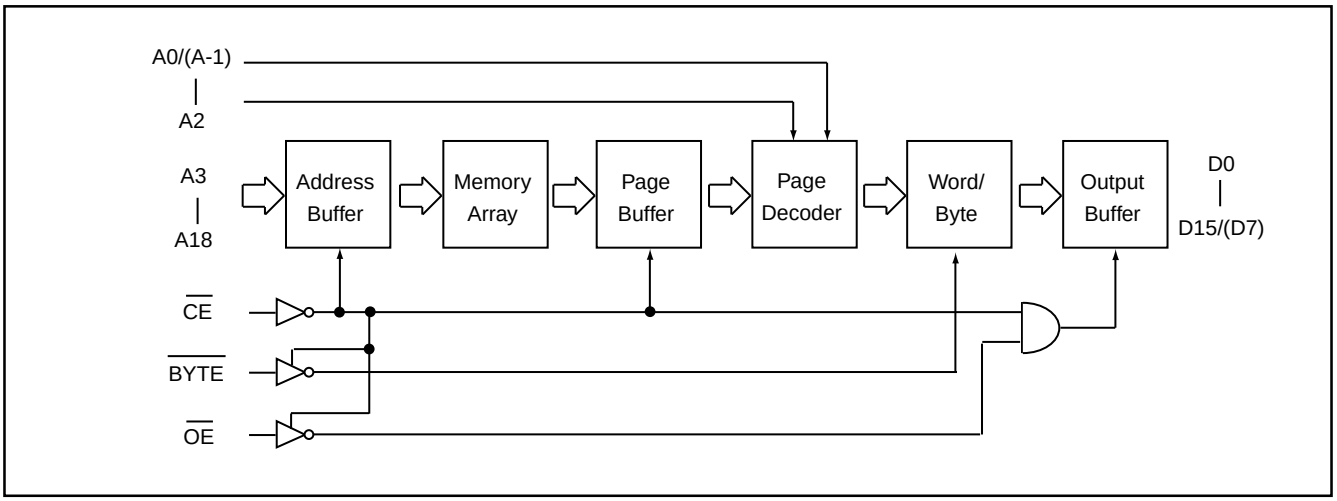
PIN DESCRIPTION

Symbol	Pin Function
A0~A18	Address Inputs
D0~D7	Data Outputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
VCC	Power Supply Pin
VSS	Ground Pin
NC	No Connection

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{Byte}$	D15/A-1	D0~D7	D8~D15	Mode	Power
H	X	X	X	High Z	High Z	-	Stand-by
L	H	X	X	High Z	High Z	-	Active
L	L	H	Output	D0~D7	D8~D15	Word	Active
L	L	L	Input	D0~D7	High Z	Byte	Active

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings
Voltage on any Pin Relative to VSS	VCC	-0.3V to 7.0V
Input Voltage	VI	-0.3V to VCC + 0.5V
Output Voltage	VO	-0.3V to VCC + 0.5V
Ambient Operating Temperature	Topr	0℃ to 70℃
Storage Temperature	Tstg	-65℃ to 125℃

DC CHARACTERISTICS (Ta = 0℃ ~ 70℃, VCC = 5V±10%)

Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	2.4V	-	IOH = -1.0mA
Output Low Voltage	VOL	-	0.4V	IOL = 2.1mA
Input High Voltage	VIH	2.2V	VCC+0.3V	
Input Low Voltage	VIL	-0.3V	0.8V	
Input Leakage Current	ILI	-	10uA	0V, VCC
Output Leakage Current	ILO	-	10uA	0V, VCC
Operating Current	ICC1	-	60mA	f=10MHz, all output open
Standby Current (TTL)	ISTB1	-	1mA	$\overline{CE}$=VIH
Standby Current (CMOS)	ISTB2	-	100uA	$\overline{CE}$> VCC - 0.2V
Input Capacitance	CIN	-	10pF	Ta = 25℃, f = 1MHZ
Output Capacitance	COUT	-	10pF	Ta = 25℃, f = 1MHZ

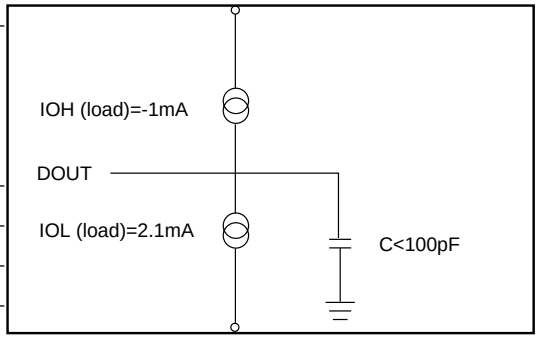
AC CHARACTERISTICS (Ta = 0℃ ~ 70℃, VCC = 5V±10%)

Item	Symbol	23C8111-95		23C8111-10		23C8111-12	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
Read Cycle Time	tRC	95ns	-	100ns	-	120ns	-
Address Access Time	tAA	-	90ns	-	100ns	-	120ns
Chip Enable Access Time	tACE	-	95ns	-	100ns	-	120ns
Page Mode Access Time	tPA	-	50ns	-	50ns	-	60ns
Output Enable Time	tOE	-	50ns	-	50ns	-	60ns
Output Hold After Address	tOH	0ns	-	0ns	-	0ns	-
Output High Z Delay	tHZ	-	20ns	-	20ns	-	20ns

Note:Output high-impedance delay (tHZ) is measured from $\overline{OE}$ or $\overline{CE}$ going high, and this parameter guaranteed by design over the full voltage and temperature operating range - not tested.

AC Test Conditions

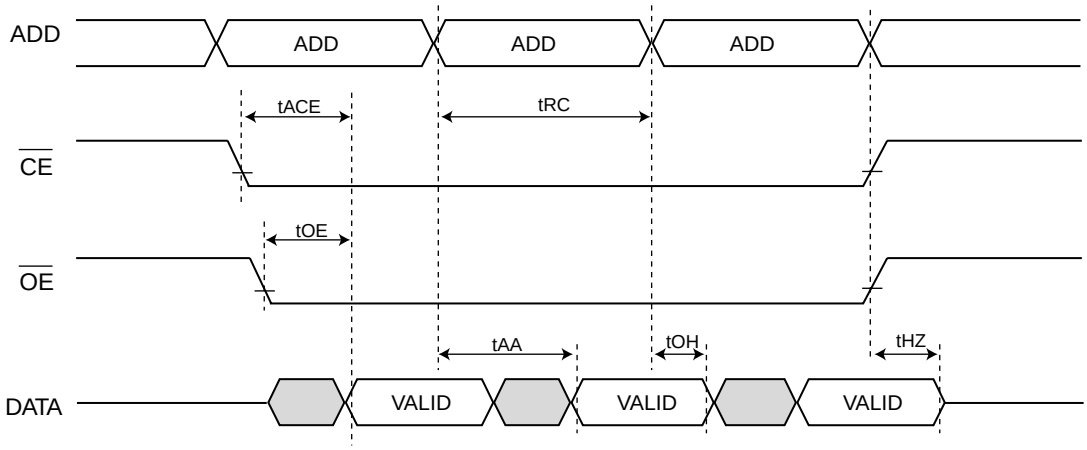
Input Pulse Levels	0.4V~2.7V for 95ns and 100ns speed grade 0.4V~2.4V for 120ns speed grade
Input Rise and Fall Times	10ns
Input Timing Level	1.5V
Output Timing Level	0.8V and 2.0V
Output Load	See Figure



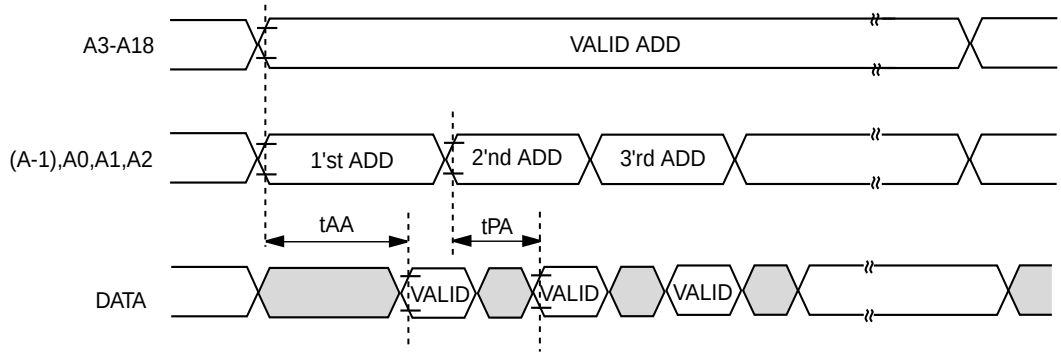
Note:No output loading is present in tester load board.
Active loading is used and under software programming control.
Output loading capacitance includes load board's and all stray capacitance.

TIMING DIAGRAM

Access Timing (Normal Access)



Page Read

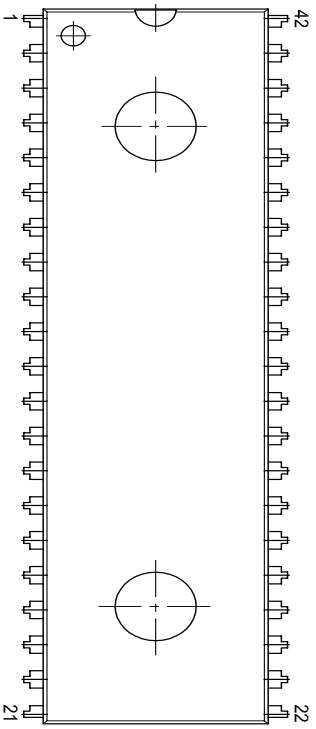


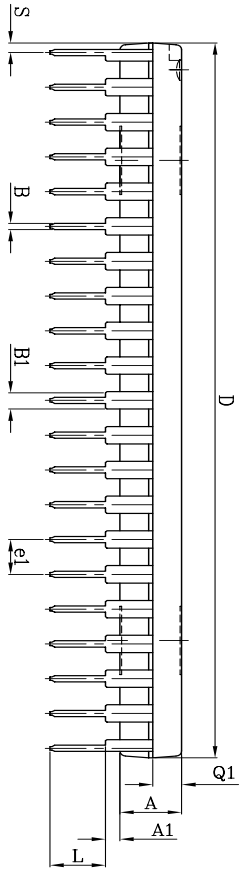
Note: $\overline{CE}$, $\overline{OE}$ are enable.

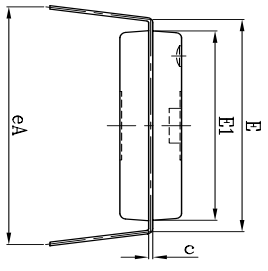
Page size is 8 words in 16-bit mode, 16 bytes in 8-bit mode.

PACKAGE INFORMATION

42-PIN PLASTIC DIP(600 mil)



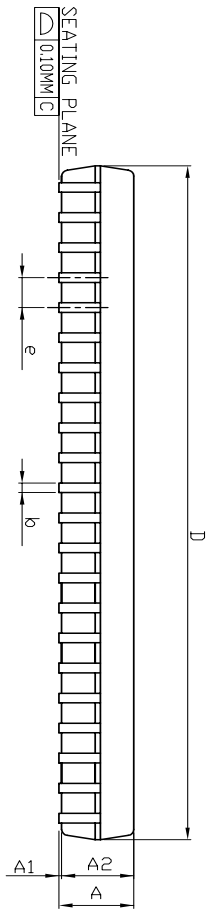


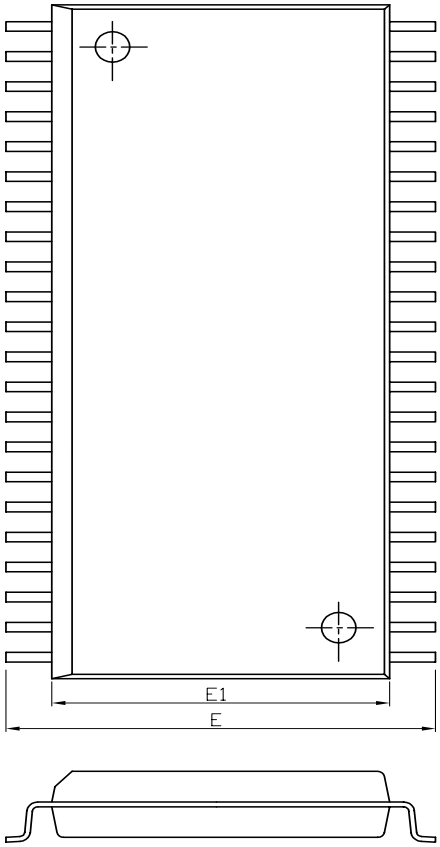


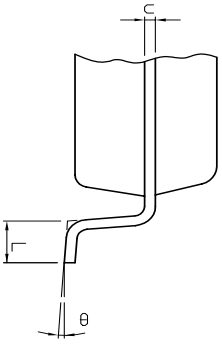
SYMBOL / UNIT	INCH(BASE)	MM(REF.)
A	0.155±0.008	3.937±0.203
A1	0.025±0.005	0.635±0.127
B	0.018 (REF.)	0.457 (REF.)
B1	0.050 (REF.)	1.270 (REF.)
c	0.010 (REF.)	0.254 (REF.)
D	2.05±0.005	52.07±0.127
E	0.600±0.005	15.240±0.127
E1	0.550±0.005	13.970±0.127
e1	0.100(REF.)	2.540 (REF.)
eA	0.650±0.030	16.510±0.762
L	0.13	3.30
Q1	0.0725±0.005	1.8415±0.127
S	0.025±0.005	0.635±0.127

旺宏電子股份有限公司 Macronix International Co., Ltd.			DWG. NO. 6110-0202.5
TITLE PACKAGE OUTLINE FOR PDIP 42L (600 MIL)			TOLERANCE .X ± .XX ±.01 ANGLE .XXX±.002
DRAWN	APPROVED	DATE	UNIT
C.L.Chiang	Leo Lee	05-02-'01	
			REVISION 4

44-PIN PLASTIC SOP







Symbol	Dimension in mm (Base)			Dimension in inch (Ref.)		
	Min	Nom	Max	Min	Nom	Max
A	—	—	3.00	—	—	0.118
A1	0.10	—	—	0.004	—	—
A2	2.57	2.69	2.82	0.101	0.106	0.111
b		0.41REF			0.016 REF	
c		0.20 REF			0.008 REF	
D	28.37	28.50	28.63	1.117	1.122	1.127
E	15.77	16.03	16.28	0.621	0.631	0.641
E1	12.47	12.60	12.73	0.491	0.496	0.501
e		1.27 REF			0.050 REF	
L	0.58	0.79	0.99	0.023	0.031	0.039
θ	—	5°	—	—	5°	—

REFERENCE DOCUMENT: JEDEC SPEC MO-175

旺宏電子股份有限公司				DWG. NO.
Macronix International Co., Ltd.				6110-0207
TITLE				TOLERANCE
PACKAGE OUTLINE FOR SOP 44L (500 MIL)				.X ±.1 ANGLE .XX ±.01 ROUGHNESS .XXX±.002
DRAWN	APPROVED	DATE	UNIT	REVISION
C.L.Chiang	Rick Chiu	11-08-'01	INCH	3

REVISION HISTORY

REVISION	DESCRIPTION	PAGE	DATE
2.1	AC Characteristics: tOH--10ns --> 0ns	P3	JAN/29/1999
2.2	Modify Package Information	P5,6	NOV/22/2001

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