This datasheet is under modification and could not be completed in time for this CD-ROM. Before designing in, please be so kind as to contact your nearest OKI office or representative. The revised datasheet will be included in the next CD-ROM issue. Please also watch our web sites for further announcements. We sincerely apologise for any inconveniences.

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# OKI Semiconductor

# MSM64164C

**Built-in RC Oscillator type A/D Converter and LCD Driver 4-Bit Microcontroller**

## GENERAL DESCRIPTION

The MSM64164C is a low power 4-bit microcontroller using OKI original CPU core nX-4/20. The MSM64164C has the minimum instruction execution time of 7.5 µs (@400 kHz) and has internal 4064-byte program memory, 256-nibble data memory, three 4-bit input-output ports, 4-bit input port, 4-bit output port, 2-channel RC oscillation, A/D converter, LCD driver for up to 120 segments, and buzzer output port.
The MSM64164C is best suited for low power, high precision thermometers and hygrometers.

## FEATURES

- Operating range
  - Operating frequencies : 32.768kHz, 400 kHz
  - Operating voltage : 1.25 to 1.7 V (1.5 V spec.)<br>2.0 to 3.5 V (3 V spec.)<br>2.2 to 3.5 V (1/2 duty)
  - Operating temperature : –40 to +85°C
- Memory space
  - Internal program memory : 4064 bytes
  - Internal data memory : 256 nibbles
- Minimum instruction execution time : 7.5 µs @400 kHz<br>91.6 µs @32.768kHz
- RC oscillation A/D converter : 2 channels<br>Time dividing 2-channel method
- LCD driver : 34; duty ratio switchable by software
  - (1) At 1/4 duty and 1/3 bias : 120 segments (max)
  - (2) At 1/3 duty and 1/3 bias : 93 segments (max)
  - (3) At 1/2 duty and 1/2 bias : 64 segments (max)
- Buzzer driver : 1 (4 output modes selectable)
- Capture register : 2 channels
- Watchdog timer
- Clock : 32.768kHz crystal oscillator and 400 kHz RC oscillator (with an external resistor)
  - CPU clock : 32.768kHz/400 kHz (switchable by software)
  - Time base clock : 32.768kHz
- Power supply voltage : 1.5 V/3 V (selectable by mask option)<br>Low power consumption
- I/O port
  - Input-output port : 3 ports × 4 bits
  - Input port : 1 port × 4 bits
  - Output port : 1 port × 4 bits<br>(8 out of the 34 LCD driver outputs can be used for another output-only port by mask option.)
- Interrupt
  - External interrupt : 2 sources
  - Internal interrupt : 8 sources

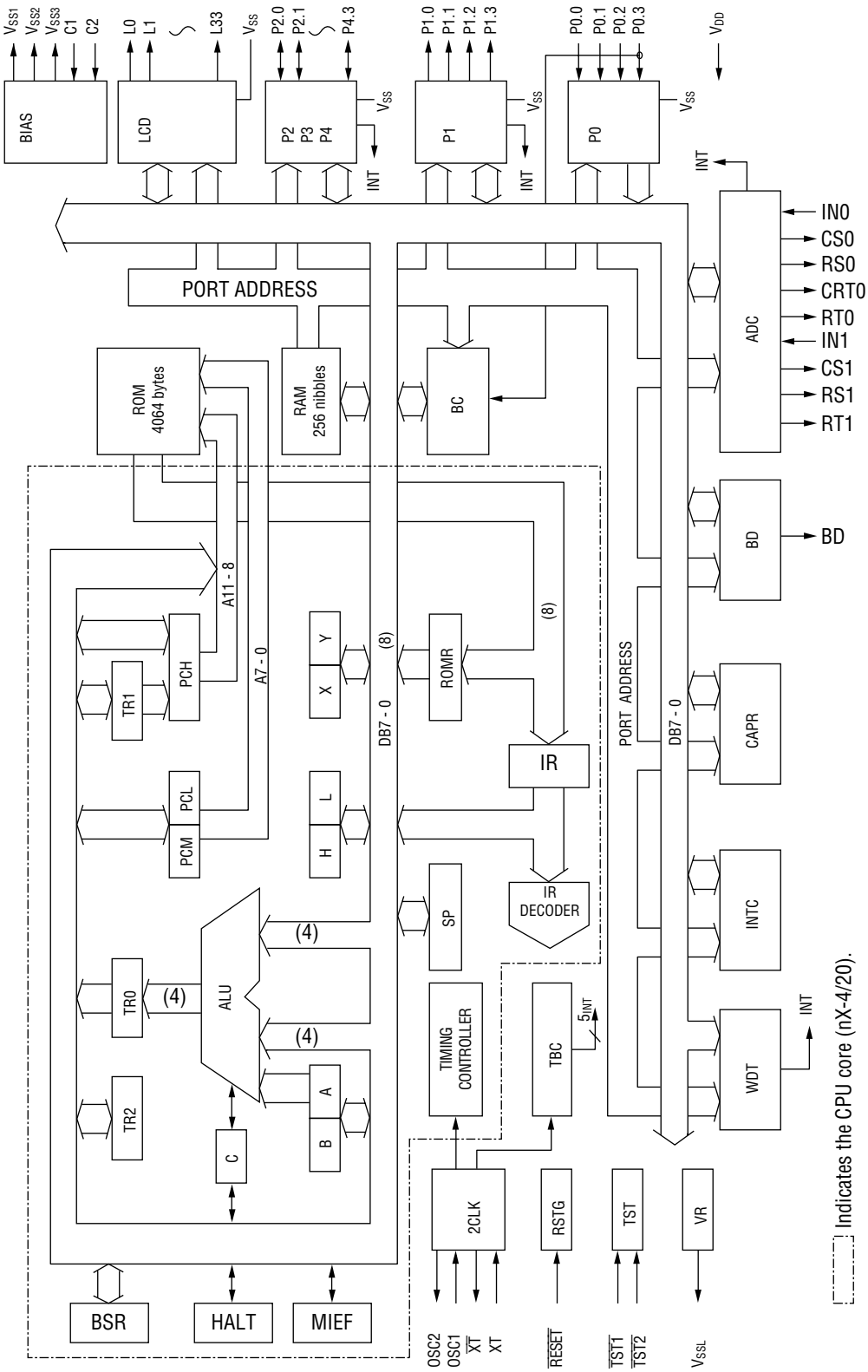
- Package options:

| | | |
|---|---|---|
| MSM64164C-xxx | : | Chip |
| MSM64164C-xxxGS-BK | : | QFP80-1420-0.80-BK (Biphenyl epoxy resin) |
| MSM64164C-xxxGS-K | : | QFP80-1414-0.65-K (Biphenyl epoxy resin) |
| MSM64164C-xxxTS-K | : | TQFP80-1212-0.50-K |

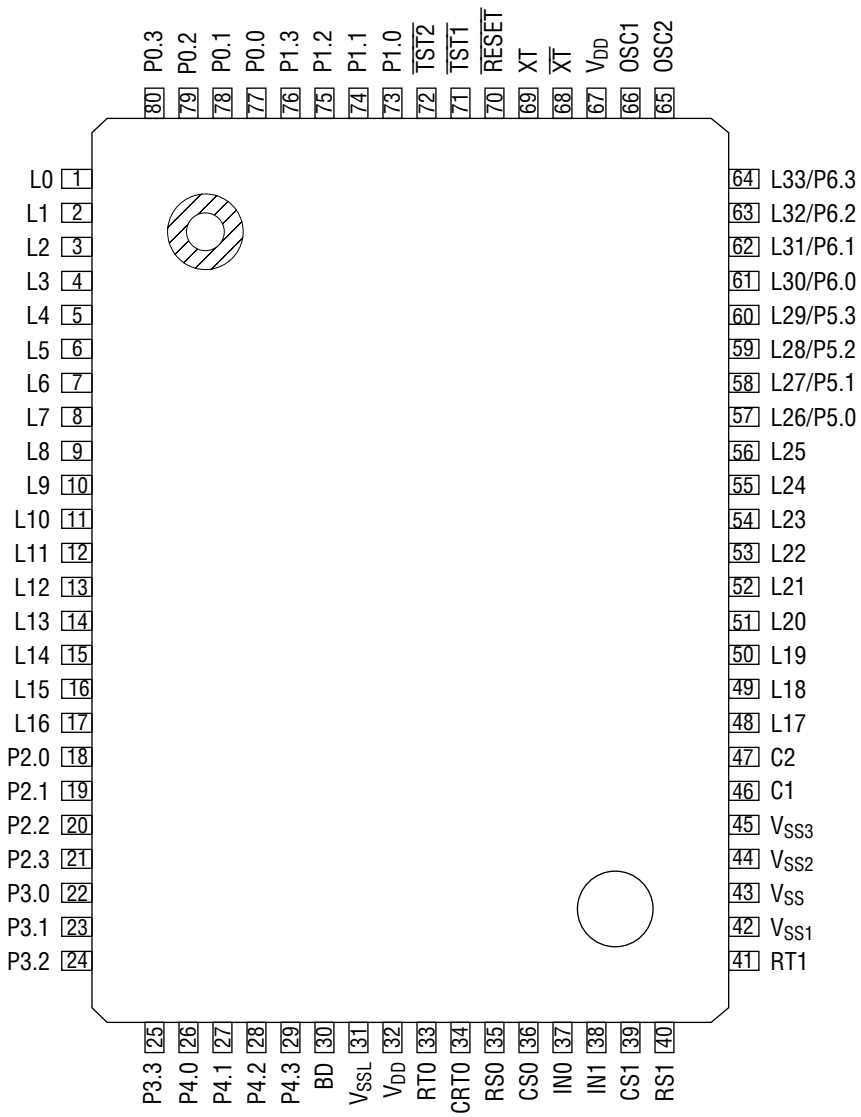
- OTP version

  MSM64P164 (Replaced the built-in program memory with one-time PROM)

## BLOCK DIAGRAM



## PIN CONFIGURATION (TOP VIEW)

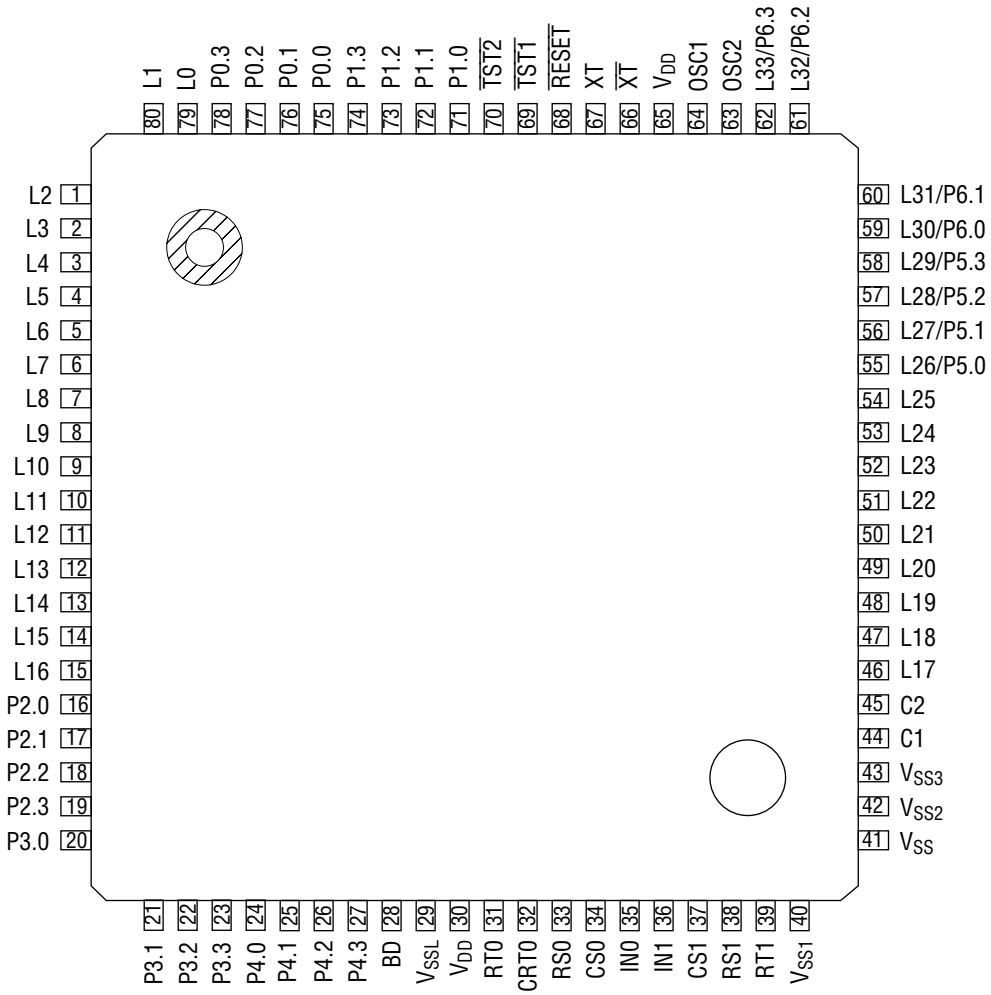



**(QFP80-1420-0.80-BK)**

**80-Pin Plastic QFP**

Note: Pin 32 and pin 67 are internally connected and $V_{DD}$ can be supplied from either pin 32 or pin 67.

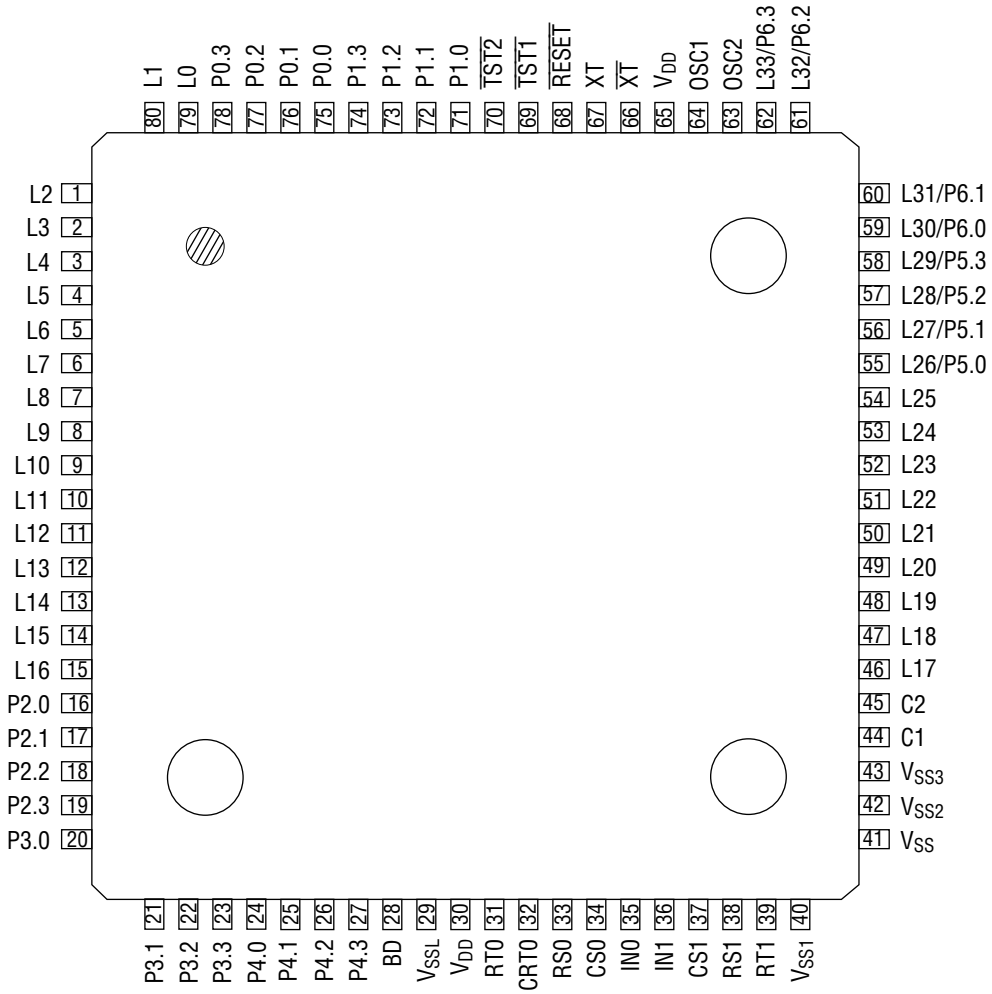
## PIN CONFIGURATION (TOP VIEW) (Continued)




**(QFP80-1414-0.65-K)**

**80-Pin Plastic QFP**

## PIN CONFIGURATION (TOP VIEW) (Continued)




**(TQFP80-1212-0.50-K)**

**80-Pin Plastic TQFP**

## PIN DESCRIPTION

### Basic Function

| Function | Symbol | Type | Description | |
|---|---|---|---|---|
| Power Supply | $V_{DD}$ | — | 0V power supply | |
| | $V_{SS1}$ | — | Negative power supply at 1.5 V spec. Bias output for driving LCD (–1.5 V) | |
| | $V_{SS2}$ | — | Negative power supply at 3.0 V spec. Bias output for driving LCD (–3.0 V) | |
| | $V_{SS3}$ | — | Bias output for driving LCD (–4.5 V). | |
| | $V_{SS}$ | — | Negative power supply for I/O port interface | |
| | $V_{SSL}$ | — | Negative power supply pin for internal logic (internally generated constant voltage) | |
| | C1, C2 | — | Capacitor connection pins for generating $V_{SS1}$, $V_{SS2}$, and $V_{SS3}$. | |
| Oscillation | XT | I | Low speed side clock oscillation input pins : Connects to the crystal resonator (32.768kHz) | |
| | $\overline{XT}$ | O | | |
| | OSC1 | I | High speed side clock pins (400 kHz) : Connects to the external resistor of oscillation ($R_{OS}$) | |
| | OSC2 | O | | |
| Port | P1.0 to P1.3 | O | Output port (P1.0 : Large current drive output port) | |
| | P0.0 to P0.3 | I | Input port | |
| | P2.0 to P4.3 | I/O | Input-output ports | |
| | BD | O | Output pin for the buzzer driver | |
| | L0 to L25 | O | LCD driver pins | |
| | L26/P5.0 to L33/P6.3 | O | LCD driver pins, output ports by mask option | |
| A/D Converter | RT0 | O | Resistance sensor connection pin for measurement | RC oscillation pins for A/D converter (channel 0) (CROSC0) |
| | CRT0 | O | Resistance /capacitance sensor connection pin for measurement | |
| | RS0 | O | Reference resistor connection pin | |
| | CS0 | O | Reference capacitor connection pin | |
| | IN0 | I | Oscillation input pin | |
| | RT1 | O | Resistance sensor connection pin for measurement | RC oscillation pins for A/D converter (channel 1) (CROSC1) |
| | RS1 | O | Reference resistor connection pin | |
| | CS1 | O | Reference capacitor connection pin | |
| | IN1 | I | Oscillation input pin | |
| Reset | $\overline{RESET}$ | I | Reset pin | |
| Test | $\overline{TST1}$ | I | Test pins | |
| | $\overline{TST2}$ | I | | |

## Secondary Function

| Function | Symbol | Type | Description |
|---|---|---|---|
| Serial Port | P3.3 | I | Secondary function of P3.3:<br>This pin is allocated to the data input of a serial port (SIN). |
| | P4.0 | O | Secondary function of P4.0:<br>This pin is allocated to the data output of a serial port (SOUT). |
| | P4.1 | O | Secondary function of P4.1:<br>This pin is allocated to the ready output of a serial port (SPR). |
| | P4.2 | I/O | Secondary function of P4.2:<br>This pin is allocated to the clock input and output of a serial port (SCLK). |
| RC Oscillation Monitor | P4.3 | O | Secondary function of P4.3:<br>This pin is a monitor output (MON) of an RC oscillation clock (OSCCLK) for an A/D converter and a 400 kHz RC oscillation clock for a system clock. |

## INSTRUCTION LIST

| | Mnemonic | Operand | B | C | Description |
|---|---|---|---|---|---|
| Transfer Instructions | LAI | $n_4$ | 1 | 1 | A←$n_4$ (vertical product instruction) |
| | LLI | $n_4$ | 1 | 1 | L←$n_4$ (vertical product instruction) |
| | LHI | $n_4$ | 2 | 2 | H←$n_4$ |
| | LYI | $n_4$ | 2 | 2 | Y←$n_4$ |
| | LXI | $n_4$ | 2 | 2 | X←$n_4$ |
| | LBS0I | $n_3$ | 2 | 2 | BSR0←$n_3$ |
| | LBS1I | $n_3$ | 2 | 2 | BSR1←$n_3$ |
| | LMI | $n_4$ | 2 | 2 | M(HL)←$n_4$ |
| | LAB | — | 2 | 2 | A←B |
| | LAL | — | 1 | 1 | A←L |
| | LAH | — | 1 | 1 | A←H |
| | LAY | — | 1 | 1 | A←Y |
| | LAX | — | 1 | 1 | A←X |
| | LAM | — | 1 | 1 | A←M(HL) |
| | LAM | @XY | 2 | 2 | A←M(XY) |
| | LAMD | $m_8$ | 2 | 2 | A←M($m_8$) |
| | LAM+ | — | 1 | 2 | A←M(HL), L←L+1, Skip if L=0 |
| | LAM– | — | 1 | 2 | A←M(HL), L←L–1, Skip if L=$0F_H$ |
| | LAMM | $n_2$ | 1 | 1 | A←M(HL), H←H∀$n_2$ |
| | LBA | — | 2 | 2 | B←A |
| | LLA | — | 1 | 1 | L←A |
| | LHA | — | 1 | 1 | H←A |
| | LYA | — | 1 | 1 | Y←A |
| | LXA | — | 1 | 1 | X←A |
| | LMA | — | 1 | 1 | M(HL)←A |
| | LMA | @XY | 2 | 2 | M(XY)←A |
| | LMAD | $m_8$ | 2 | 2 | M($m_8$)←A |
| | LMA+ | — | 1 | 2 | M(HL)←A, L←L+1, Skip if L=0 |
| | LMA– | — | 1 | 2 | M(HL)←A, L←L–1, Skip if L=$0F_H$ |

Notes: "B" refers to the byte length of an instruction.
"C" refers to the number of execution machine cycles of an instruction.

## INSTRUCTION LIST (Continued)

| | Mnemonic | Operand | B | C | Description |
|---|---|---|---|---|---|
| Byte Transfer Instructions | LBAI | $n_8$ | 2 | 2 | BA←$n_8$ |
| | LHLI | $n_8$ | 2 | 2 | HL←$n_8$ |
| | LXYI | $n_8$ | 2 | 2 | XY←$n_8$ |
| | LMBI | $n_8$ | 2 | 2 | $M_b$(HL)←$n_8$ |
| | LMBI | @XY, $n_8$ | 3 | 3 | $M_b$(XY)←$n_8$ |
| | LALB | — | 2 | 2 | BA←HL |
| | LAYB | — | 2 | 2 | BA←XY |
| | LLAB | — | 2 | 2 | HL←BA |
| | LYAB | — | 2 | 2 | XY←BA |
| | LAMB | — | 1 | 2 | BA←$M_b$(HL) |
| | LAMB | @XY | 2 | 3 | BA←$M_b$(XY) |
| | LAMDB | $m_8$ | 2 | 2 | BA←$M_b$($m_8$) |
| | LMAB | — | 1 | 2 | $M_b$(HL)←BA |
| | LMAB | @XY | 2 | 3 | $M_b$(XY)←BA |
| | LMADB | $m_8$ | 2 | 2 | $M_b$($m_8$)←BA |
| | LMTB | $a_4$ | 2 | 3 | $M_b$(HL)←T($a_4$, XY) |
| Exchange Instructions | XAB | — | 1 | 2 | A↔B |
| | XAM | — | 1 | 1 | A↔M(HL) |
| | XAM | @XY | 2 | 2 | A↔M(XY) |
| | XAMD | $m_8$ | 2 | 2 | A↔M($m_8$) |
| | XAM+ | — | 1 | 2 | A↔M(HL), L←L+1, Skip if L=0 |
| | XAM– | — | 1 | 2 | A↔M(HL), L←L–1, Skip if L=0$F_H$ |
| | XAMM | $n_2$ | 1 | 1 | A↔M(HL), H←H∀$n_2$ |
| | XAMB | — | 1 | 2 | BA↔$M_b$(HL) |
| | XAMB | @XY | 2 | 3 | BA↔$M_b$(XY) |
| | XAMDB | $m_8$ | 2 | 2 | BA↔$M_b$($m_8$) |
| Operation Instructions | AIS | $n_4$ | 1 | 1 | A←A+$n_4$, Skip if carry=1 |
| | ADC | — | 1 | 1 | A, C←A+M(HL)+C |
| | ADC | @XY | 2 | 2 | A, C←A+M(XY)+C |
| | ADS | — | 1 | 1 | A←A+M(HL), Skip if carry=1 |
| | ADS | @XY | 2 | 2 | A←A+M(XY), Skip if carry=1 |

Note: "carry" refers to a carry of the operation result.

## INSTRUCTION LIST (Continued)

| | Mnemonic | Operand | B | C | Description |
|---|---|---|---|---|---|
| Operation Instructions | ADCS | — | 1 | 1 | A,C←A+M(HL)+C, Skip if carry=1 |
| | ADCS | @XY | 2 | 2 | A,C←A+M(XY)+C, Skip if carry=1 |
| | SUBC | — | 1 | 1 | A,C←A–M(HL)–C |
| | SUBC | @XY | 2 | 2 | A,C←A–M(XY)–C |
| | SUBS | — | 1 | 1 | A←A–M(HL), Skip if borrow=1 |
| | SUBS | @XY | 2 | 2 | A←A–M(XY), Skip if borrow=1 |
| | SUBCS | — | 1 | 1 | A,C←A–M(HL)–C, Skip if borrow=0 |
| | SUBCS | @XY | 2 | 2 | A,C←A–M(XY)–C, Skip if borrow=0 |
| | ANDI | $n_4$ | 2 | 2 | A←A∨$n_4$ |
| | AND | — | 1 | 1 | A←A∧M(HL) |
| | AND | @XY | 2 | 2 | A←A∧M(XY) |
| | ORI | $n_4$ | 2 | 2 | A←A∨$n_4$ |
| | OR | — | 1 | 1 | A←A∨M(HL) |
| | OR | @XY | 2 | 2 | A←A∨M(XY) |
| | EORI | $n_4$ | 2 | 2 | A←A∀$n_4$ |
| | EOR | — | 1 | 1 | A←A∀M(HL) |
| | EOR | @XY | 2 | 2 | A←A∀M(HL) |
| | CMA | — | 2 | 2 | A←$\overline{A}$ |
| | RAL | — | 1 | 1 | C←$A_3$←$A_2$←$A_1$←$A_0$←C |
| | RAR | — | 1 | 1 | C→$A_3$→$A_2$→$A_1$→$A_0$→C |
| Byte Operation Instructions | ADCB | — | 1 | 2 | BA, C←BA+ $M_b$(HL)+C |
| | ADCB | @XY | 2 | 3 | BA, C←BA+ $M_b$(XY)+C |
| | ADSB | — | 1 | 2 | BA←BA+ $M_b$(HL), Skip if carry=1 |
| | ADSB | @XY | 2 | 3 | BA←BA+ $M_b$(XY), Skip if carry=1 |
| | SUBCB | — | 1 | 2 | BA, C←BA– $M_b$(HL)–C |
| | SUBCB | @XY | 2 | 3 | BA, C←BA– $M_b$(XY)–C |
| | SUBSB | — | 1 | 2 | BA←BA– $M_b$(HL), Skip if borrow=1 |
| | SUBSB | @XY | 2 | 3 | BA←BA– $M_b$(XY), Skip if borrow=1 |

Notes: "Carry" refers to a carry of the operation result.
"Borrow" refers to a borrow of the operation result.

## INSTRUCTION LIST (Continued)

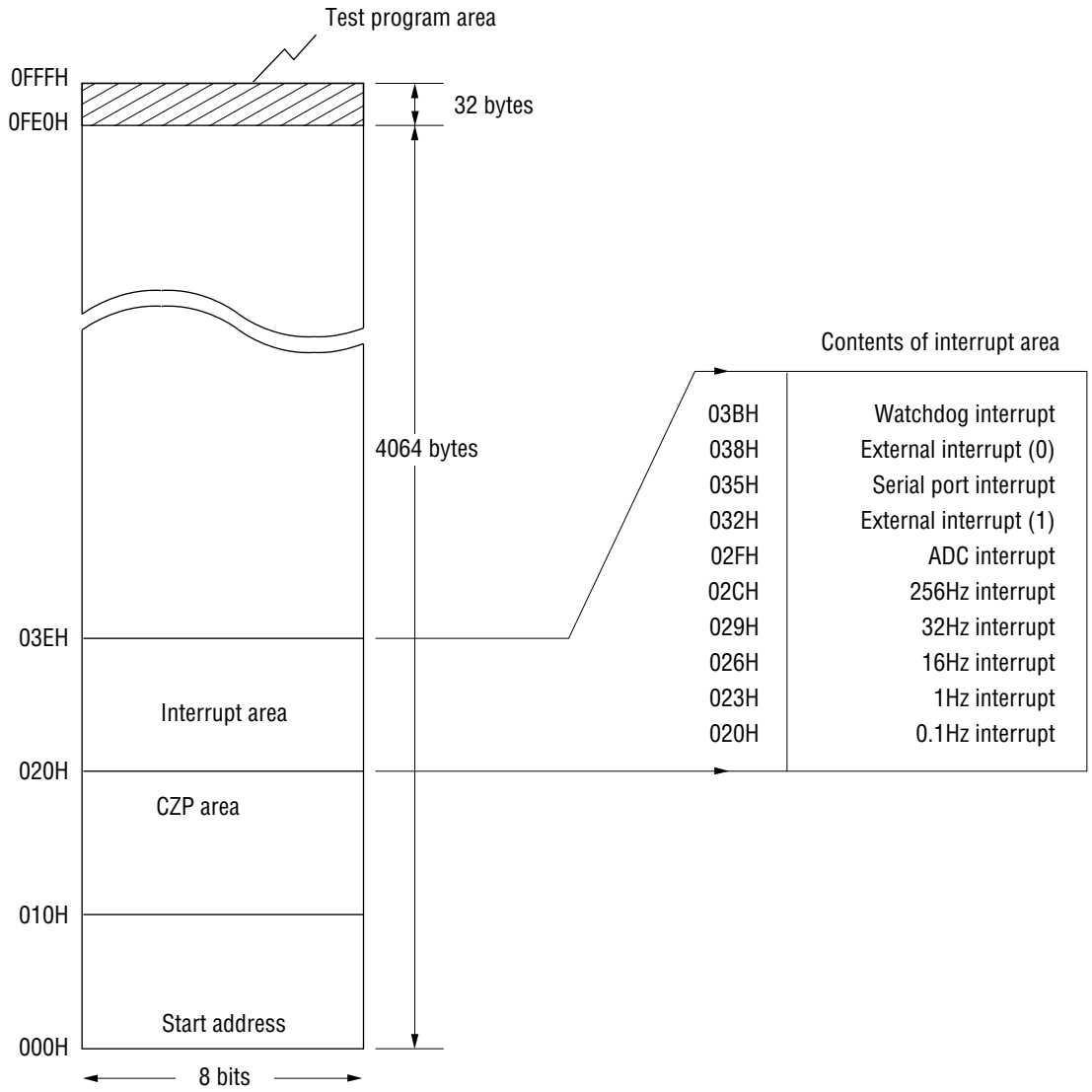
| | Mnemonic | Operand | B | C | Description |
|---|---|---|---|---|---|
| Bit Operation Instructions | SC | — | 1 | 1 | C←1 |
| | RC | — | 1 | 1 | C←0 |
| | TC | — | 1 | 1 | Skip if C=0 |
| | SBE | — | 1 | 1 | BEF←1 |
| | RBE | — | 1 | 1 | BEF←0 |
| | SBC | — | 1 | 1 | BCF←1 |
| | RBC | — | 1 | 1 | BCF←0 |
| | SMB | $n_2$ | 1 | 1 | M(HL)[$n_2$]←1 |
| | SMB | @XY, $n_2$ | 2 | 2 | M(XY)[$n_2$]←1 |
| | SMBD | $m_8$, $n_2$ | 2 | 2 | M($m_8$)[$n_2$]←1 |
| | RMB | $n_2$ | 1 | 1 | M(HL)[$n_2$]←0 |
| | RMB | @XY, $n_2$ | 2 | 2 | M(XY)[$n_2$]←0 |
| | RMBD | $m_8$, $n_2$ | 2 | 2 | M($m_8$)[$n_2$]←0 |
| | TAB | $n_2$ | 1 | 1 | Skip if A[$n_2$]=1 |
| | TMB | $n_2$ | 1 | 1 | Skip if M(HL)[$n_2$]=1 |
| | TMB | @XY, $n_2$ | 2 | 2 | Skip if M(XY)[$n_2$]=1 |
| | TMBD | $m_8$, $n_2$ | 2 | 2 | Skip if M($m_8$)[$n_2$]=1 |
| Increment/ decrement Instructions | INA | — | 1 | 1 | A←A+1, Skip if A=0 |
| | INL | — | 1 | 1 | L←L+1, Skip if L=0 |
| | INH | — | 1 | 1 | H←H+1, Skip if H=0 |
| | INY | — | 1 | 1 | Y←Y+1, Skip if Y=0 |
| | INX | — | 1 | 1 | X←X+1, Skip if X=0 |
| | INM | — | 1 | 1 | M(HL)←M(HL)+1, Skip if M(HL)=0 |
| | INM | @XY | 2 | 2 | M(XY)←M(XY)+1, Skip if M(XY)=0 |
| | INMD | $m_8$ | 2 | 2 | M($m_8$)←M($m_8$)+1, Skip if M($m_8$)=0 |
| | DCA | — | 1 | 1 | A←A–1, Skip if A=$0F_H$ |
| | DCL | — | 1 | 1 | L←L–1, Skip if L=$0F_H$ |
| | DCH | — | 1 | 1 | H←H–1, Skip if H=$0F_H$ |
| | DCY | — | 1 | 1 | Y←Y–1, Skip if Y=$0F_H$ |
| | DCX | — | 1 | 1 | X←X–1, Skip if X=$0F_H$ |
| | DCM | — | 1 | 1 | M(HL)←M(HL)–1, Skip if M(HL)=$0F_H$ |
| | DCM | @XY | 2 | 2 | M(XY)←M(XY)–1, Skip if M(XY)=$0F_H$ |
| | DCMD | $m_8$ | 2 | 2 | M($m_8$)←M($m_8$)–1, Skip if M($m_8$)=$0F_H$ |

## INSTRUCTION LIST (Continued)

| | Mnemonic | Operand | B | C | Description |
|---|---|---|---|---|---|
| Comparison Instructions | CAI | $n_4$ | 2 | 2 | Skip if A=$n_4$ |
| | CLI | $n_4$ | 2 | 2 | Skip if L=$n_4$ |
| | CMI | $n_4$ | 2 | 2 | Skip if M(HL)=$n_4$ |
| | CAB | — | 1 | 1 | Skip if A=B |
| | CAM | — | 1 | 1 | Skip if A=M(HL) |
| | CAM | @XY | 2 | 2 | Skip if A=M(XY) |
| | CAMD | $m_8$ | 2 | 2 | Skip if A=M($m_8$) |
| | CAMB | — | 1 | 2 | Skip if BA=$M_b$(HL) |
| | CAMB | @XY | 2 | 3 | Skip if BA=$M_b$(XY) |
| Stack Instructions | PUSH | BA | 1 | 2 | ST←BA, SP←SP–1 |
| | PUSH | HL | 1 | 2 | ST←HL, SP←SP–1 |
| | PUSH | BSR | 1 | 2 | ST←BSR, SP←SP–1 |
| | POP | BA | 1 | 2 | SP←SP+1, BA←ST |
| | POP | HL | 1 | 2 | SP←SP+1, HL←ST |
| | POP | BSR | 1 | 2 | SP←SP+1, BSR←ST |
| Branch Instructions | JCP | $a_6$ | 1 | 1 | $PC_{5-0}$←$a_6$ |
| | JP | $a_{11}$ | 2 | 2 | $PC_{10-0}$←$a_{11}$ |
| | LJP | $a_{12}$ | 3 | 5 | $PC_{11-0}$←$a_{12}$ |
| | JA | — | 1 | 1 | $PC_{5-0}$←BA(lower 6 bits) |
| | JM | — | 1 | 3 | $PC_{11-0}$←[$M_b$(HL), BA] |
| Subroutine Instructions | CZP | $a_5$ | 1 | 4 | ST←PC+1, $PC_{4-0}$←$a_5$, $PC_{11-5}$←0<br>SP←SP–2($a_5$ is an even number of $10_H$ to $1E_H$) |
| | CAL | $a_{11}$ | 2 | 4 | ST←PC+2, $PC_{10-0}$←$a_{11}$, SP←SP–2 |
| | LCAL | $a_{12}$ | 3 | 5 | ST←PC+3, $PC_{11-0}$←$a_{12}$, SP←SP–2 |
| | RT | — | 1 | 3 | $PC_{11-0}$←ST, SP←SP+2 |
| | RTS | — | 1 | 3 | $PC_{11-0}$←ST, SP←SP+2, Then skip |
| | RTI | — | 1 | 5 | $PC_{11-0}$←•C•HL•BA←ST, SP+4, MI←1 |
| | NOP | — | 1 | 1 | No operation |

## MEMORY MAPS

### Program Memory

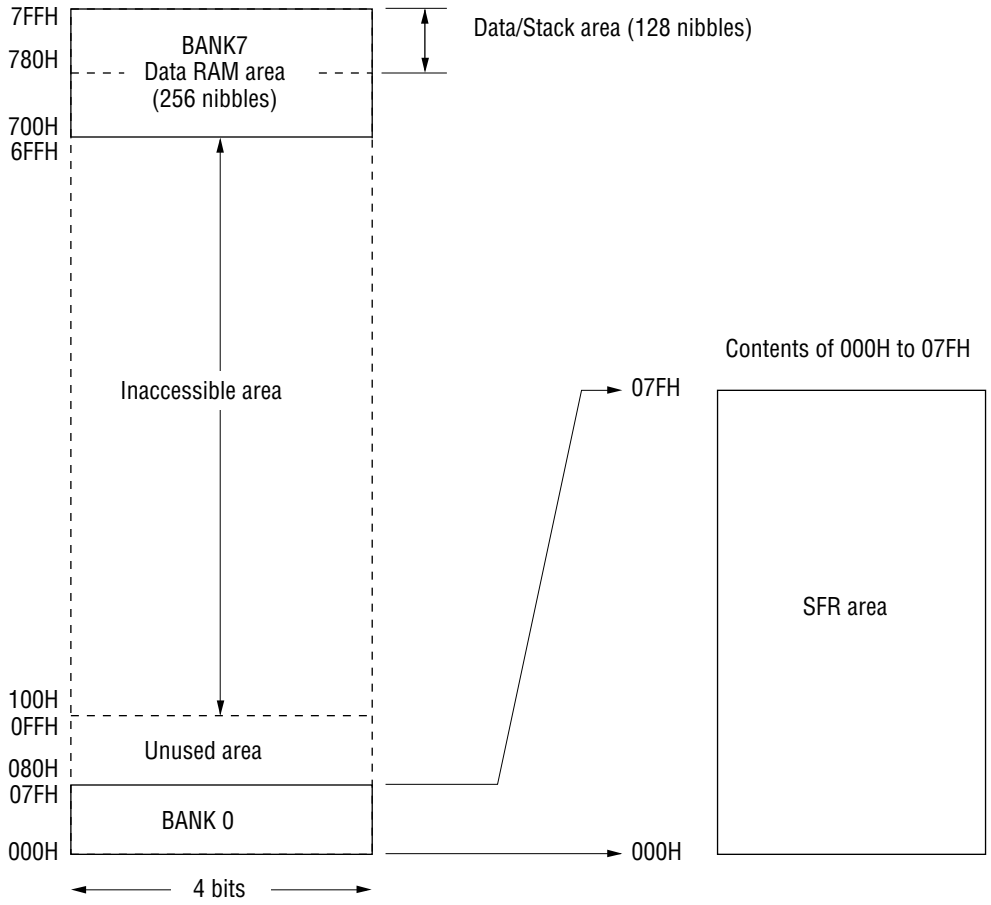



**Program Memory Map**

Address 000H is the instruction execution start address by the system reset.
The CZP area from address 010H to address 01FH is the start address for the CZP subroutine of one-byte call instruction.
The start address of interrupt subroutine is assigned to the interrupt address from address 020H to 03DH.
The user area has 4064 bytes of address 000H to address 0FDF. No program can be stored in the test program area.

### Data Memory

The data memory area consists of 8 banks and each bank has 256 nibbles (256 × 4 bits).
The data RAM is assigned to BANK 7 and peripheral ports are assigned to BANK 0.




**Data Memory Map**

Half the data RAM area (128 nibbles) also serves as stack area. The stack is a memory starting from address 7FFH toward the low-order addresses where 4 nibbles are used by Subroutine Call Instruction and 8 nibbles are used by an interrupt.
The addresses 080H to 0FFH of BANK 0 and the addresses 700H to 77FH of BANK 7 are not assigned as the data memory, so access to these addresses has no effect. Moreover, it is impossible to access BANK 1 to BANK 6.

## ABSOLUTE MAXIMUM RATINGS (1.5 V Spec)

($V_{DD}$=0 V)

| Parameter | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Power Supply Voltage 1 | $V_{SS1}$ | Ta=25°C | –2.0 to +0.3 | V |
| Power Supply Voltage 2 | $V_{SS2}$ | Ta=25°C | –4.0 to +0.3 | V |
| Power Supply Voltage 3 | $V_{SS3}$ | Ta=25°C | –5.5 to +0.3 | V |
| Power Supply Voltage 4 | $V_{SSL}$ | Ta=25°C | –2.0 to +0.3 | V |
| Power Supply Voltage 5 | $V_{SS}$ | Ta=25°C | –5.5 to +0.3 | V |
| Input Voltage 1 | $V_{IN1}$ | $V_{SS1}$ Input, Ta=25°C | $V_{SS1}$ –0.3 to +0.3 | V |
| Input Voltage 2 | $V_{IN2}$ | $V_{SS}$ Input, Ta=25°C | $V_{SS}$ –0.3 to +0.3 | V |
| Input Voltage 3 | $V_{IN3}$ | $V_{SSL}$ Input, Ta=25°C | $V_{SSL}$ –0.3 to +0.3 | V |
| Output Voltage 1 | $V_{OUT1}$ | $V_{SS1}$ Output, Ta=25°C | $V_{SS1}$ –0.3 to +0.3 | V |
| Output Voltage 2 | $V_{OUT2}$ | $V_{SS2}$ Output, Ta=25°C | $V_{SS2}$ –0.3 to +0.3 | V |
| Output Voltage 3 | $V_{OUT3}$ | $V_{SS3}$ Output, Ta=25°C | $V_{SS3}$ –0.3 to +0.3 | V |
| Output Voltage 4 | $V_{OUT4}$ | $V_{SS}$ Output, Ta=25°C | $V_{SS}$ –0.3 to +0.3 | V |
| Output Voltage 5 | $V_{OUT5}$ | $V_{SSL}$ Output, Ta=25°C | $V_{SSL}$ –0.3 to +0.3 | V |
| Storage Temperature | $T_{STG}$ | — | –55 to +125 | °C |

## RECOMMENDED OPERATING CONDITIONS (1.5 V Spec)

($V_{DD}$=0 V)

| Parameter | Symbol | Condition | Range | Unit |
|---|---|---|---|---|
| Operating Temperature | $T_{op}$ | — | –40 to +85 | °C |
| Operating Voltage | $V_{SS1}$ | — | –1.7 to –1.25 | V |
| | $V_{SS}$ | — | –5.25 to $V_{SS1}$ | V |
| 400 kHz OSC External Resistance | $R_{OS}$ | — | 250 to 500 | kΩ |
| X'tal Oscillator Frequency | $f_{XT}$ | — | 30 to 35 | kHz |

## ELECTRICAL CHARACTERISTICS (1.5 V Spec)

### DC Characteristics

($V_{DD}$=0 V, $V_{SS1}$=$V_{SS}$=–1.5 V, Ta=–40 to +85°C unless otherwise specified)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit | Measuring Circuit |
|---|---|---|---|---|---|---|---|
| $V_{SS2}$ Voltage | $V_{SS2}$ | Ca, Cb, C12=0.1 µF +100% –50% | –3.2 | –3.0 | –2.8 | V | 1 |
| $V_{SS3}$ Voltage | $V_{SS3}$ | Ca, Cb, C12=0.1 µF +100% –50% | –4.7 | –4.5 | –4.3 | V | |
| $V_{SSL}$ Voltage | $V_{SSL}$ | — | –1.5 | –1.3 | –0.6 | V | |
| XTOSC Oscillation Start Voltage | $V_{STA}$ | Within 5 seconds after oscillation starts | — | — | –1.45 | V | |
| XTOSC Oscillation Hold Voltage | $V_{HOLD}$ | — | — | — | –1.25 | V | |
| XTOSC Stop Detection Time | $T_{STOP}$ | — | 0.1 | — | 1000 | ms | |
| XTOSC Internal Capacitance | $C_G$ | — | 10 | 15 | 20 | pF | |
| XTOSC External Capacitance | $C_{GEX}$ | External $C_G$ option | 10 | — | 30 | pF | |
| XTOSC Internal Capacitance | $C_D$ | — | 10 | 15 | 20 | pF | |
| 400kOSC Internal Capacitance | $C_{OS}$ | — | 8 | 12 | 16 | pF | |
| 400kOSC Oscillation Frequency | $f_{OSC}$ | External resistor $R_{OS}$=300 kΩ $V_{SS1}$ =–1.25 to –1.7 V | 80 | 220 | 350 | kHz | |
| POR Generation Voltage | $V_{POR1}$ | When $V_{SS1}$ is between $V_{POR1}$ and –1.5 V | –0.4 | — | 0 | V | |
| POR Non-generation Voltage | $V_{POR2}$ | No POR when $V_{SS1}$ is between $V_{POR2}$ and –1.5 V | –1.5 | — | –1.2 | V | |

Notes: 1. "XTOSC" refers to the 32.768 kHz crystal oscillation circuit.
2. "400kOSC" refers to the 400 kHz RC oscillation circuit.
3. "POR" refers to Power-On Reset.
4. "$T_{STOP}$" indicates that a system reset occurs if XTOSC stops oscillation for more than this duration.

## DC Characteristics (Continued)

($V_{DD}$=0 V, $V_{SS1}$=$V_{SS}$=–1.5 V, Ta=–40 to +85°C unless otherwise specified)

| Parameter | Symbol | Condition | | Min. | Typ. | Max. | Unit | Measuring Circuit |
|---|---|---|---|---|---|---|---|---|
| Power Comsumption 1 | $I_{DD1}$ | CPU in halt state (400k OSC halt) | Ta=–40 to +40°C | — | 2 | 5 | µA | 1 |
| | | | Ta=+40 to +85°C | — | 2 | 30 | µA | |
| Power Comsumption 2 | $I_{DD2}$ | CPU in operation state (400k OSC halt) | Ta=–40 to +40°C | — | 5 | 15 | µA | |
| | | | Ta=+40 to +85°C | — | 5 | 40 | µA | |
| Power Comsumption 3 | $I_{DD3}$ | CPU in operation state (400k OSC in operation) $R_{OS}$=300kΩ | | — | 40 | 80 | µA | |
| Power Comsumption 4 | $I_{DD4}$ | Serial transfer, $f_{SCK}$=300 kHz, CPU in operation state (400k OSC halt) | Ta=–40 to +40°C | — | 7 | 25 | µA | |
| | | | Ta=+40 to +85°C | — | 7 | 50 | µA | |
| Power Comsumption 5 | $I_{DD5}$ | CPU in halt state (400k OSC halt), A/D converter in oscillation state | RT0=10 kΩ | — | 150 | 230 | µA | |
| | | | RT0=2 kΩ | — | 600 | 900 | µA | |

## DC Characteristics (Continued)

($V_{DD}$=0 V, $V_{SS1}$=$V_{SSL}$=$V_{SS}$=–1.5 V, $V_{SS2}$=–3.0 V, $V_{SS3}$=–4.5 V, Ta=–40 to +85°C unless otherwise specified)

| Parameter (Pin Name) | Symbol | Condition | Min. | Typ. | Max. | Unit | Measuring Circuit |
|---|---|---|---|---|---|---|---|
| Output Current 1 (P1.0) | $I_{OH1}$ | $V_{OH1}$=–0.5 V | –2.1 | –0.7 | –0.2 | mA | 2 |
| | $I_{OL1}$ | $V_{OL1}$=$V_{SS1}$+0.5 V | 1 | 3 | 9 | mA | |
| | $I_{OH1S}$ | $V_{SS}$=–5 V, $V_{OH1S}$=–0.5 V | –36 | –12 | –4 | mA | |
| | $I_{OL1S}$ | $V_{SS}$=–5 V, $V_{OL1}$=$V_{SS}$+0.5 V | 4 | 12 | 36 | mA | |
| Output Current 2 (P1.1 to P1.3) (P2.0 to P2.3) (P3.0 to P3.3) (P4.0 to P4.3) | $I_{OH2}$ | $V_{OH2}$=–0.5 V | –2.1 | –0.7 | –0.2 | mA | |
| | $I_{OL2}$ | $V_{OL2}$=$V_{SS}$+0.5 V | 0.2 | 0.7 | 2.1 | mA | |
| | $I_{OH2S}$ | $V_{SS}$=–5 V, $V_{OH2S}$=–0.5 V | –9 | –3 | –1 | mA | |
| | $I_{OL2S}$ | $V_{SS}$=–5 V, $V_{OL2}$=$V_{SS}$+0.5 V | 1 | 3 | 9 | mA | |
| Output Current 3 (BD) | $I_{OH3}$ | $V_{OH3}$=–0.7 V | –1.8 | –0.6 | –0.2 | mA | |
| | $I_{OL3}$ | $V_{OL3}$=$V_{SS1}$+0.7 V | 0.2 | 0.6 | 1.8 | mA | |
| Output Current 4 (RT0, RT1, RS0, RS1, CRT0, CS0, CS1) | $I_{OH4}$ | $V_{OH4}$=–0.1 V | –1.1 | –0.6 | –0.3 | mA | |
| | $I_{OL4}$ | $V_{OL4}$=$V_{SS1}$+0.1 V | 0.3 | 0.6 | 1.1 | mA | |
| Output Current 5 (When L26 to L33 are configured as output ports) | $I_{OH5}$ | $V_{OH5}$=–0.5 V | –1.5 | –0.5 | –0.1 | mA | |
| | $I_{OL5}$ | $V_{OL5}$=$V_{SS1}$+0.5 V | 0.1 | 0.5 | 1.5 | mA | |
| | $I_{OH5S}$ | $V_{SS}$=–5V, $V_{OH5S}$=–0.5 V | –2.0 | –0.7 | –0.2 | mA | |
| | $I_{OL5S}$ | $V_{SS}$=–5 V, $V_{OL5S}$=$V_{SS}$+0.5 V | 0.2 | 0.7 | 2.0 | mA | |
| Output Current 6 (OSC2) | $I_{OH6}$ | $V_{OH6}$=–0.5 V | –2.1 | –0.7 | –0.2 | mA | |
| | $I_{OL6}$ | $V_{OL6}$=$V_{SS1}$+0.5 V | 0.2 | 0.7 | 2.1 | mA | |
| Output Current 7 (L0 to L33) | $I_{OH7}$ | $V_{OH7}$=–0.2 V ($V_{DD}$ level) | — | — | –4 | µA | |
| | $I_{OMH7}$ | $V_{OMH7}$=$V_{SS1}$+0.2 V ($V_{SS1}$ level) | 4 | — | — | µA | |
| | $I_{OMH7S}$ | $V_{OMH7S}$=$V_{SS1}$–0.2 V ($V_{SS1}$ level) | — | — | –4 | µA | |
| | $I_{OML7}$ | $V_{OML7}$=$V_{SS2}$+0.2 V ($V_{SS2}$ level) | 4 | — | — | µA | |
| | $I_{OML7S}$ | $V_{OML7S}$=$V_{SS2}$–0.2 V ($V_{SS2}$ level) | — | — | –4 | µA | |
| | $I_{OL7}$ | $V_{OL7}$=$V_{SS3}$+0.2 V ($V_{SS3}$ level) | 4 | — | — | µA | |
| Output Leakage Current (P1.0 to P1.3) (P2.0 to P2.3) (P3.0 to P3.3) (P4.0 to P4.3) (RT0, RT1, RS0, RS1, CRT0, CS0, CS1) | $I_{OOH}$ | $V_{OH}$=$V_{DD}$ | — | — | 0.3 | µA | |
| | $I_{OOL}$ | $V_{OL}$=$V_{SS1}$ | –0.3 | — | — | µA | |

## DC Characteristics (Continued)

($V_{DD}$=0 V, $V_{SS1}$=$V_{SSL}$=$V_{SS}$=–1.5 V, $V_{SS2}$=–3.0 V, $V_{SS3}$=–4.5 V, Ta=–40 to +85°C unless otherwise specified)

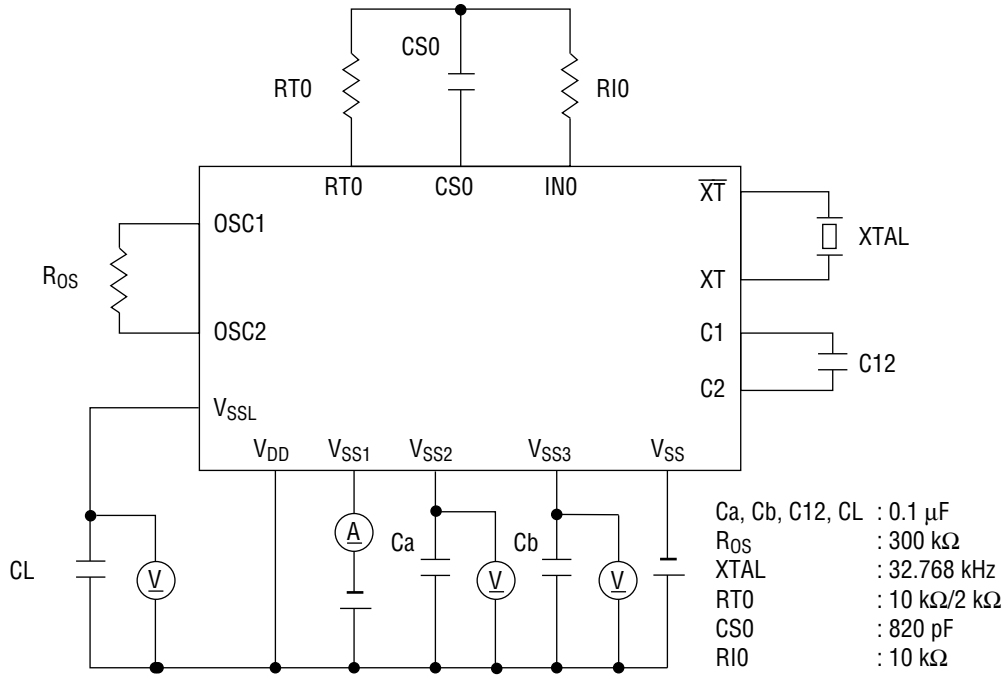
| Parameter (Pin Name) | Symbol | Condition | Min. | Typ. | Max. | Unit | Measuring Circuit |
|---|---|---|---|---|---|---|---|
| Input Current 1 (P0.0 to P0.3) (P2.0 to P2.3) (P3.0 to P3.3) (P4.0 to P4.3) | $I_{IH1}$ | $V_{IH1}$=$V_{DD}$ (pull-down) | 5 | 18 | 60 | µA | 3 |
| | $I_{IL1}$ | $V_{IL1}$=$V_{SS1}$ (pull-up) | –60 | –18 | –5 | µA | |
| | $I_{IH1S}$ | $V_{IH1}$=$V_{DD}$, $V_{SS}$=–5 V (pull-down) | 70 | 250 | 660 | µA | |
| | $I_{IL1S}$ | $V_{IL1}$=$V_{SS}$=–5 V (pull-up) | –660 | –250 | –70 | µA | |
| | $I_{IH1Z}$ | $V_{IH1}$=$V_{DD}$ (high impedance) | 0 | — | 1 | µA | |
| | $I_{IL1Z}$ | $V_{IL1}$=$V_{SS}$(high impedance) | –1 | — | 0 | µA | |
| Input Current 2 (IN0, IN1) | $I_{IH2}$ | $V_{IH2}$=$V_{DD}$ (pull-down) | 5 | 18 | 60 | µA | |
| | $I_{IH2Z}$ | $V_{IH2}$=$V_{DD}$ (high impedance) | 0 | — | 1 | µA | |
| | $I_{IL2Z}$ | $V_{IL2}$=$V_{SS1}$(high impedance) | –1 | — | 0 | µA | |
| Input Current 3 (OSC1) | $I_{IL3}$ | $V_{IL3}$=$V_{SS1}$ (pull-up) | –60 | –22 | –6 | µA | |
| | $I_{IH3Z}$ | $V_{IH3}$=$V_{DD}$ (high impedance) | 0 | — | 1 | µA | |
| | $I_{IL3Z}$ | $V_{IL3}$=$V_{SS1}$ (high impedance) | –1 | — | 0 | µA | |
| Input Current 4 ($\overline{RESET}$, $\overline{TST1}$, $\overline{TST2}$) | $I_{IH4}$ | $V_{IH4}$=$V_{DD}$ | 0 | — | 1 | µA | |
| | $I_{IL4}$ | $V_{IL4}$=$V_{SS1}$ | –1.5 | –0.75 | –0.3 | mA | |
| Input Voltage 1 (P0.0 to P0.3) (P2.0 to P2.3) (P3.0 to P3.3) (P4.0 to P4.3) | $V_{IH1}$ | — | –0.3 | — | 0 | V | 4 |
| | $V_{IL1}$ | — | –1.5 | — | –1.2 | V | |
| | $V_{IH1S}$ | $V_{SS}$=–5 V | –1 | — | 0 | V | |
| | $V_{IL1S}$ | $V_{SS}$=–5 V | –5 | — | –4 | V | |
| Input Voltage 2 (IN0, IN1, OSC1) | $V_{IH2}$ | — | –0.3 | — | 0 | V | |
| | $V_{IL2}$ | — | –1.5 | — | –1.2 | V | |
| Input Voltage 3 ($\overline{RESET}$, $\overline{TST1}$, $\overline{TST2}$) | $V_{IH3}$ | — | –0.3 | — | 0 | V | |
| | $V_{IL3}$ | — | –1.5 | — | –1.2 | V | |

## DC Characteristics (Continued)

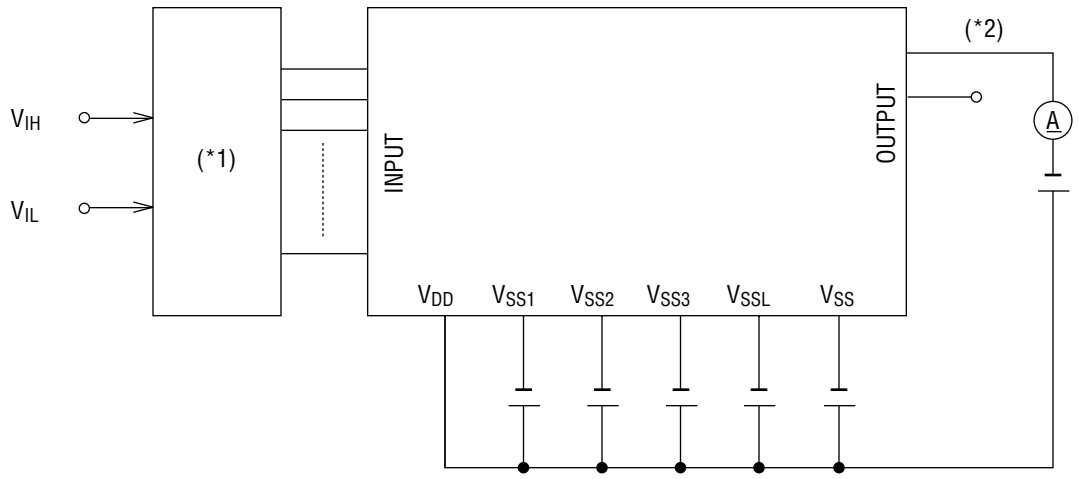
($V_{DD}$=0 V, $V_{SS1}$=$V_{SSL}$=$V_{SS}$=–1.5 V, $V_{SS2}$=–3.0 V, $V_{SS3}$=–4.5 V, Ta=–40 to +85°C unless otherwise specified)

| Parameter (Pin Name) | Symbol | Condition | Min. | Typ. | Max. | Unit | Measuring Circuit |
|---|---|---|---|---|---|---|---|
| Hysteresis Width (P0.0 to P0.3) (P2.0 to P2.3) (P3.0 to P3.3) (P4.0 to P4.3) | $\Delta V_{T1}$ | — | 0.05 | 0.1 | 0.3 | V | 4 |
| | $\Delta V_{T1S}$ | $V_{SS}$=–5 V | 0.25 | 1.0 | 1.5 | V | |
| Hysteresis Width ($\overline{RESET}$, $\overline{TST1}$, $\overline{TST2}$) | $\Delta V_{T2}$ | — | 0.05 | 0.1 | 0.3 | V | |
| Input Pin Capacitance (P0.0 to P0.3) (P2.0 to P2.3) (P3.0 to P3.3) (P4.0 to P4.3) | $C_{IN}$ | — | — | — | 5 | pF | 1 |

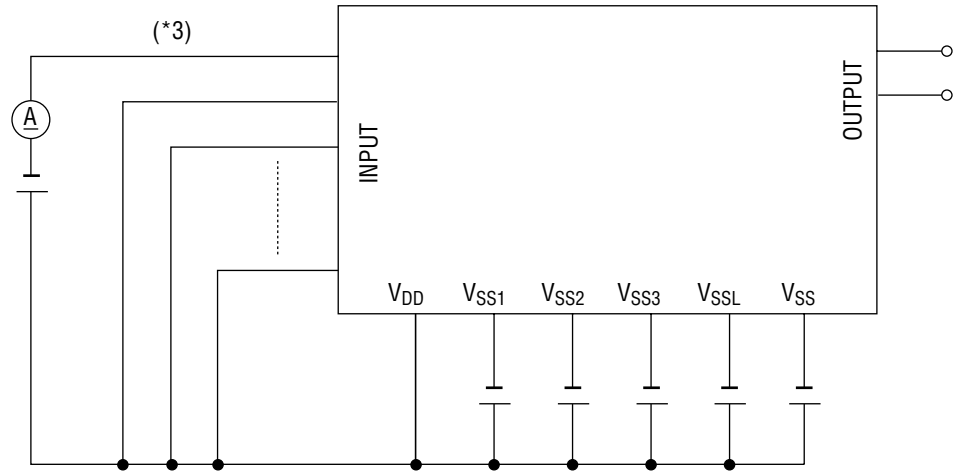
**Measuring Circuit 1**



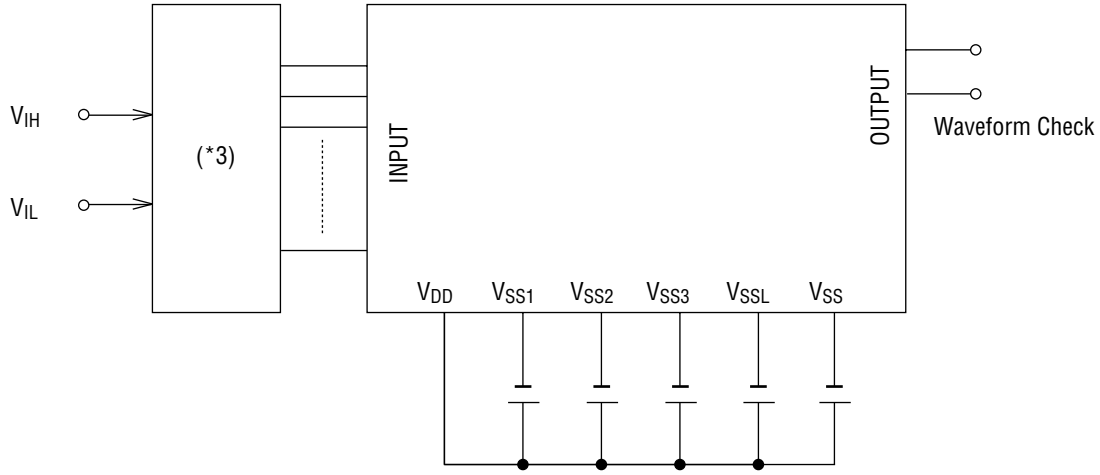

**Measuring Circuit 2**



### Measuring Circuit 3




### Measuring Circuit 4




*1 Input logic to select a specified state.
*2 To be repeated for the specified output pin.
*3 To be repeated for the specified input pin.

### A/D Converter Characteristics

($V_{DD}$=0 V, $V_{SS1}$=$V_{SS}$=–1.5 V, Ta=–40 to +85°C unless otherwise specified)

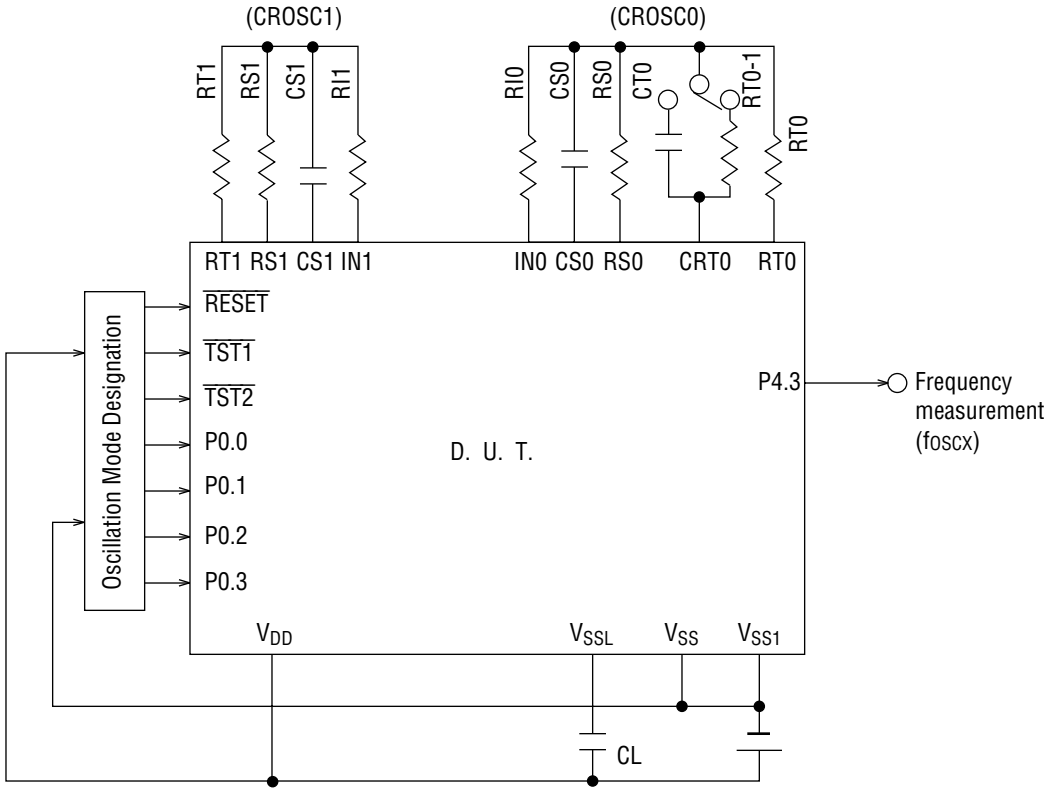
| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit | Measuring Circuit |
|---|---|---|---|---|---|---|---|
| Resistor for Oscillation | RS0, RS1, RT0, RT0-1, RT1 | CS0, CT0, CS1≥740 pF | 2 | — | — | kΩ | 5 |
| Input Current Limiting Resistor | RI0, RI1 | — | 1 | 10 | — | kΩ | |
| Oscillation Frequency | $f_{OSC1}$ | Resistor for oscillation=2 kΩ | 165 | 221 | 256 | kHz | |
| | $f_{OSC2}$ | Resistor for oscillation=10 kΩ | 41.8 | 52.2 | 60.6 | kHz | |
| | $f_{OSC3}$ | Resistor for oscillation=200 kΩ | 2.55 | 3.04 | 3.53 | kHz | |
| RS•RT Oscillation Frequency Ratio (*) | Kf1 | RT0, RT0-1, RT1= 2 kΩ | 3.89 | 4.18 | 4.35 | — | |
| | Kf2 | RT0, RT0-1, RT1=10 kΩ | 0.990 | 1 | 1.010 | — | |
| | Kf3 | RT0, RT0-1, RT1=200 kΩ | 0.0561 | 0.0584 | 0.0637 | — | |

* Kfx is the ratio of the oscillation frequency by a sensor resistor to the oscillation frequency by a reference resistor in the same condition.

$$Kfx = \frac{f_{OSCX}\ (RT0\text{-}CS0\ Oscillation)}{f_{OSCX}\ (RS0\text{-}CS0\ Oscillation)}\ ,\ \frac{f_{OSCX}\ (RT0\text{-}1\text{-}CS0\ Oscillation)}{f_{OSCX}\ (RS0\text{-}CS0\ Oscillation)}\ ,\ \frac{f_{OSCX}\ (RT1\text{-}CS1\ Oscillation)}{f_{OSCX}\ (RS1\text{-}CS1\ Oscillation)}$$

(X=1,2,3)

**Measuring Circuit 5**

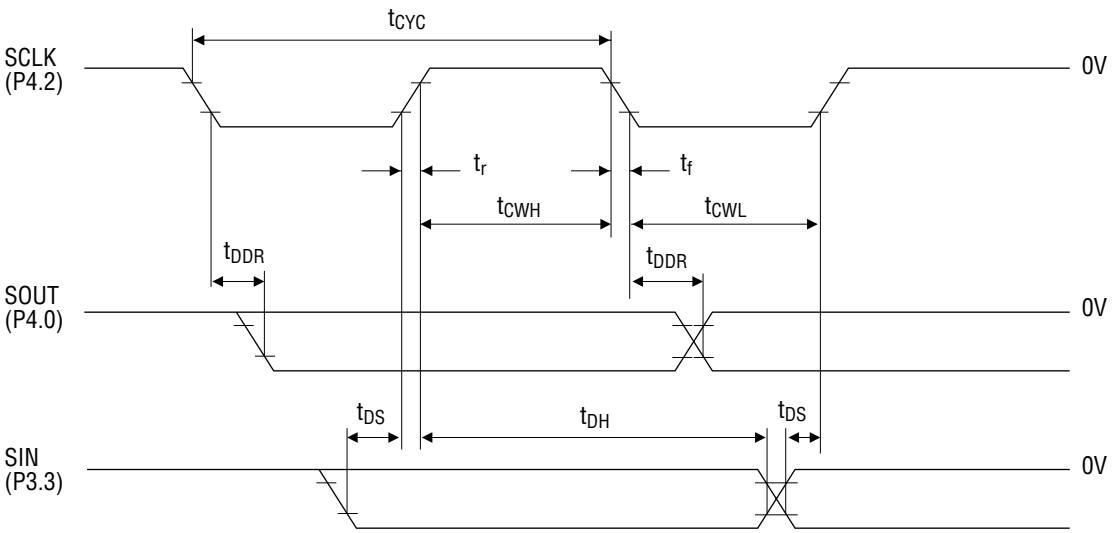



RT0, RT0-1, RT1 = 2 kΩ/10 kΩ/200 kΩ
RS0, RS1 = 10 kΩ
RI0, RI1 = 10 kΩ
CS0, CT0, CS1 = 820 pF
CL = 0.1 μF

### AC Characteristics (Serial Interface)

($V_{DD}$=0 V, $V_{SS1}$=–1.5 V, $V_{SS}$=–5 V, Ta=–40 to +85°C)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| SCLK Input Fall Time | $t_f$ | — | — | — | 1 | µs |
| SCLK Input Rise Time | $t_r$ | — | — | — | 1 | µs |
| SCLK Input "L" Level Pulse Width | $t_{CWL}$ | — | 0.8 | — | — | µs |
| SCLK Input "H" Level Pulse Width | $t_{CWH}$ | — | 0.8 | — | — | µs |
| SCLK Input Cycle Time | $t_{CYC}$ | $V_{SS}$=–5.25 V to $V_{SS1}$ | 2.0 | — | — | µs |
| SCLK Output Cycle Time | $t_{CYC1(○)}$ | CPU is operating at 32 kHz | — | 30.5 | — | µs |
| SCLK Output Cycle Time | $t_{CYC2(○)}$ | CPU is operating at 400 kHz | — | 4.5 | — | µs |
| SOUT Output delay Time | $t_{DDR}$ | CL=10pF | — | — | 0.4 | µs |
| SIN Input Setup Time | $t_{DS}$ | — | 0.5 | — | — | µs |
| SIN Input Hold TIme | $t_{DH}$ | — | 0.8 | — | — | µs |




("H" level=–1 V, "L" level=–4 V)

## ABSOLUTE MAXIMUM RATINGS (3.0 V Spec)

($V_{DD}$=0 V)

| Parameter | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Power Supply Voltage 1 | $V_{SS1}$ | Ta=25°C | –2.0 to +0.3 | V |
| Power Supply Voltage 2 | $V_{SS2}$ | Ta=25°C | –4.0 to +0.3 | V |
| Power Supply Voltage 3 | $V_{SS3}$ | Ta=25°C | –5.5 to +0.3 | V |
| Power Supply Voltage 4 | $V_{SSL}$ | Ta=25°C | –4.0 to +0.3 | V |
| Power Supply Voltage 5 | $V_{SS}$ | Ta=25°C | –5.5 to +0.3 | V |
| Input Voltage 1 | $V_{IN1}$ | $V_{SS2}$ Input, Ta=25°C | $V_{SS2}$ –0.3 to +0.3 | V |
| Input Voltage 2 | $V_{IN2}$ | $V_{SS}$ Input, Ta=25°C | $V_{SS}$ –0.3 to +0.3 | V |
| Input Voltage 3 | $V_{IN3}$ | $V_{SSL}$ Input, Ta=25°C | $V_{SSL}$ –0.3 to +0.3 | V |
| Output Voltage 1 | $V_{OUT1}$ | $V_{SS2}$ Output, Ta=25°C | $V_{SS2}$ –0.3 to +0.3 | V |
| Output Voltage 2 | $V_{OUT2}$ | $V_{SS3}$ Output, Ta=25°C | $V_{SS3}$ –0.3 to +0.3 | V |
| Output Voltage 3 | $V_{OUT3}$ | $V_{SS}$ Output, Ta=25°C | $V_{SS}$ –0.3 to +0.3 | V |
| Output Voltage 4 | $V_{OUT4}$ | $V_{SSL}$ Output, Ta=25°C | $V_{SSL}$ –0.3 to +0.3 | V |
| Storage Temperature | $T_{STG}$ | — | –55 to +125 | °C |

## RECOMMENDED OPERATING CONDITIONS (3.0 V Spec)

($V_{DD}$=0 V)

| Parameter | Symbol | Condition | Range | Unit |
|---|---|---|---|---|
| Operating Temperature | $T_{op}$ | — | –40 to +85 | °C |
| Operating Voltage | $V_{SS2}$ | Using LCD with "duty 1/2" | –3.5 to –2.2 | V |
| | | Except using LCD with "duty 1/2" | –3.5 to –2.0 | |
| | | — | –5.25 to (0.8•$V_{SS2}$, –2.0max.)* | |
| 400 kHz OSC External Resistance | $R_{OS}$ | — | 90 to 500 | kΩ |
| X'tal Oscillator Frequency | $f_{XT}$ | — | 30 to 66 | kHz |

* Indicatates that the value of $V_{SS}$ is 80% of $V_{SS2}$ and should not exceed –2.0 V.

## ELECTRICAL CHARACTERISTICS (3.0 V Spec)

### DC Characteristics

($V_{DD}$=0 V, $V_{SS2}$=$V_{SS}$=–3.0 V, Ta=–40 to +85°C unless otherwise specified)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit | Measuring Circuit |
|---|---|---|---|---|---|---|---|
| $V_{SS1}$ Voltage | $V_{SS1}$ | Ca, Cb, C12=0.1 µF +100% –50% | –1.7 | –1.5 | –1.3 | V | 1 |
| $V_{SS3}$ Voltage | $V_{SS3}$ | Ca, Cb, C12=0.1 µF +100% –50% | –4.7 | –4.5 | –4.3 | V | |
| $V_{SSL}$ Voltage | $V_{SSL}$ | — | –1.9 | –1.3 | –0.6 | V | |
| XTOSC Oscillation Start Voltage | $V_{STA}$ | Within 5 seconds after oscillation starts | — | — | –2.0 | V | |
| XTOSC Oscillation Hold Voltage | $V_{HOLD}$ | — | — | — | –2.0 | V | |
| XTOSC Stop Detection Time | $T_{STOP}$ | — | 0.1 | — | 1000 | ms | |
| XTOSC Internal Capacitance | $C_G$ | — | 10 | 15 | 20 | pF | |
| XTOSC External Capacitance | $C_{GEX}$ | External $C_G$ option | 10 | — | 30 | pF | |
| XTOSC Internal Capacitance | $C_D$ | — | 10 | 15 | 20 | pF | |
| 400kOSC Internal Capacitance | $C_{OS}$ | — | 8 | 12 | 16 | pF | |
| 400kOSC Oscillation Frequency | $f_{OSC}$ | External resistor $R_{OS}$=100 kΩ $V_{SS2}$ =–2.0 to –3.5 V | 300 | 400 | 620 | kHz | |
| POR Generation Voltage | $V_{POR1}$ | When $V_{SS2}$ is between $V_{POR1}$ and –3.0 V | –0.7 | — | 0 | V | |
| POR Non-generation Voltage | $V_{POR2}$ | No POR when $V_{SS2}$ is between $V_{POR2}$ and –3.0 V | –3 | — | –2 | V | |

Notes: 1. "XTOSC" refers to the 32.768 kHz X'tal oscillation circuit.
2. "400kOSC" refers to the 400 kHz RC oscillation circuit.
3. "POR" refers to Power-On Reset.
4. "$T_{STOP}$" indicates that a system reset occurs if XTOSC stops oscillation for more than this duration.

## DC Characteristics (Continued)

($V_{DD}$=0 V, $V_{SS2}$=$V_{SS}$=–3.0 V, Ta=–40 to +85°C unless otherwise specified)

| Parameter | Symbol | Condition | | Min. | Typ. | Max. | Unit | Measuring Circuit |
|---|---|---|---|---|---|---|---|---|
| Current Comsumption 1 | $I_{DD1}$ | CPU in halt state (400k OSC halt) | Ta=–40 to +40°C | — | 1.5 | 4.5 | µA | 1 |
| | | | Ta=+40 to +85°C | — | 1.5 | 30 | µA | |
| Current Comsumption 2 | $I_{DD2}$ | CPU in operation state (400k OSC halt) | Ta=–40 to +40°C | — | 5 | 15 | µA | |
| | | | Ta=+40 to +85°C | — | 5 | 40 | µA | |
| Current Comsumption 3 | $I_{DD3}$ | CPU in operation state (400k OSC in operation) | | — | 220 | 450 | µA | |
| Current Comsumption 4 | $I_{DD4}$ | Serial transfer, $f_{SCK}$=300 kHz, CPU operation state (400k OSC halt) | Ta=–40 to +40°C | — | 7 | 25 | µA | |
| | | | Ta=+40 to +85°C | — | 7 | 50 | µA | |
| Current Comsumption 5 | $I_{DD5}$ | CPU in halt state (400k OSC halt), A/D converter in oscillation state | RT0=10 kΩ | — | 300 | 450 | µA | |
| | | | RT0=2 kΩ | — | 1300 | 2000 | µA | |

## DC Characteristics (Continued)

($V_{DD}$=0 V, $V_{SS1}$=$V_{SSL}$=–1.5 V, $V_{SS2}$=$V_{SS}$=–3.0 V, $V_{SS3}$=–4.5 V, Ta=–40 to +85°C unless otherwise specified)

| Parameter (Pin Name) | Symbol | Condition | Min. | Typ. | Max. | Unit | Measuring Circuit |
|---|---|---|---|---|---|---|---|
| Output Current 1 (P1.0) | $I_{OH1}$ | $V_{OH1}$=–0.5 V | –6 | –2 | –0.7 | mA | 2 |
| | $I_{OL1}$ | $V_{OL1}$=$V_{SS}$+0.5 V | 3 | 8 | 25 | mA | |
| | $I_{OH1S}$ | $V_{SS}$=–5 V, $V_{OH1S}$=–0.5 V | –36 | –12 | –4 | mA | |
| | $I_{OL1S}$ | $V_{SS}$=–5 V, $V_{OL1}$=$V_{SS}$+0.5 V | 4 | 12 | 36 | mA | |
| Output Current 2 (P1.1 to P1.3) (P2.0 to P2.3) (P3.0 to P3.3) (P4.0 to P4.3) | $I_{OH2}$ | $V_{OH2}$=–0.5 V | –6 | –2 | –0.7 | mA | |
| | $I_{OL2}$ | $V_{OL2}$=$V_{SS}$+0.5 V | 0.7 | 2 | 6 | mA | |
| | $I_{OH2S}$ | $V_{SS}$=–5 V, $V_{OH2S}$=–0.5 V | –9 | –3 | –1 | mA | |
| | $I_{OL2S}$ | $V_{SS}$=–5 V, $V_{OL2}$=$V_{SS}$+0.5 V | 1 | 3 | 9 | mA | |
| Output Current 3 (BD) | $I_{OH3}$ | $V_{OH3}$=–0.7 V | –6 | –2 | –0.7 | mA | |
| | $I_{OL3}$ | $V_{OL3}$=$V_{SS2}$+0.7 V | 0.7 | 2 | 6 | mA | |
| Output Current 4 (RT0, RT1, RS0, RS1, CRT0, CS0, CS1) | $I_{OH4}$ | $V_{OH4}$=–0.1 V | –2.5 | –1.3 | –0.7 | mA | |
| | $I_{OL4}$ | $V_{OL4}$=$V_{SS2}$+0.1 V | 0.7 | 1.3 | 2.5 | mA | |
| Output Current 5 (When L26 to L33 are configured as output ports.) | $I_{OH5}$ | $V_{OH5}$=–0.5 V | –1.5 | –0.6 | –0.15 | mA | |
| | $I_{OL5}$ | $V_{OL5}$=$V_{SS}$+0.5 V | 0.15 | 0.6 | 1.5 | mA | |
| | $I_{OH5S}$ | $V_{SS}$=–5 V, $V_{OH5S}$=–0.5 V | –2.0 | –0.7 | –0.2 | mA | |
| | $I_{OL5S}$ | $V_{SS}$=–5 V, $V_{OL5S}$=$V_{SS}$+0.5 V | 0.2 | 0.7 | 2.0 | mA | |
| Output Current 6 (OSC2) | $I_{OH6}$ | $V_{OH6}$=–0.5 V | –6 | –2 | –0.7 | mA | |
| | $I_{OL6}$ | $V_{OL6}$=$V_{SS2}$+0.5 V | 0.7 | 2 | 6 | mA | |
| Output Current 7 (L0 to L33) | $I_{OH7}$ | $V_{OH7}$=–0.2 V ($V_{DD}$ level) | — | — | –4 | µA | |
| | $I_{OMH7}$ | $V_{OMH7}$=$V_{SS1}$+0.2 V ($V_{SS1}$ level) | 4 | — | — | µA | |
| | $I_{OMH7S}$ | $V_{OMH7S}$=$V_{SS1}$–0.2 V ($V_{SS1}$ level) | — | — | –4 | µA | |
| | $I_{OML7}$ | $V_{OML7}$=$V_{SS2}$+0.2 V ($V_{SS2}$ level) | 4 | — | — | µA | |
| | $I_{OML7S}$ | $V_{OML7S}$=$V_{SS2}$–0.2 V ($V_{SS2}$ level) | — | — | –4 | µA | |
| | $I_{OL7}$ | $V_{OL7}$=$V_{SS3}$+0.2 V ($V_{SS3}$ level) | 4 | — | — | µA | |
| Output Leakage (P1.0 to P1.3) (P2.0 to P2.3) (P3.0 to P3.3) (P4.0 to P4.3) (RT0, RT1, RS0, RS1, CRT0, CS0, CS1) | $I_{OOH}$ | $V_{OH}$=$V_{DD}$ | — | — | 0.3 | µA | |
| | $I_{OOL}$ | $V_{OL}$=$V_{SS2}$ | –0.3 | — | — | µA | |

## DC Characteristics (Continued)

($V_{DD}$=0 V, $V_{SS1}$=$V_{SSL}$=–1.5 V, $V_{SS2}$=$V_{SS}$=–3.0 V, $V_{SS3}$=–4.5 V, Ta=–40 to +85°C unless otherwise specified)

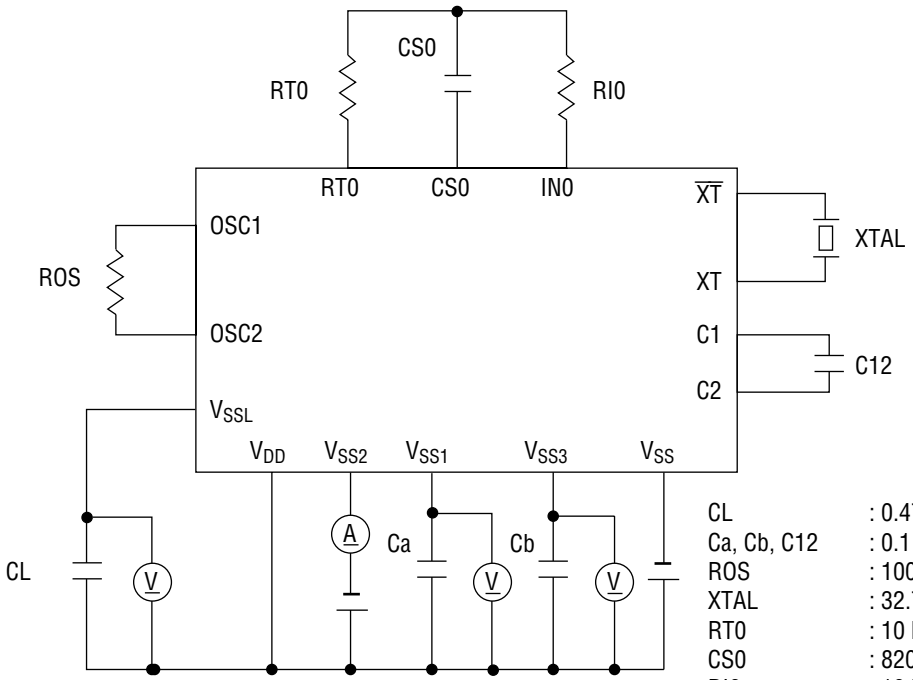
| Parameter (Pin Name) | Symbol | Condition | Min. | Typ. | Max. | Unit | Measuring Circuit |
|---|---|---|---|---|---|---|---|
| Input Current 1 (P0.0 to P0.3) (P2.0 to P2.3) (P3.0 to P3.3) (P4.0 to P4.3) | $I_{IH1}$ | $V_{IH1}$=$V_{DD}$ (pull-down) | 30 | 90 | 300 | µA | 3 |
| | $I_{IL1}$ | $V_{IL1}$=$V_{SS}$ (pull-up) | –300 | –90 | –30 | µA | |
| | $I_{IH1S}$ | $V_{IH1}$=$V_{DD}$, $V_{SS}$=–5 V (pull-down) | 80 | 250 | 800 | µA | |
| | $I_{IL1S}$ | $V_{IL1}$=$V_{SS}$=–5 V (pull-up) | –800 | –250 | –80 | µA | |
| | $I_{IH1Z}$ | $V_{IH1}$=$V_{DD}$ (high impedance) | 0 | — | 1 | µA | |
| | $I_{IL1Z}$ | $V_{IL1}$=$V_{SS}$ (high impedance) | –1 | — | 0 | µA | |
| Input Current 2 (IN0, IN1) | $I_{IH2}$ | $V_{IH2}$=$V_{DD}$ (pull-down) | 30 | 90 | 300 | µA | |
| | $I_{IH2Z}$ | $V_{IH2}$=$V_{DD}$ (high impedance) | 0 | — | 1 | µA | |
| | $I_{IL2Z}$ | $V_{IL2}$=$V_{SS2}$ (high impedance) | –1 | — | 0 | µA | |
| Input Current 3 (OSC1) | $I_{IL3}$ | $V_{IL3}$=$V_{SS2}$ (pull-up) | –300 | –110 | –10 | µA | |
| | $I_{IH3Z}$ | $V_{IH3}$=$V_{DD}$ (high impedance) | 0 | — | 1 | µA | |
| | $I_{IL3Z}$ | $V_{IL3}$=$V_{SS2}$ (high impedance) | –1 | — | 0 | µA | |
| Input Current 4 ($\overline{RESET}$, $\overline{TST1}$, $\overline{TST2}$) | $I_{IH4}$ | $V_{IH4}$=$V_{DD}$ | 0 | — | 1 | µA | |
| | $I_{IL4}$ | $V_{IL4}$=$V_{SS2}$ | –3 | –1.5 | –0.75 | mA | |
| Input Voltage 1 (P0.0 to P0.3) (P2.0 to P2.3) (P3.0 to P3.3) (P4.0 to P4.3) | $V_{IH1}$ | — | –0.6 | — | 0 | V | 4 |
| | $V_{IL1}$ | — | –3.0 | — | –2.4 | V | |
| | $V_{IH1S}$ | $V_{SS}$=–5 V | –1 | — | 0 | V | |
| | $V_{IL1S}$ | $V_{SS}$=–5 V | –5 | — | –4 | V | |
| Input Voltage 2 (IN0, IN1, OSC1) | $V_{IH2}$ | — | –0.6 | — | 0 | V | |
| | $V_{IL2}$ | — | –3.0 | — | –2.4 | V | |
| Input Voltage 3 ($\overline{RESET}$, $\overline{TST1}$, $\overline{TST2}$) | $V_{IH3}$ | — | –0.6 | — | 0 | V | |
| | $V_{IL3}$ | — | –3.0 | — | –2.4 | V | |

## DC Characteristics (Continued)

($V_{DD}$=0 V, $V_{SS1}$=$V_{SSL}$=–1.5 V, $V_{SS2}$=$V_{SS}$=–3.0 V, $V_{SS3}$=–4.5 V, Ta=–40 to +85°C unless otherwise specified)

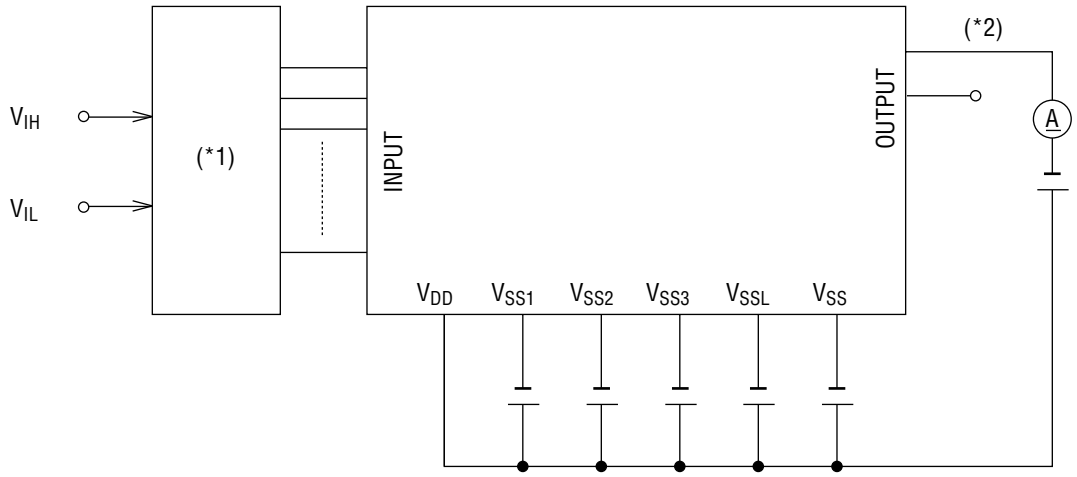
| Parameter (Pin Name) | Symbol | Condition | Min. | Typ. | Max. | Unit | Measuring Circuit |
|---|---|---|---|---|---|---|---|
| Hysteresis Width (P0.0 to P0.3) (P2.0 to P2.3) (P3.0 to P3.3) (P4.0 to P4.3) | $\Delta V_{T1}$ | — | 0.2 | 0.5 | 1 | V | 4 |
| | $\Delta V_{T1S}$ | $V_{SS}$=–5 V | 0.25 | 1.0 | 1.5 | V | |
| Hysteresis Width ($\overline{RESET}$, $\overline{TST1}$, $\overline{TST2}$) | $\Delta V_{T2}$ | — | 0.2 | 0.5 | 1 | V | |
| Input Pin Capacitance (P0.0 to P0.3) (P2.0 to P2.3) (P3.0 to P3.3) (P4.0 to P4.3) | $C_{IN}$ | — | — | — | 5 | pF | 1 |

**Measuring Circuit 1**

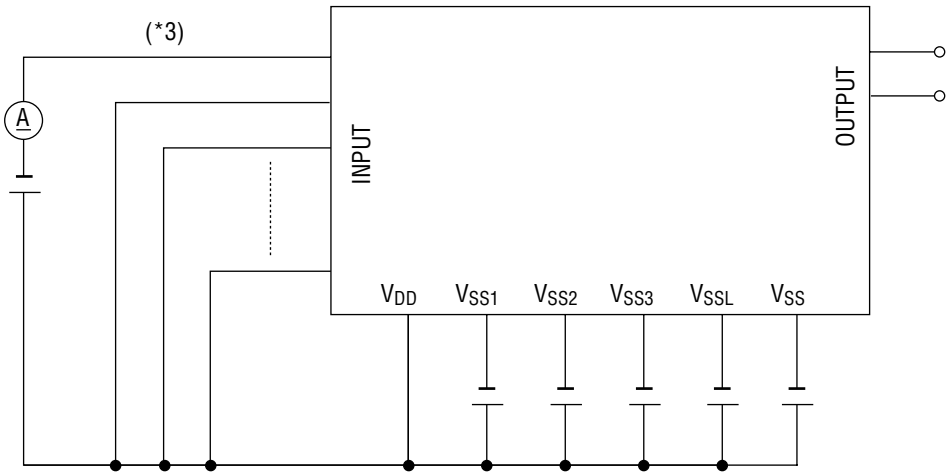



| | |
|---|---|
| CL | : 0.47 µF |
| Ca, Cb, C12 | : 0.1 µF |
| ROS | : 100 kΩ |
| XTAL | : 32.768 kHz |
| RT0 | : 10 kΩ/2 kΩ |
| CS0 | : 820 pF |
| RI0 | : 10 kΩ |

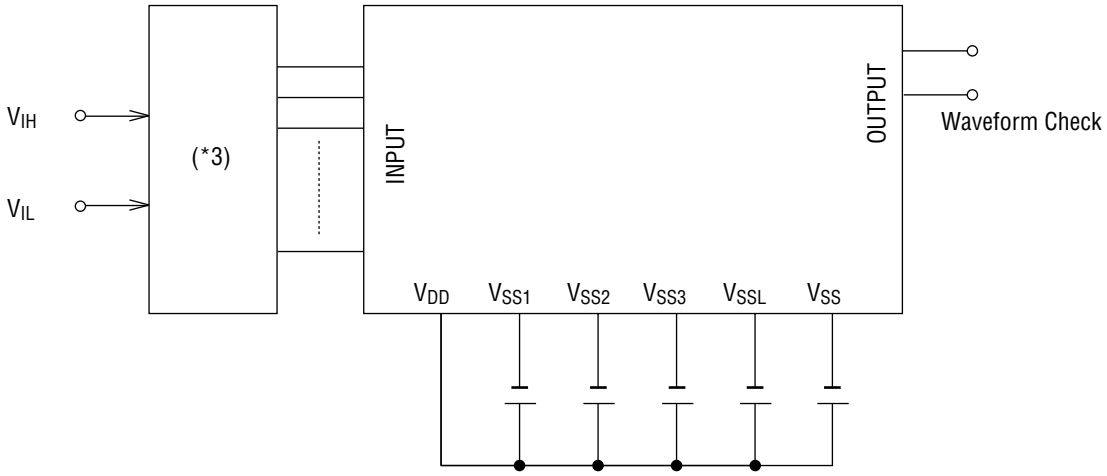
**Measuring Circuit 2**



### Measuring Circuit 3




### Measuring Circuit 4




*1 Input logic to select a specified state.
*2 To be repeated for the specified output pin.
*3 To be repeated for the specified input pin.

### A/D Converter Characteristics

($V_{DD}$=0 V, $V_{SS2}$=$V_{SS}$=–3.0 V, Ta=–40 to +85°C unless otherwise specified)

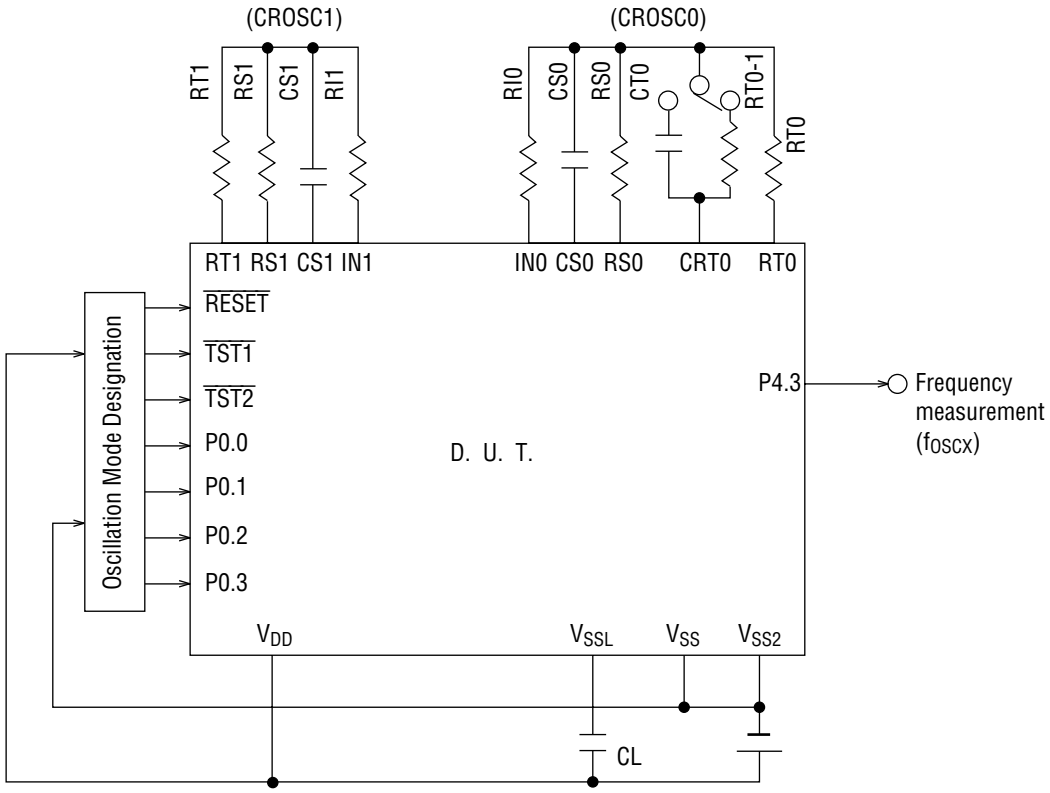
| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit | Measuring Circuit |
|---|---|---|---|---|---|---|---|
| Resistor for Oscillation | RS0, RS1, RT0, RT0-1, RT1 | CS0, CT0, CS1≥740 pF | 1 | — | — | kΩ | 5 |
| Input Current Limiting Resistor | RI0, RI1 | — | 1 | 10 | — | kΩ | |
| Oscillation Frequency | $f_{OSC1}$ | Resistor for oscillation=2 kΩ | 200 | 239 | 277 | kHz | |
| | $f_{OSC2}$ | Resistor for oscillation=10 kΩ | 46.5 | 55.4 | 64.3 | kHz | |
| | $f_{OSC3}$ | Resistor for oscillation=200 kΩ | 2.79 | 3.32 | 3.85 | kHz | |
| RS•RT Oscillation Frequency Ratio (*) | Kf1 | RT0, RT0-1, RT1= 2 kΩ | 4.115 | 4.22 | 4.326 | — | |
| | Kf2 | RT0, RT0-1, RT1=10 kΩ | 0.990 | 1 | 1.010 | — | |
| | Kf3 | RT0, RT0-1, RT1=200 kΩ | 0.0573 | 0.0616 | 0.0659 | — | |

* Kfx is the ratio of the oscillation frequency by a sensor resistor to the oscillation frequency by a reference resistor in the same condition.

$$Kfx = \frac{f_{OSCX}\ (RT0\text{-}CS0\ Oscillation)}{f_{OSCX}\ (RS0\text{-}CS0\ Oscillation)}\ ,\ \frac{f_{OSCX}\ (RT0\text{-}1\text{-}CS0\ Oscillation)}{f_{OSCX}\ (RS0\text{-}CS0\ Oscillation)}\ ,\ \frac{f_{OSCX}\ (RT1\text{-}CS1\ Oscillation)}{f_{OSCX}\ (RS1\text{-}CS1\ Oscillation)}$$

(X=1,2,3)

**Measuring Circuit 5**

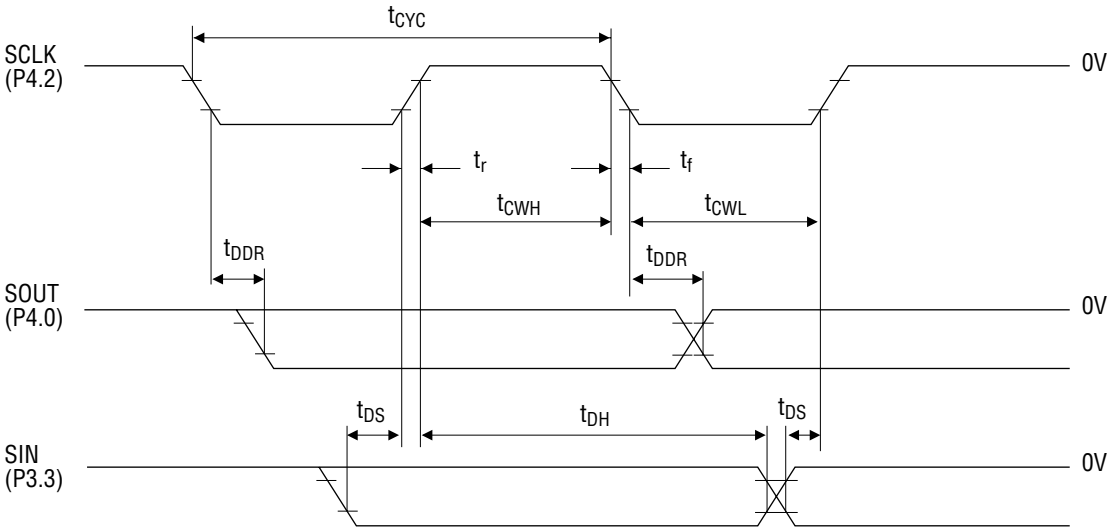



RT0, RT0-1, RT1 = 2 kΩ/10 kΩ/200 kΩ
RS0, RS1 = 10 kΩ
RI0, RI1 = 10 kΩ
CS0, CT0, CS1 = 820 pF
CL = 0.47 μF

### AC Characteristics (Serial Interface)

($V_{DD}$=0 V, $V_{SS2}$=–3 V, $V_{SS}$=–5 V, Ta=–40 to +85°C)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| SCLK Input Fall Time | $t_f$ | — | — | — | 1 | µs |
| SCLK Input Rise Time | $t_r$ | — | — | — | 1 | µs |
| SCLK Input "L" Level Pulse Width | $t_{CWL}$ | — | 0.8 | — | — | µs |
| SCLK Input "H" Level Pulse Width | $t_{CWH}$ | — | 0.8 | — | — | µs |
| SCLK Input Cycle Time | $t_{CYC}$ | — | 2.0 | — | — | µs |
| SCLK Output Cycle Time | $t_{CYC1(○)}$ | CPU is operating at 32 kHz | — | 30.5 | — | µs |
| SCLK Output Cycle Time | $t_{CYC2(○)}$ | CPU is operating at 400 kHz | — | 2.5 | — | µs |
| SOUT Output delay Time | $t_{DDR}$ | CL=10pF | — | — | 0.4 | µs |
| SIN Input Setup Time | $t_{DS}$ | — | 0.5 | — | — | µs |
| SIN Input Hold TIme | $t_{DH}$ | — | 0.8 | — | — | µs |




("H" level=–1 V, "L" level=–4 V)

## FUNCTIONAL DESCRIPTION

### CPU Peripheral Function

**• A/D converter (ADC)**

The MSM64164C has a built-in two-channel RC oscillation A/D converter. The A/D converter is composed of a two-channel oscillation circuit, Counter A (CNTA0 to 4 is a 4.8-digit decade counter), Counter B (CNTB0 to 3 is a 14-bit binary counter), and A/D Converter Control Registers 0 and 1 (ADCON0, ADCON1).

By counting oscillation frequencies due to a resistor or capacitor connected to the RC oscillation circuit, the A/D converter converts resistance values or capacitance values to corresponding digital values. By using a thermistor or humidity sensor as a resistance, a thermometer or a hygrometer can be constructed. By applying sensors to the two-channel RC oscillation circuit, it is also possible to extend measurement ranges or measurement at two places.

**• Serial port (SIOP)**

The MSM64164C has an 8-bit synchronous serial port. Receive/transmit operation of the serial port is performed simultaneously and the serial transfer clock can select either internal or external mode. Direction of transfer data can be big endian or little endian. Each pin of the serial port is assigned as secondary functions of P3.3 and P4.0 to P4.2. Setting each bit of SIN, SOUT, SPR and SCLK of P33CON and P40CON to P42CON to "1" makes each pin valid.

**• LCD driver (LCD)**

The MSM64164C has a built-in LCD driver for 34 outputs.

The LCD driver consists of 31 × 4-bit display registers (DSPR0 to 30), a Display Control Register (DSPCON), a 34-output LCD driver circuit, and a bias generation circuit (BIAS).

There are three types of driving methods: 1/4 duty, 1/3 duty and 1/2 duty.

A mask option can select either a common driver or a segment driver for each LCD driver pin.

A mask option can also specify assignment of each bit of the display register to each segment.

All the display registers must be selected by a mask option.

L26 to L33 of the LCD driver can become output ports by a mask option.

The relationship between the duty, the bias method, and the maximum segment number follows:

1/4 duty 1/3 bias method --------120 segments
1/3 duty 1/3 bias method --------93 segments
1/2 duty 1/2 bias method --------64 segments

**• Buzzer driver (BD)**

The MSM64164C has a built-in buzzer driver with 15 buzzer output frequencies and four buzzer output modes. Each buzzer output is selected by the Buzzer Control Register (BDCON) and the Buzzer Frequency Control Register (BFCON).

**• Capture circuit (CAPR)**

The MSM64164C captures 32 Hz to 256 Hz output of the time base counter at the falling of Port 0.0 or 0.1 (P0.0 or P0.1) to "L" level when the pull-up resistance input is chosen or at the rising to "H" level when the pull-down resistance input is chosen. The capture circuit is composed of the Capture Control Register (CAPCON) and the Capture Registers (CAPR0, CAPR1) that fetch output from the time base counter.

**• Watchdog timer (WDT)**

The MSM64164C has a built-in watchdog timer for reliable CPU operation. The watchdog timer is composed of a 6-bit watchdog timer counter (WDTC) to count a 16Hz output and a watchdog timer control register (WDTCON) to reset WDTC.

**• Clock generation circuit (2CLK)**

The clock generation circuit (2CLK) in the MSM64164C contains a 32.768 kHz crystal oscillation circuit, a 400 kHz RC oscillation circuit, and a clock control port. This circuit generates the system clock (CLK) and the time base clock (32.768 kHz).

The system clock drives the CPU while the time base clock drives the time base counter and the buzzer driver.

Via the contents of the frequency Control Register (FCON), the system clock can be switched between 32.768 kHz (the output of the X'tal oscillation circuit) and 400 kHz (the output of the RC oscillation circuit).

Note: The oscillation frequency of the RC oscillation circuit varies depending on the value of an external resistor ($R_{OS}$), operating power supply voltage ($V_{DD}$), and ambient temperatures (Ta). In this manual, the output of the RC oscillation circuit is taken as 400 kHz for convenience.

**• Time base counter (TBC)**

The MSM64164C has a built-in time base counter (TBC) that generates clocks to be supplied to internal peripheral circuits. The time base counter is composed of 15 binary counters. The count clock of the time base is driven by the oscillation clock (32.768 kHz) of the crystal oscillation circuit. The output of the time base counter is used for the buzzer driver, the system reset circuit, the watchdog timer, the time base interrupt, the sampling clocks of each port, and the capture circuit.

**• I/O port**

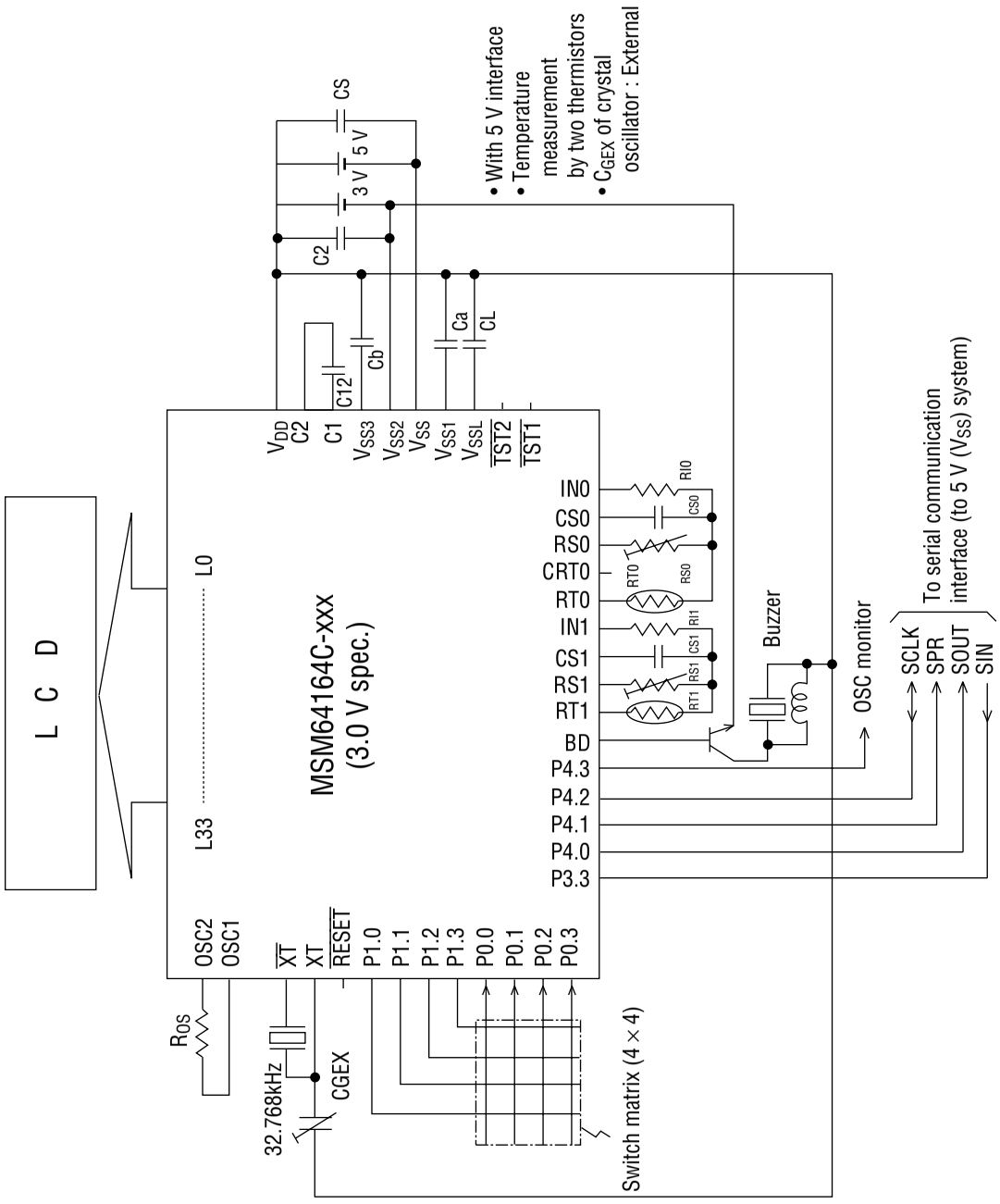
| | | |
|---|---|---|
| Input-output ports (P2, P3, P4) (12 bits) | : | Pull-up (down) input, high Z input, CMOS output, NMOS open-drain output ; settable individually, "0" for external interrupts. |
| Input ports (P0) (4 bits) | : | Pull-up (down) input, high Z input, "1" for external interrupts. |
| Output ports (P1) (4 bits) | : | CMOS output, NMOS open drain output. |

**• Interrupt (INTC)**

The MSM64164C has ten interrupt sources (10 vector addresses) of which two are external interrupts from ports and eight are internal interrupts.

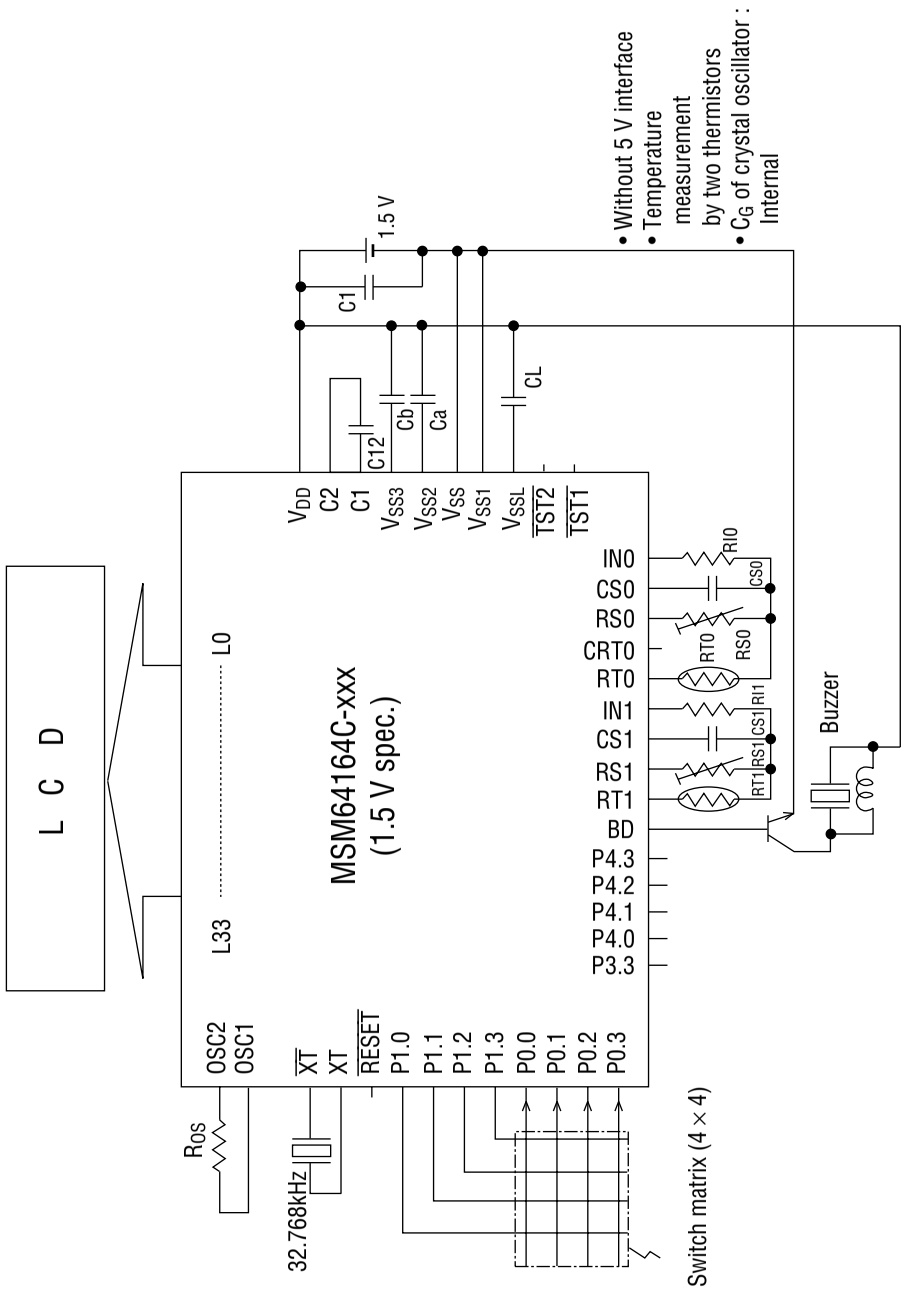
Of the ten interrupt sources, only the watchdog interrupt cannot be disabled (non-maskable interrupt). The other nine interrupts are controlled by the master interrupt enable flag (MI) and the interrupt enable the registers (IE0, IE1 and IE2). When an interrupt condition is met, CPU the branches to a vector address corresponding to the interrupt source.

## APPLICATION CIRCUITS




**3.0 V Spec. Application Circuit**

## APPLICATION CIRCUITS (Continued)




**1.5 V Spec. Application Circuit**