

### Low Noise, Low Power I<sup>2</sup>C™ Bus, 128 Taps

The ISL22316 integrates a single digitally controlled potentiometer (DCP) and non-volatile memory on a monolithic CMOS integrated circuit.

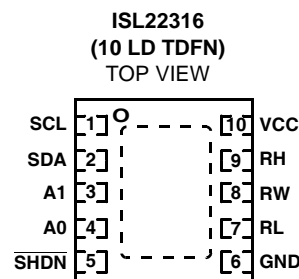
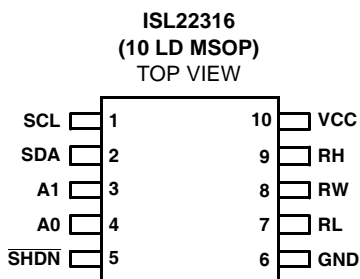
The digitally controlled potentiometer is implemented with a combination of resistor elements and CMOS switches. The position of the wipers are controlled by the user through the I<sup>2</sup>C bus interface. The potentiometer has an associated volatile Wiper Register (WR) and a non-volatile Initial Value Register (IVR) that can be directly written to and read by the user. The contents of the WR controls the position of the wiper. At power-up, the device recalls the contents of the DCP's IVR to the WR.

The DCP can be used as a three-terminal potentiometer or as a two-terminal variable resistor in a wide variety of applications including control, parameter adjustments, and signal processing.

### Features

- 128 resistor taps
- I<sup>2</sup>C serial interface
  - Two address pins, up to four devices/bus
- Non-volatile storage of wiper position
- Wiper resistance: 70Ω typical @ V<sub>CC</sub> = 3.3V
- Shutdown mode
- Shutdown current 5μA max
- Power supply: 2.7V to 5.5V
- 50kΩ or 10kΩ total resistance
- High reliability
  - Endurance: 1,000,000 data changes per bit per register
  - Register data retention: 50 years @ T ≤ +55°C
- 10 Ld MSOP or 10 Ld TDFN package
- Pb-free (RoHS compliant)

### Pinouts



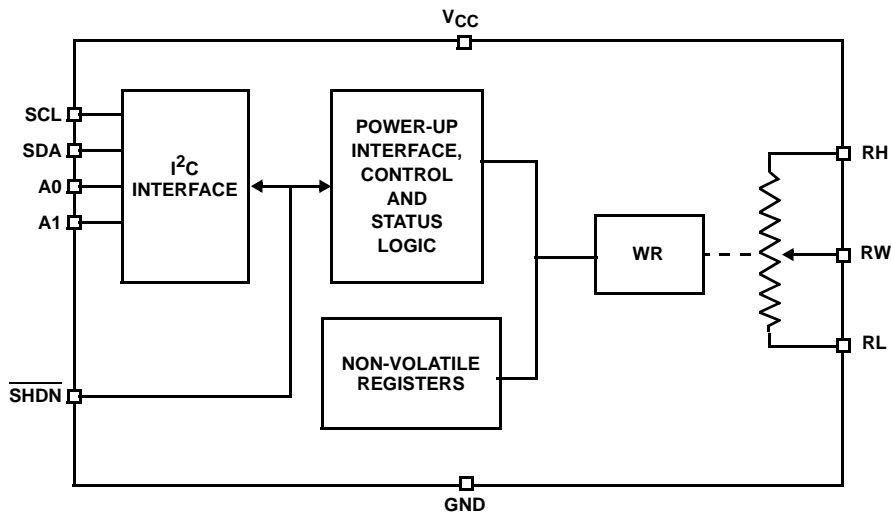
### Ordering Information

| PART NUMBER<br>(Note) | PART MARKING | RESISTANCE OPTION<br>(kΩ) | TEMP. RANGE<br>(°C) | PACKAGE<br>(Pb-free) | PKG. DWG. # |
|-----------------------|--------------|---------------------------|---------------------|----------------------|-------------|
| ISL22316UFU10Z*       | 316UZ        | 50                        | -40 to +125         | 10 Ld MSOP           | M10.118     |
| ISL22316WUFU10Z*      | 316WZ        | 10                        | -40 to +125         | 10 Ld MSOP           | M10.118     |
| ISL22316UFRT10Z*      | 316U         | 50                        | -40 to +125         | 10 Ld 3x3 TDFN       | L10.3x3B    |
| ISL22316WFRT10Z*      | 316W         | 10                        | -40 to +125         | 10 Ld 3x3 TDFN       | L10.3x3B    |

\*Add "-TK" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

## Block Diagram



## Pin Descriptions

| MSOP PIN NUMBER | TDFN PIN NUMBER | PIN NAME                 | DESCRIPTION   |
|-----------------|-----------------|--------------------------|---|
| 1               | 1               | SCL                      | Open drain I <sup>2</sup> C interface clock input             |
| 2               | 2               | SDA                      | Open drain Serial data I/O for the I <sup>2</sup> C interface |
| 3               | 3               | A1                       | Device address input for the I <sup>2</sup> C interface       |
| 4               | 4               | A0                       | Device address input for the I <sup>2</sup> C interface       |
| 5               | 5               | $\overline{\text{SHDN}}$ | Shutdown active low input                                     |
| 6               | 6               | GND                      | Device ground pin   |
| 7               | 7               | RL                       | "Low" terminal of DCP   |
| 8               | 8               | RW                       | "Wiper" terminal of DCP                                       |
| 9               | 9               | RH                       | "High" terminal of DCP  |
| 10              | 10              | VCC                      | Power supply pin  |

**Absolute Maximum Ratings**

|  |                               |
|--|-------------------------------|
| Storage Temperature                                      | -65°C to +150°C               |
| Voltage at any Digital Interface Pin with Respect to GND | -0.3V to V <sub>CC</sub> +0.3 |
| V <sub>CC</sub>  | -0.3V to +6V                  |
| Voltage at any DCP Pin with Respect to GND               | -0.3V to V <sub>CC</sub>      |
| I <sub>W</sub> (10s)                                     | ±6mA                          |
| Latchup (Note 1)   | Class II, Level B @ +125°C    |
| <b>ESD Ratings</b>                                       |                               |
| Human Body Model   | .5kV                          |
| Charge Device Model                                      | 1kV                           |

**Thermal Information**

|  |   |                      |
|--|---|----------------------|
| Thermal Resistance (Typical)                   | $\theta_{JA}$ (°C/W)  | $\theta_{JC}$ (°C/W) |
| 10 Lead MSOP (Note 2)                          | 162   | N/A                  |
| 10 Lead TDFN (Notes 3, 4)                      | 74  | 7                    |
| Maximum Junction Temperature (Plastic Package) | +150°C  |                      |
| Pb-free Reflow Profile                         | see link below<br><a href="http://www.intersil.com/pbfree/Pb-FreeReflow.asp">http://www.intersil.com/pbfree/Pb-FreeReflow.asp</a> |                      |

**Recommended Operating Conditions**

|   |                 |
|---|-----------------|
| Temperature Range (Extended Industrial) | -40°C to +125°C |
| V <sub>CC</sub>                         | 2.7V to 5.5V    |
| Power Rating of each DCP                | .5mW            |
| Wiper Current of each DCP               | ±3.0mA          |

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

**NOTES:**

- Jedec Class II pulse conditions and failure criterion used. Level B exceptions are: using a max positive pulse of 6.5V on the SHDN pin, and using a max negative pulse of -1V for all pins.
- $\theta_{JA}$  is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
- $\theta_{JA}$  is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
- For  $\theta_{JC}$ , the "case temp" location is the center of the exposed metal pad on the package underside.

**Analog Specifications** Over recommended operating conditions, unless otherwise stated.

| SYMBOL  | PARAMETER   | TEST CONDITIONS   | MIN (Note 19) | TYP (Note 5) | MAX (Note 19)   | UNIT             |
|---|---|---|---------------|--------------|-----------------|------------------|
| R <sub>TOTAL</sub>  | R <sub>H</sub> to R <sub>L</sub> Resistance           | W option  |               | 10           |                 | k $\Omega$       |
|   |   | U option  |               | 50           |                 | k $\Omega$       |
|   | R <sub>H</sub> to R <sub>L</sub> Resistance Tolerance |   | -20           |              | +20             | %                |
|   |   | End-to-End Temperature Coefficient  | W option      |              | ±50             |                  |
|   |   | U option  |               | ±80          |                 | ppm/°C (Note 18) |
| R <sub>W</sub>  | Wiper Resistance                                      | V <sub>CC</sub> = 3.3V, wiper current = V <sub>CC</sub> /R <sub>TOTAL</sub> |               | 70           | 200             | $\Omega$         |
| V <sub>RH</sub> , V <sub>RL</sub>   | V <sub>RH</sub> and V <sub>RL</sub> Terminal Voltages | V <sub>RH</sub> and V <sub>RL</sub> to GND                                  | 0             |              | V <sub>CC</sub> | V                |
| C <sub>H</sub> /C <sub>L</sub> /C <sub>W</sub> (Note 18)  | Potentiometer Capacitance                             |   |               | 10/10/25     |                 | pF               |
| I <sub>LkgDCP</sub>   | Leakage on DCP Pins                                   | Voltage at pin from GND to V <sub>CC</sub>                                  |               | 0.1          | 1               | $\mu$ A          |
| <b>VOLTAGE DIVIDER MODE (0V @ R<sub>L</sub>; V<sub>CC</sub> @ R<sub>H</sub>; measured at R<sub>W</sub>, unloaded)</b> |   |   |               |              |                 |                  |
| INL (Note 10)   | Integral Non-linearity                                | Monotonic over all tap positions, W and U option                            | -1            |              | 1               | LSB (Note 6)     |
| DNL (Note 9)  | Differential Non-linearity                            | Monotonic over all tap positions, W and U option                            | -0.5          |              | 0.5             | LSB (Note 6)     |
| ZSerror (Note 7)  | Zero-scale Error                                      | W option  | 0             | 1            | 5               | LSB (Note 6)     |
|   |   | U option  | 0             | 0.5          | 2               |                  |
| FSerror (Note 8)  | Full-scale Error                                      | W option  | -5            | -1           | 0               | LSB (Note 6)     |
|   |   | U option  | -2            | -1           | 0               |                  |
| TC <sub>V</sub> (Notes 11, 18)  | Ratiometric Temperature Coefficient                   | DCP register set to 40 hex for W and U option                               |               | ±4           |                 | ppm/°C           |

**Analog Specifications** Over recommended operating conditions, unless otherwise stated. (Continued)

| SYMBOL  | PARAMETER                  | TEST CONDITIONS  | MIN<br>(Note 19) | TYP<br>(Note 5) | MAX<br>(Note 19) | UNIT            |
|---|----------------------------|--|------------------|-----------------|------------------|-----------------|
| <b>RESISTOR MODE</b> (Measurements between $R_W$ and $R_L$ with $R_H$ not connected, or between $R_W$ and $R_H$ with $R_L$ not connected) |                            |  |                  |                 |                  |                 |
| RINL<br>(Note 15)   | Integral Non-linearity     | DCP register set between 10 hex and 7F hex; monotonic over all tap positions; W and U option | -1               |                 | 1                | MI<br>(Note 12) |
| RDNL<br>(Note 14)   | Differential Non-linearity | W option   | -1               |                 | 1                | MI<br>(Note 12) |
|   |                            | U option   | -0.5             |                 | 0.5              | MI<br>(Note 12) |
| Roffset<br>(Note 13)  | Offset                     | W option   | 0                | 1               | 5                | MI<br>(Note 12) |
|   |                            | U option   | 0                | 0.5             | 2                | MI<br>(Note 12) |

**Operating Specifications** Over the recommended operating conditions, unless otherwise specified.

| SYMBOL                     | PARAMETER   | TEST CONDITIONS   | MIN<br>(Note 19) | TYP<br>(Note 5) | MAX<br>(Note 19) | UNIT |
|----------------------------|---|---|------------------|-----------------|------------------|------|
| $I_{CC1}$                  | $V_{CC}$ Supply Current (Volatile Write/Read)                           | $f_{SCL} = 400\text{kHz}$ ; SDA = Open; (for I <sup>2</sup> C, active, read and write states)                             |                  |                 | 0.5              | mA   |
| $I_{CC2}$                  | $V_{CC}$ Supply Current (Non-volatile Write/Read)                       | $f_{SCL} = 400\text{kHz}$ ; SDA = Open; (for I <sup>2</sup> C, active, read and write states)                             |                  |                 | 3                | mA   |
| $I_{SB}$                   | $V_{CC}$ Current (Standby)  | $V_{CC} = +5.5\text{V}$ @ +85°C, I <sup>2</sup> C interface in standby state  |                  |                 | 5                | μA   |
|                            |   | $V_{CC} = +5.5\text{V}$ @ +125°C, I <sup>2</sup> C interface in standby state   |                  |                 | 7                | μA   |
|                            |   | $V_{CC} = +3.6\text{V}$ @ +85°C, I <sup>2</sup> C interface in standby state  |                  |                 | 3                | μA   |
|                            |   | $V_{CC} = +3.6\text{V}$ @ +125°C, I <sup>2</sup> C interface in standby state   |                  |                 | 5                | μA   |
| $I_{SD}$                   | $V_{CC}$ Current (Shutdown)   | $V_{CC} = +5.5\text{V}$ @ +85°C, I <sup>2</sup> C interface in standby state  |                  |                 | 3                | μA   |
|                            |   | $V_{CC} = +5.5\text{V}$ @ +125°C, I <sup>2</sup> C interface in standby state   |                  |                 | 5                | μA   |
|                            |   | $V_{CC} = +3.6\text{V}$ @ +85°C, I <sup>2</sup> C interface in standby state  |                  |                 | 2                | μA   |
|                            |   | $V_{CC} = +3.6\text{V}$ @ +125°C, I <sup>2</sup> C interface in standby state   |                  |                 | 4                | μA   |
| $I_{LkgDig}$               | Leakage Current, at Pins A0, A1, $\overline{\text{SHDN}}$ , SDA and SCL | Voltage at pin from GND to $V_{CC}$ , SDA is inactive   | -1               |                 | 1                | μA   |
| $t_{DCP}$<br>(Note 18)     | DCP Wiper Response Time   | SCL falling edge of last bit of DCP data byte to wiper new position   |                  | 1.5             |                  | μs   |
| $t_{ShdnRec}$<br>(Note 18) | DCP Recall Time from Shutdown Mode                                      | From rising edge of $\overline{\text{SHDN}}$ signal to wiper stored position and RH connection                            |                  | 1.5             |                  | μs   |
|                            |   | SCL falling edge of last bit of ACR data byte to wiper stored position and RH connection                                  |                  | 1.5             |                  | μs   |
| $V_{por}$                  | Power-on Recall Voltage   | Minimum $V_{CC}$ at which memory recall occurs  | 2.0              |                 | 2.6              | V    |
| $V_{CCRamp}$               | $V_{CC}$ Ramp Rate  |   | 0.2              |                 |                  | V/ms |
| $t_D$                      | Power-up Delay  | $V_{CC}$ above $V_{por}$ , to DCP Initial Value Register recall completed and I <sup>2</sup> C Interface in standby state |                  |                 | 3                | ms   |

**Operating Specifications** Over the recommended operating conditions, unless otherwise specified. (Continued)

| SYMBOL                                 | PARAMETER   | TEST CONDITIONS  | MIN<br>(Note 19)     | TYP<br>(Note 5) | MAX<br>(Note 19)   | UNIT   |
|--|---|--|----------------------|-----------------|--------------------|--------|
| <b>EEPROM SPECIFICATION</b>            |   |  |                      |                 |                    |        |
|  | EEPROM Endurance  |  | 1,000,000            |                 |                    | Cycles |
|  | EEPROM Retention  | Temperature $T \leq +55^{\circ}\text{C}$   | 50                   |                 |                    | Years  |
| $t_{WC}$<br>(Note 17)                  | Non-volatile Write Cycle Time   |  |                      | 12              | 20                 | ms     |
| <b>SERIAL INTERFACE SPECIFICATIONS</b> |   |  |                      |                 |                    |        |
| $V_{IL}$                               | A1, A0, $\overline{\text{SHDN}}$ , SDA, and SCL Input Buffer LOW Voltage  |  | -0.3                 |                 | $0.3 \cdot V_{CC}$ | V      |
| $V_{IH}$                               | A1, A0, $\overline{\text{SHDN}}$ , SDA, and SCL Input Buffer HIGH Voltage |  | $0.7 \cdot V_{CC}$   |                 | $V_{CC} + 0.3$     | V      |
| Hysteresis                             | SDA and SCL Input Buffer Hysteresis                                       |  | $0.05 \cdot V_{CC}$  |                 |                    | V      |
| $V_{OL}$                               | SDA Output Buffer LOW Voltage, Sinking 4mA                                |  | 0                    |                 | 0.4                | V      |
| $C_{pin}$<br>(Note 18)                 | A1, A0, $\overline{\text{SHDN}}$ , SDA, and SCL Pin Capacitance           |  |                      | 10              |                    | pF     |
| $f_{SCL}$                              | SCL Frequency   |  |                      |                 | 400                | kHz    |
| $t_{sp}$                               | Pulse Width Suppression Time at SDA and SCL Inputs                        | Any pulse narrower than the max spec is suppressed   |                      |                 | 50                 | ns     |
| $t_{AA}$                               | SCL Falling Edge to SDA Output Data Valid                                 | SCL falling edge crossing 30% of $V_{CC}$ , until SDA exits the 30% to 70% of $V_{CC}$ window                              |                      |                 | 900                | ns     |
| $t_{BUF}$                              | Time the Bus Must be Free Before the Start of a New Transmission          | SDA crossing 70% of $V_{CC}$ during a STOP condition, to SDA crossing 70% of $V_{CC}$ during the following START condition | 1300                 |                 |                    | ns     |
| $t_{LOW}$                              | Clock LOW Time  | Measured at the 30% of $V_{CC}$ crossing   | 1300                 |                 |                    | ns     |
| $t_{HIGH}$                             | Clock HIGH Time   | Measured at the 70% of $V_{CC}$ crossing   | 600                  |                 |                    | ns     |
| $t_{SU:STA}$                           | START Condition Setup Time  | SCL rising edge to SDA falling edge; both crossing 70% of $V_{CC}$   | 600                  |                 |                    | ns     |
| $t_{HD:STA}$                           | START Condition Hold Time   | From SDA falling edge crossing 30% of $V_{CC}$ to SCL falling edge crossing 70% of $V_{CC}$                                | 600                  |                 |                    | ns     |
| $t_{SU:DAT}$                           | Input Data Setup Time   | From SDA exiting the 30% to 70% of $V_{CC}$ window, to SCL rising edge crossing 30% of $V_{CC}$                            | 100                  |                 |                    | ns     |
| $t_{HD:DAT}$                           | Input Data Hold Time  | From SCL rising edge crossing 70% of $V_{CC}$ to SDA entering the 30% to 70% of $V_{CC}$ window                            | 0                    |                 |                    | ns     |
| $t_{SU:STO}$                           | STOP Condition Setup Time   | From SCL rising edge crossing 70% of $V_{CC}$ , to SDA rising edge crossing 30% of $V_{CC}$                                | 600                  |                 |                    | ns     |
| $t_{HD:STO}$                           | STOP Condition Hold Time for Read, or Volatile Only Write                 | From SDA rising edge to SCL falling edge; both crossing 70% of $V_{CC}$  | 1300                 |                 |                    | ns     |
| $t_{DH}$                               | Output Data Hold Time   | From SCL falling edge crossing 30% of $V_{CC}$ , until SDA enters the 30% to 70% of $V_{CC}$ window                        | 0                    |                 |                    | ns     |
| $t_R$                                  | SDA and SCL Rise Time   | From 30% to 70% of $V_{CC}$  | $20 + 0.1 \cdot C_b$ |                 | 250                | ns     |
| $t_F$                                  | SDA and SCL Fall Time   | From 70% to 30% of $V_{CC}$  | $20 + 0.1 \cdot C_b$ |                 | 250                | ns     |
| $C_b$                                  | Capacitive Loading of SDA or SCL  | Total on-chip and off-chip   | 10                   |                 | 400                | pF     |

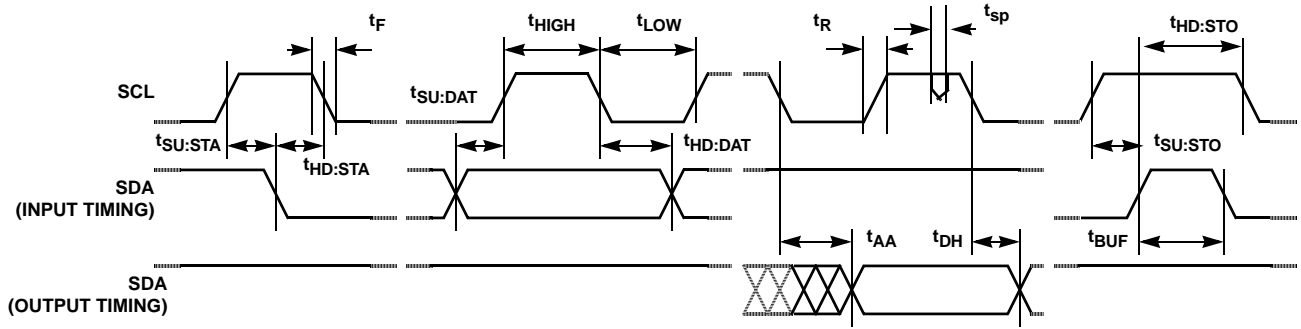
**Operating Specifications** Over the recommended operating conditions, unless otherwise specified. (Continued)

| SYMBOL            | PARAMETER                                 | TEST CONDITIONS   | MIN<br>(Note 19) | TYP<br>(Note 5) | MAX<br>(Note 19) | UNIT |
|-------------------|---|---|------------------|-----------------|------------------|------|
| R <sub>pu</sub>   | SDA and SCL Bus Pull-up Resistor Off-chip | Maximum is determined by t <sub>R</sub> and t <sub>F</sub><br>For C <sub>b</sub> = 400pF, max is about 2kΩ–2.5kΩ<br>For C <sub>b</sub> = 40pF, max is about 15kΩ–20kΩ | 1                |                 |                  | kΩ   |
| t <sub>SU:A</sub> | A1 and A0 Setup Time                      | Before START condition  | 600              |                 |                  | ns   |
| t <sub>HD:A</sub> | A1 and A0 Hold Time                       | After STOP condition  | 600              |                 |                  | ns   |

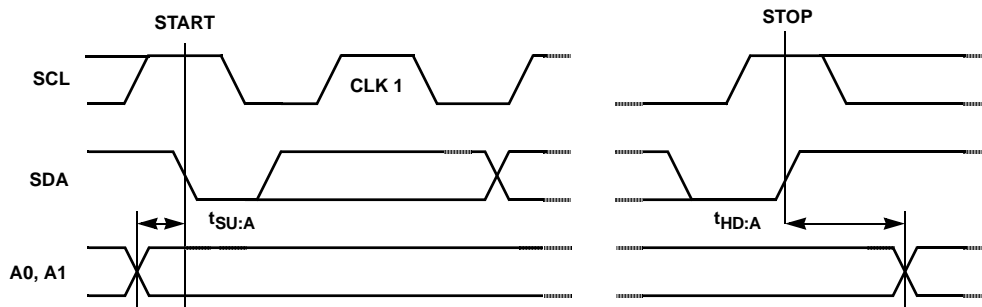
NOTES:

5. Typical values are for T<sub>A</sub> = +25°C and 3.3V supply voltage.
6. LSB:  $[V(RW)_{127} - V(RW)_0]/127$ . V(RW)<sub>127</sub> and V(RW)<sub>0</sub> are V(RW) for the DCP register set to 7F hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.
7. ZS error = V(RW)<sub>0</sub>/LSB.
8. FS error =  $[V(RW)_{127} - V_{CC}]/LSB$ .
9. DNL =  $[V(RW)_i - V(RW)_{i-1}]/LSB - 1$ , for i = 1 to 127. i is the DCP register setting.
10. INL =  $[V(RW)_i - (i \cdot LSB) - V(RW)_0]/LSB$  for i = 1 to 127
11.  $T_{CV} = \frac{\text{Max}(V(RW)_i) - \text{Min}(V(RW)_i)}{[\text{Max}(V(RW)_i) + \text{Min}(V(RW)_i)]/2} \times \frac{10^6}{+165^\circ\text{C}}$  for i = 16 to 127 decimal, T = -40°C to +125°C. Max( ) is the maximum value of the wiper voltage and Min ( ) is the minimum value of the wiper voltage over the temperature range.
12. MI =  $|RW_{127} - RW_0|/127$ . MI is a minimum increment. RW<sub>127</sub> and RW<sub>0</sub> are the measured resistances for the DCP register set to 7F hex and 00 hex respectively.
13. Roffset = RW<sub>0</sub>/MI, when measuring between RW and RL.  
Roffset = RW<sub>127</sub>/MI, when measuring between RW and RH.
14. RDNL = (RW<sub>i</sub> - RW<sub>i-1</sub>)/MI - 1, for i = 16 to 127.
15. RINL =  $[RW_i - (MI \cdot i) - RW_0]/MI$ , for i = 16 to 127.
16.  $T_{CR} = \frac{[\text{Max}(Ri) - \text{Min}(Ri)]}{[\text{Max}(Ri) + \text{Min}(Ri)]/2} \times \frac{10^6}{+165^\circ\text{C}}$  for i = 16 to 127, T = -40°C to +125°C. Max( ) is the maximum value of the resistance and Min ( ) is the minimum value of the resistance over the temperature range.
17. t<sub>WC</sub> is the time from a valid STOP condition at the end of a Write sequence of I2C serial interface, to the end of the self-timed internal non-volatile write cycle.
18. Limits should be considered typical and are not production tested.
19. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

SDA vs SCL Timing



A0 and A1 Pin Timing



Typical Performance Curves

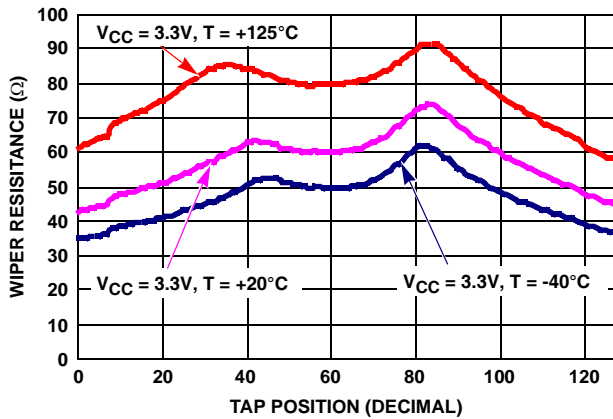


FIGURE 1. WIPER RESISTANCE vs TAP POSITION [  $I(RW) = V_{CC}/R_{TOTAL}$  ] FOR 10k $\Omega$  (W)

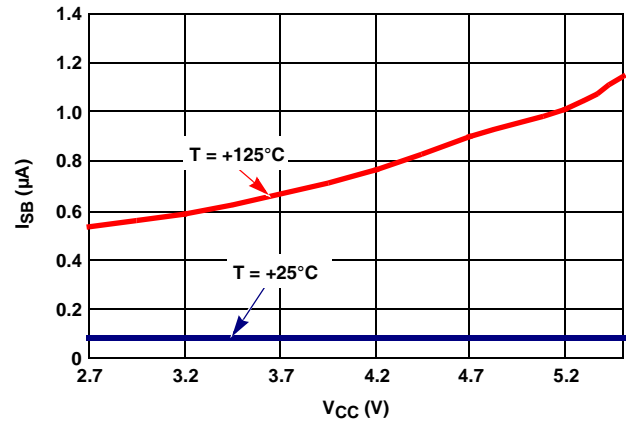


FIGURE 2. STANDBY  $I_{CC}$  vs  $V_{CC}$

Typical Performance Curves (Continued)

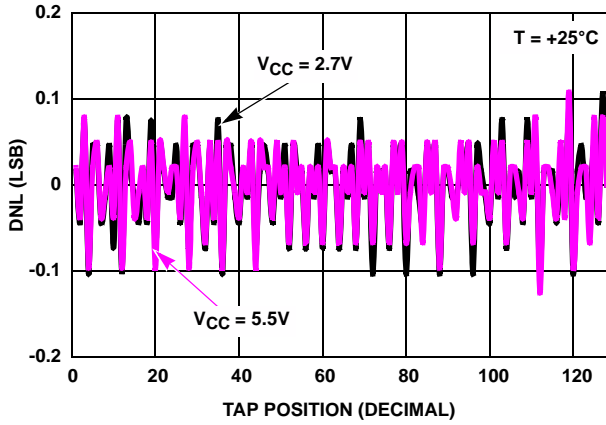


FIGURE 3. DNL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

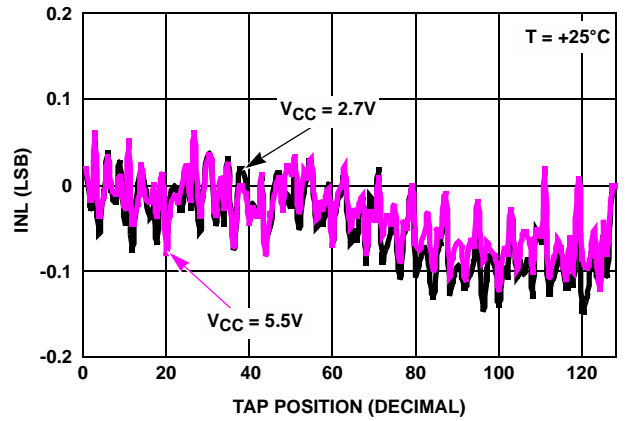


FIGURE 4. INL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

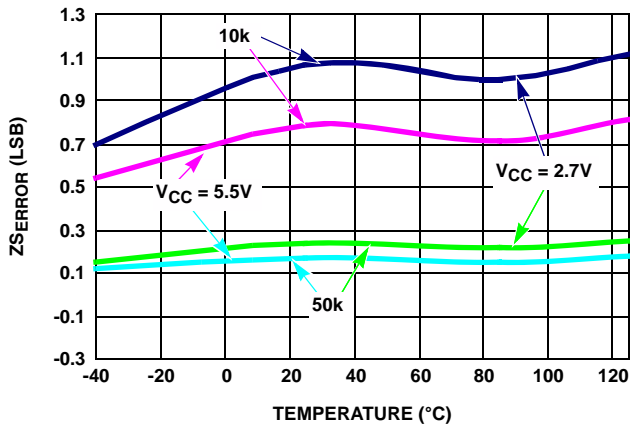


FIGURE 5. ZSEERROR vs TEMPERATURE

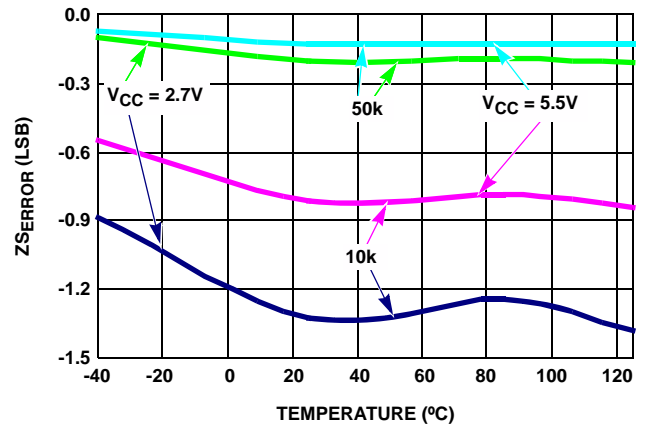


FIGURE 6. FSEERROR vs TEMPERATURE

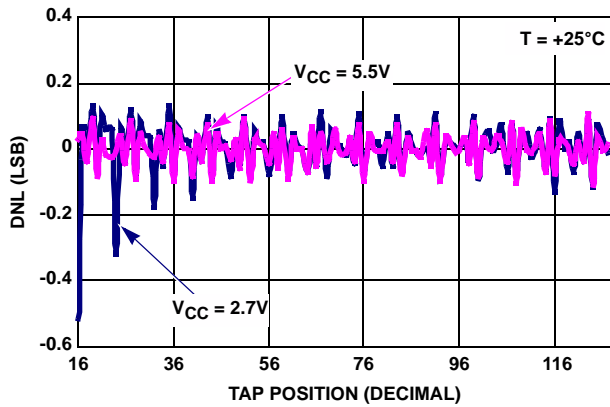


FIGURE 7. DNL vs TAP POSITION IN RHEOSTAT MODE FOR 10kΩ (W)

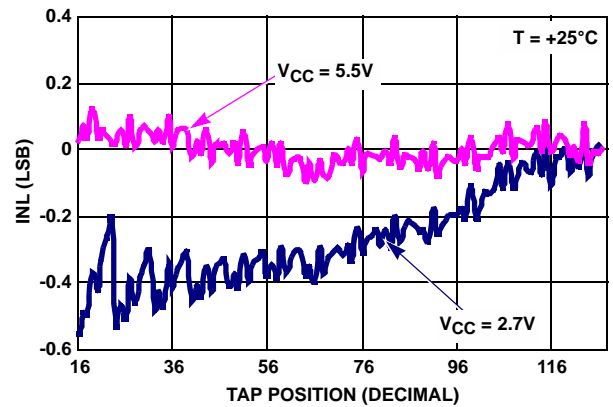


FIGURE 8. INL vs TAP POSITION IN RHEOSTAT MODE FOR 10kΩ (W)



Typical Performance Curves (Continued)

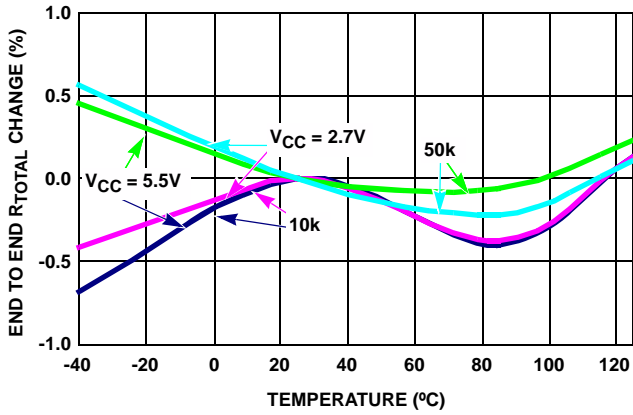


FIGURE 9. END-TO-END R<sub>TOTAL</sub> % CHANGE vs TEMPERATURE

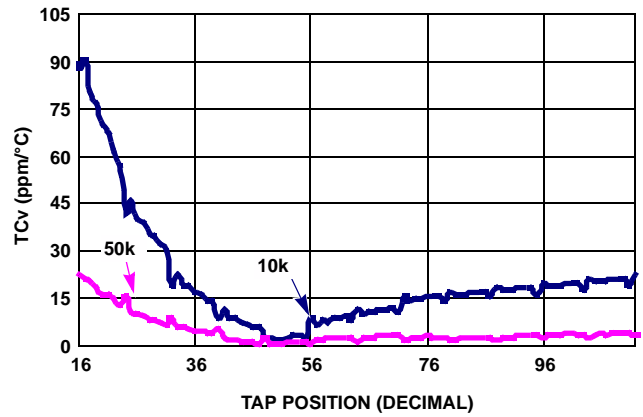


FIGURE 10. TC FOR VOLTAGE DIVIDER MODE IN ppm

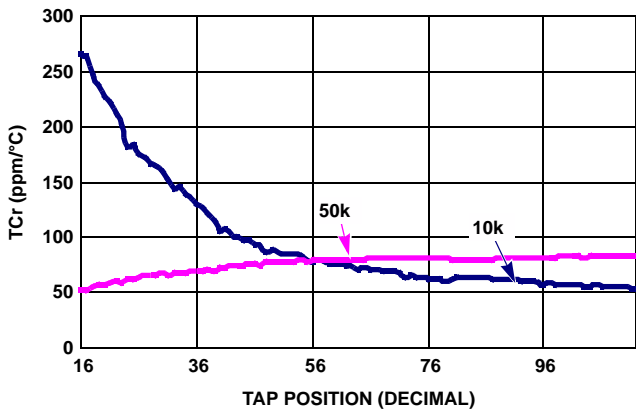


FIGURE 11. TC FOR RHEOSTAT MODE IN ppm

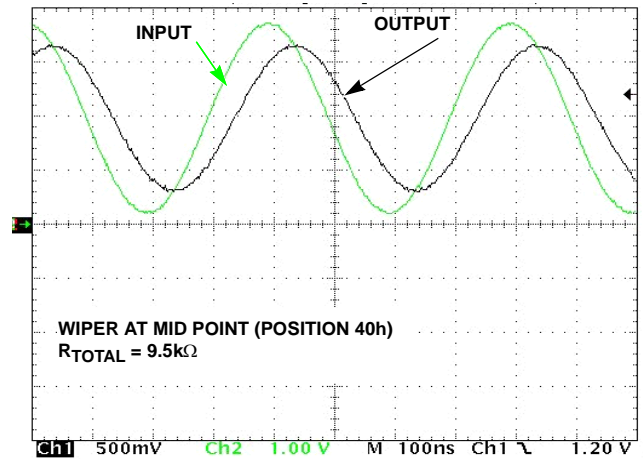


FIGURE 12. FREQUENCY RESPONSE (2.6MHz)

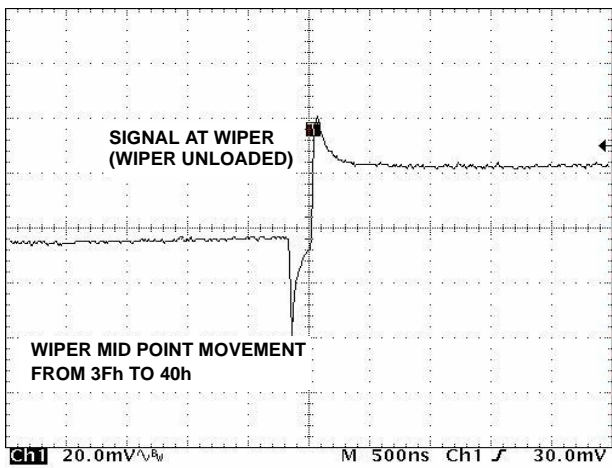


FIGURE 13. MIDSACLE GLITCH, CODE 3Fh TO 40h

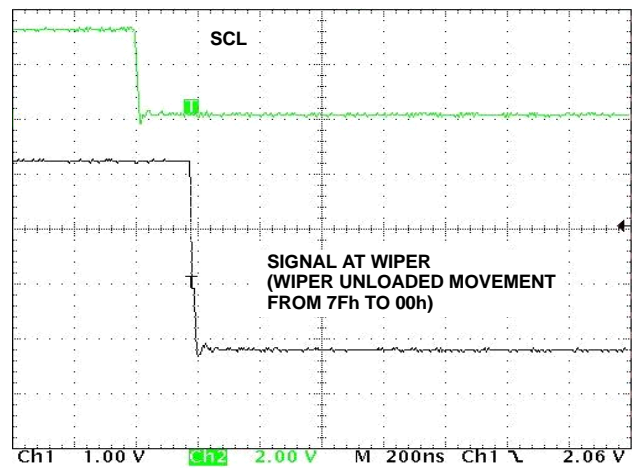


FIGURE 14. LARGE SIGNAL SETTLING TIME

## Pin Description

### Potentiometers Pins

#### RH AND RL

The high (RH) and low (RL) terminals of the ISL22316 are equivalent to the fixed terminals of a mechanical potentiometer. RH and RL are referenced to the relative position of the wiper and not the voltage potential on the terminals. With WR set to 127 decimal, the wiper will be closest to RH, and with the WR set to 0, the wiper is closest to RL.

#### RW

RW is the wiper terminal and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the WR register.

#### SHDN

The  $\overline{\text{SHDN}}$  pin forces the resistor to end-to-end open circuit condition on RH and shorts RW to RL. When  $\overline{\text{SHDN}}$  is returned to logic high, the previous latch settings put RWi at the same resistance setting prior to shutdown. **This pin is logically AND with the SHDN bit in the ACR register.** The I<sup>2</sup>C interface is still available in shutdown mode and all registers are accessible. This pin must remain HIGH for normal operation.

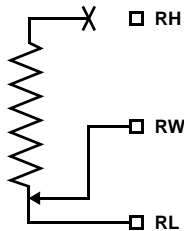


FIGURE 15. DCP CONNECTION IN SHUTDOWN MODE

### Bus Interface Pins

#### SERIAL DATA INPUT/OUTPUT (SDA)

The SDA is a bidirectional serial data input/output pin for I<sup>2</sup>C interface. It receives device address, operation code, wiper address and data from an I<sup>2</sup>C external master device at the rising edge of the serial clock SCL, and it shifts out data after each falling edge of the serial clock.

SDA requires an external pull-up resistor, since it is an open drain input/output.

#### SERIAL CLOCK (SCL)

This input is the serial clock of the I<sup>2</sup>C serial interface. SCL requires an external pull-up resistor, since it is an open drain input.

#### DEVICE ADDRESS (A1, A0)

The address inputs are used to set the least significant 2 bits of the 7-bit I<sup>2</sup>C interface slave address. A match in the slave

address serial data stream must match with the Address input pins in order to initiate communication with the ISL22316. A maximum of four ISL22316 devices may occupy the I<sup>2</sup>C serial bus.

## Principles of Operation

The ISL22316 is an integrated circuit incorporating one DCP with its associated registers, non-volatile memory and an I<sup>2</sup>C serial interface providing direct communication between a host and the potentiometer and memory. The resistor array is comprised of individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The electronic switches on the device operate in a “make before break” mode when the wiper changes tap positions.

When the device is powered down, the last value stored in IVR will be maintained in the non-volatile memory. When power is restored, the contents of the IVR is recalled and loaded into the WR to set the wiper to the initial value.

### DCP Description

The DCP is implemented with a combination of resistor elements and CMOS switches. The physical ends of each DCP are equivalent to the fixed terminals of a mechanical potentiometer (RH and RL pins). The RW pin of the DCP is connected to intermediate nodes, and is equivalent to the wiper terminal of a mechanical potentiometer. The position of the wiper terminal within the DCP is controlled by a 7-bit volatile Wiper Register (WR). When the WR of a DCP contains all zeroes (WR<6:0>: 00h), its wiper terminal (RW) is closest to its “Low” terminal (RL). When the WR register of a DCP contains all ones (WR<6:0>: 7Fh), its wiper terminal (RW) is closest to its “High” terminal (RH). As the value of the WR increases from all zeroes (0) to all ones (127 decimal), the wiper moves monotonically from the position closest to RL to the closest to RH. At the same time, the resistance between RW and RL increases monotonically, while the resistance between RH and RW decreases monotonically.

While the ISL22316 is being powered up, the WR is reset to 40h (64 decimal), which locates RW roughly at the center between RL and RH. After the power supply voltage becomes large enough for reliable non-volatile memory reading, the WR will be reload with the value stored in a non-volatile Initial Value Register (IVR).

The WR and IVR can be read or written to directly using the I<sup>2</sup>C serial interface as described in the following sections.

### Memory Description

The ISL22316 contains one non-volatile 8-bit register, known as the Initial Value Register (IVR), and two volatile 8-bit registers, Wiper Register (WR) and Access Control Register (ACR). Table 1 shows the Memory map of the ISL22316. The

non-volatile register (IVR) at address 0, contain initial wiper position and volatile registers (WR) contain current wiper position.

TABLE 1. MEMORY MAP

| ADDRESS | NON-VOLATILE | VOLATILE |
|---------|--------------|----------|
| 2       | —            | ACR      |
| 1       | Reserved     |          |
| 0       | IVR          | WR       |

The non-volatile IVR and volatile WR registers are accessible with the same address.

The Access Control Register (ACR) contains information and control bits described in Table 2.

The VOL bit (ACR<7>) determines whether the access is to wiper registers WR or initial value registers IVR.

TABLE 2. ACCESS CONTROL REGISTER (ACR)

|     |      |     |   |   |   |   |   |
|-----|------|-----|---|---|---|---|---|
| VOL | SHDN | WIP | 0 | 0 | 0 | 0 | 0 |
|-----|------|-----|---|---|---|---|---|

If VOL bit is 0, the non-volatile IVR register is accessible. If VOL bit is 1, only the volatile WR is accessible. Note, value is written to IVR register also is written to the WR. The default value of this bit is 0.

The SHDN bit (ACR<6>) disables or enables Shutdown mode. This bit is logically AND with SHDN pin. When this bit is 0, DCP is in Shutdown mode. Default value of SHDN bit is 1.

The WIP bit (ACR<5>) is read only bit. It indicates that non-volatile write operation is in progress. It is impossible to write to the WR or ACR while WIP bit is 1.

**Shutdown Mode**

The device can be put in Shutdown mode either by pulling the SHDN pin to GND or setting the SHDN bit in the ACR register to 0. The truth table for Shutdown mode is in Table 3.

TABLE 3.

| SHDN pin | SHDN bit | Mode             |
|----------|----------|------------------|
| High     | 1        | Normal operation |
| Low      | 1        | Shutdown         |
| High     | 0        | Shutdown         |
| Low      | 0        | Shutdown         |

**I<sup>2</sup>C Serial Interface**

The ISL22316 supports an I<sup>2</sup>C bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL22316 operates as a slave device in all applications.

All communication over the I<sup>2</sup>C interface is conducted by sending the MSB of each byte of data first.

**Protocol Conventions**

Data states on the SDA line must change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 16). On power-up of the ISL22316, the SDA pin is in the input mode.

All I<sup>2</sup>C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL22316 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 16). A START condition is ignored during the power-up of the device.

All I<sup>2</sup>C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 16). A STOP condition at the end of a read operation, or at the end of a write operation places the device in its standby mode.

An ACK, Acknowledge, is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (see Figure 17).

The ISL22316 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL22316 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation

A valid Identification Byte contains 01010 as the five MSBs, and the following two bits matching the logic values present at pins A1 and A0. The LSB is the Read/Write bit. Its value is "1" for a Read operation, and "0" for a Write operation (see Table 4).

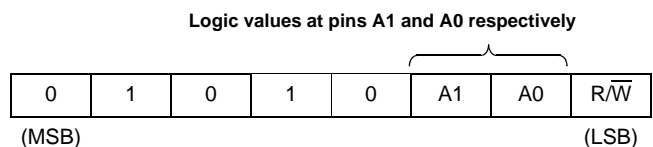


TABLE 4. IDENTIFICATION BYTE FORMAT

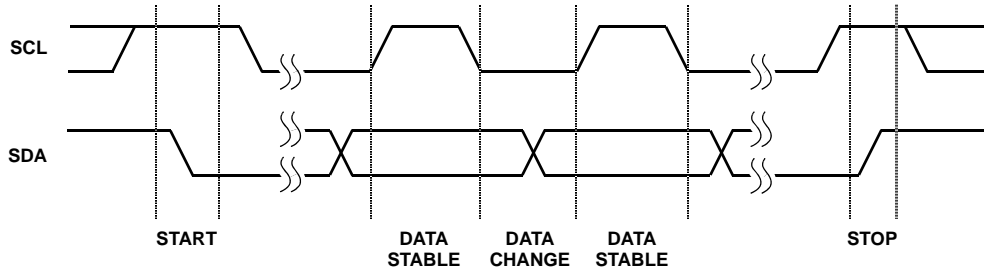


FIGURE 16. VALID DATA CHANGES, START AND STOP CONDITIONS

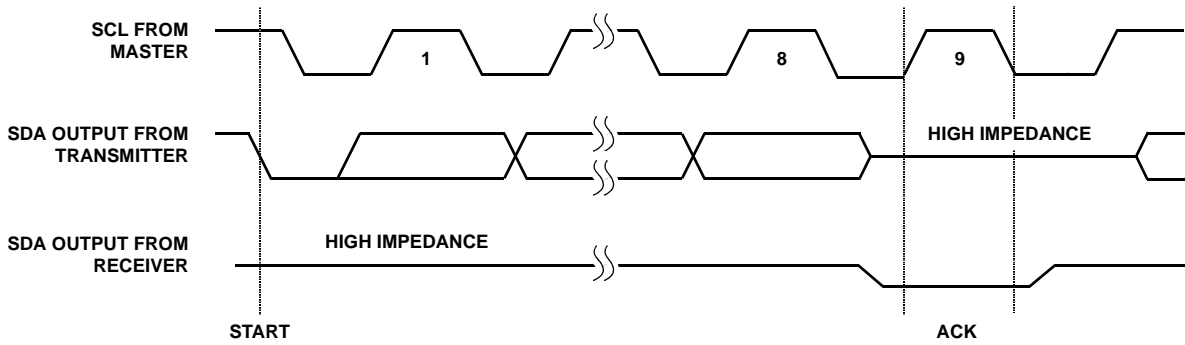


FIGURE 17. ACKNOWLEDGE RESPONSE FROM RECEIVER

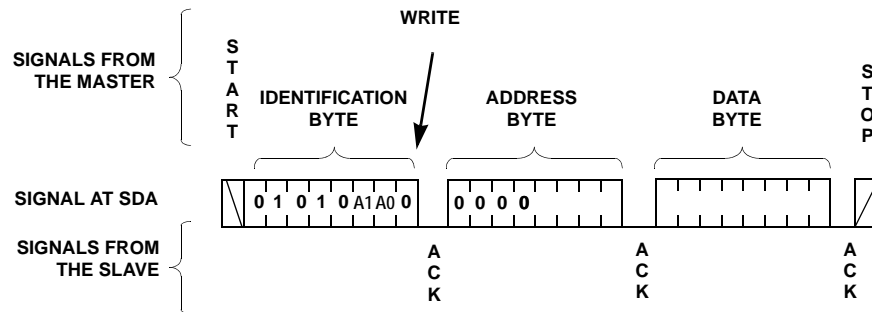


FIGURE 18. BYTE WRITE SEQUENCE

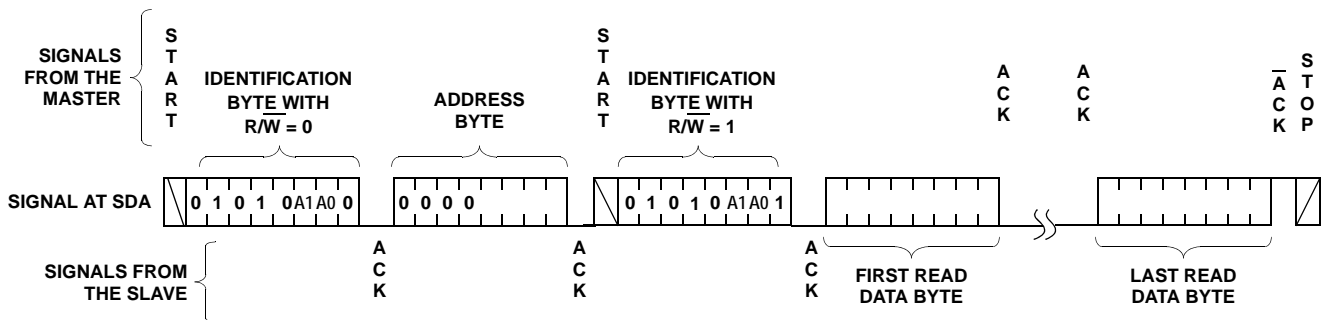


FIGURE 19. READ SEQUENCE

## **Write Operation**

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL22316 responds with an ACK. At this time, the device enters its standby state (see Figure 18).

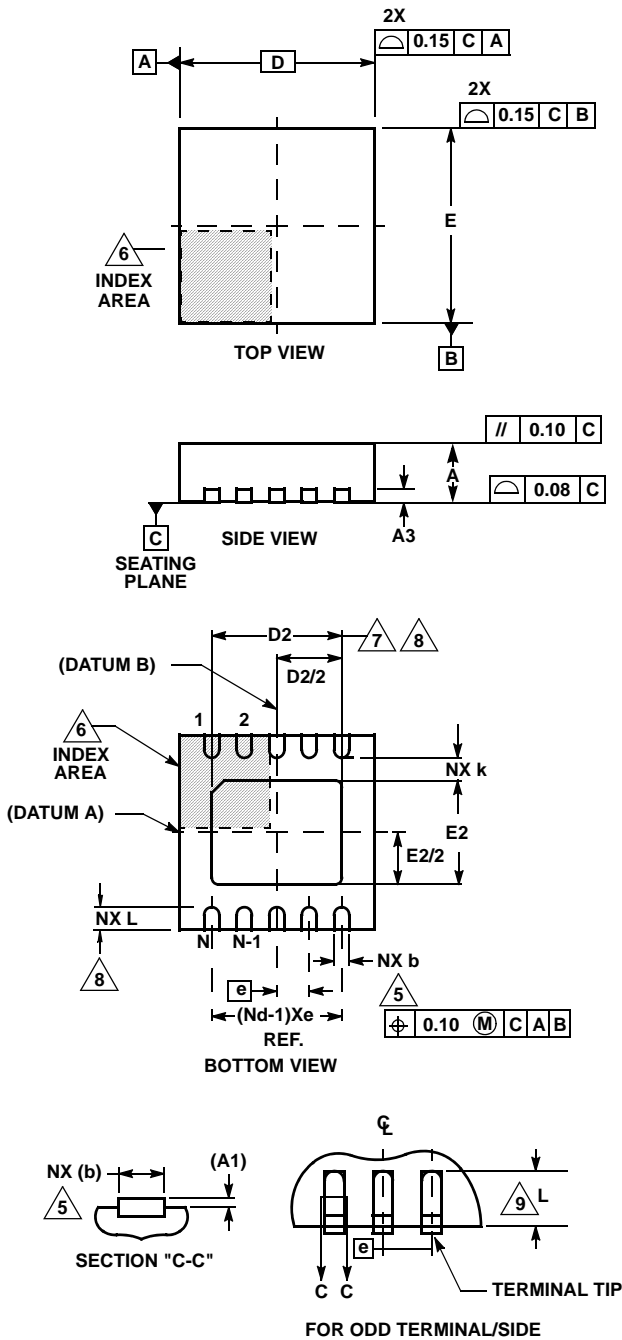
The non-volatile write cycle starts after STOP condition is determined and it requires up to 20ms delay for the next non-volatile write.

## **Read Operation**

A Read operation consists of a three byte instruction followed by one or more Data Bytes (See Figure 19). The master initiates the operation issuing the following sequence: a START, the Identification byte with the  $\overline{R/W}$  bit set to "0", an Address Byte, a second START, and a second Identification byte with the  $\overline{R/W}$  bit set to "1". After each of the three bytes, the ISL22316 responds with an ACK. Then the ISL22316 transmits Data Bytes as long as the master responds with an ACK during the SCL cycle following the eighth bit of each byte. The master terminates the read operation (issuing a  $\overline{ACK}$  and STOP condition) following the last bit of the last Data Byte (see Figure 19).

In order to read back the non-volatile IVR, it is recommended that the application reads the ACR first to verify the WIP bit is 0. If the WIP bit (ACR[5]) is not 0, the host should repeat its reading sequence again.

Thin Dual Flat No-Lead Plastic Package (TDFN)



L10.3x3B

10 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE

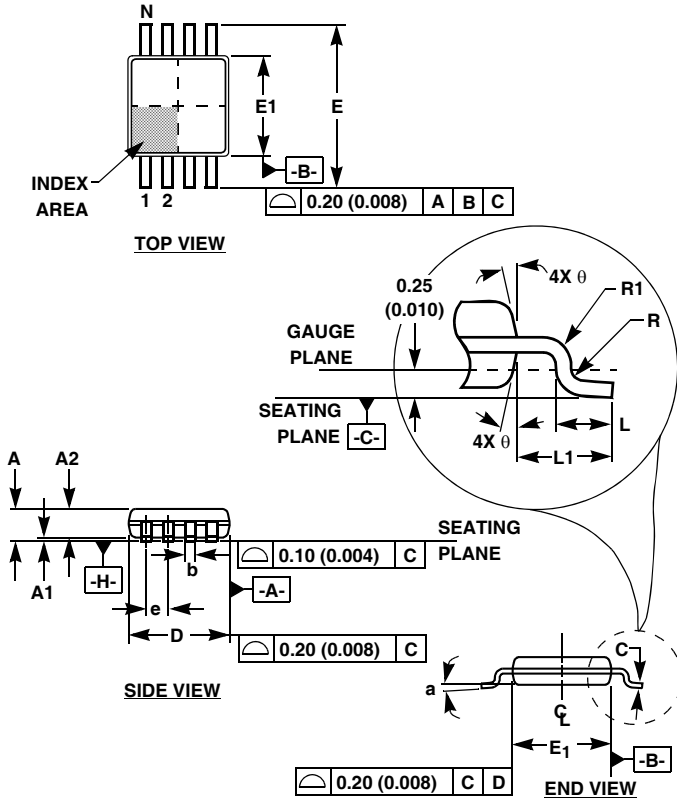
| SYMBOL | MILLIMETERS |         |      | NOTES |
|--------|-------------|---------|------|-------|
|        | MIN         | NOMINAL | MAX  |       |
| A      | 0.70        | 0.75    | 0.80 | -     |
| A1     | -           | -       | 0.05 | -     |
| A3     | 0.20 REF    |         |      | -     |
| b      | 0.18        | 0.25    | 0.30 | 5, 8  |
| D      | 3.00 BSC    |         |      | -     |
| D2     | 2.23        | 2.38    | 2.48 | 7, 8  |
| E      | 3.00 BSC    |         |      | -     |
| E2     | 1.49        | 1.64    | 1.74 | 7, 8  |
| e      | 0.50 BSC    |         |      | -     |
| k      | 0.20        | -       | -    | -     |
| L      | 0.30        | 0.40    | 0.50 | 8     |
| N      | 10          |         |      | 2     |
| Nd     | 5           |         |      | 3     |

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NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. COMPLIANT TO JEDEC MO-229-WEED-3 except for dimensions E2 & D2.

Mini Small Outline Plastic Packages (MSOP)



M10.118 (JEDEC MO-187BA)  
10 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

| SYMBOL | INCHES    |       | MILLIMETERS |      | NOTES |
|--------|-----------|-------|-------------|------|-------|
|        | MIN       | MAX   | MIN         | MAX  |       |
| A      | 0.037     | 0.043 | 0.94        | 1.10 | -     |
| A1     | 0.002     | 0.006 | 0.05        | 0.15 | -     |
| A2     | 0.030     | 0.037 | 0.75        | 0.95 | -     |
| b      | 0.007     | 0.011 | 0.18        | 0.27 | 9     |
| c      | 0.004     | 0.008 | 0.09        | 0.20 | -     |
| D      | 0.116     | 0.120 | 2.95        | 3.05 | 3     |
| E1     | 0.116     | 0.120 | 2.95        | 3.05 | 4     |
| e      | 0.020 BSC |       | 0.50 BSC    |      | -     |
| E      | 0.187     | 0.199 | 4.75        | 5.05 | -     |
| L      | 0.016     | 0.028 | 0.40        | 0.70 | 6     |
| L1     | 0.037 REF |       | 0.95 REF    |      | -     |
| N      | 10        |       | 10          |      | 7     |
| R      | 0.003     | -     | 0.07        | -    | -     |
| R1     | 0.003     | -     | 0.07        | -    | -     |
| θ      | 5°        | 15°   | 5°          | 15°  | -     |
| α      | 0°        | 6°    | 0°          | 6°   | -     |

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NOTES:

- These package dimensions are within allowable dimensions of JEDEC MO-187BA.
- Dimensioning and tolerancing per ANSI Y14.5M-1994.
- Dimension "D" does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
- Dimension "E1" does not include interlead flash or protrusions and are measured at Datum Plane. [-H-] Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
- Formed leads shall be planar with respect to one another within 0.10mm (.004) at seating Plane.
- "L" is the length of terminal for soldering to a substrate.
- "N" is the number of terminal positions.
- Terminal numbers are shown for reference only.
- Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of "b" dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
- Datums [-A-] and [-B-] to be determined at Datum plane [-H-].
- Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only

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