Section 14 Electrical Characteristics

14.1 Absolute Maximum Ratings

Table 14-1 lists the absolute maximum ratings.

Table 14-1 Absolute Maximum Ratings

Item		Symbol	Value	Unit	Notes
Power supply voltage		V_{CC}	–0.3 to +7.0	V	1
Analog power supply voltage		AV_{CC}	–0.3 to +7.0	V	1
		AV_{ref}	–0.3 to AV_{CC} +0.3	V	1
Reference level supply voltage		VT_{ref}	–0.3 to V_{CC} +0.3	V	1
Programming voltage		V_{PP}	–0.3 to +13.0	V	1
Input voltage	Ports other than port B	V_{in}	–0.3 to V_{CC} +0.3	V	1
	Port B	AV_{in}	–0.3 to AV_{CC} +0.3	V	1
Operating temperature		T_{opr}	0 to 75	Åé	1
Storage temperature		T_{stg}	–55 to +125	Åé	1

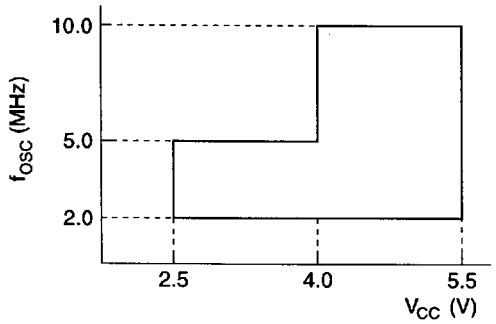
Note: 1. Permanent damage may occur to the chip if maximum ratings are exceeded. Normal operation should be under the conditions specified in Electrical Characteristics. Exceeding these values can result in incorrect operation and reduced reliability.

14.2 Electrical Characteristics

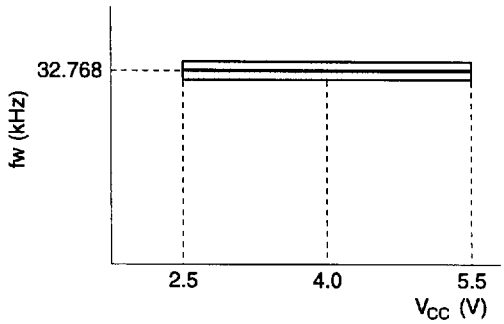
14.2.1 Power Supply Voltage and Operating Range

The power supply voltage and operating range are indicated by the shaded region in the figures below.

1. Power supply voltage vs. oscillator frequency range

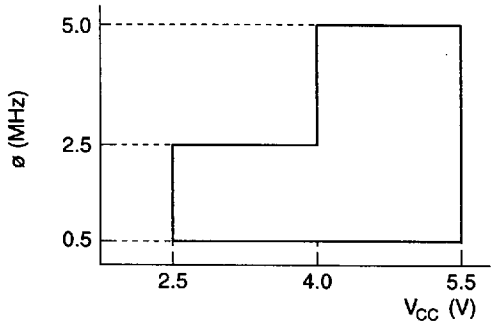


• Active mode (high and medium speeds)
• Sleep mode

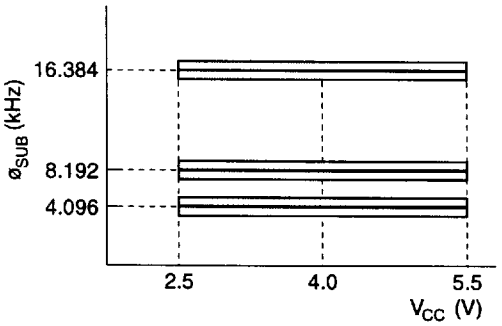


• All operating modes

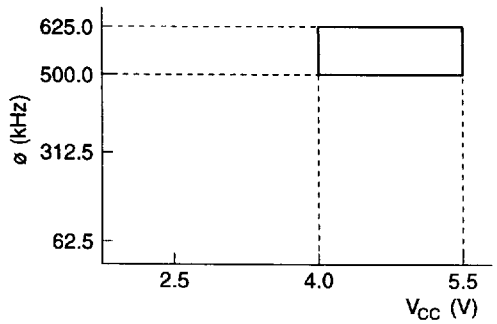
2. Power supply voltage vs. clock frequency range



• Active mode (high speed)
• Sleep mode (except CPU)

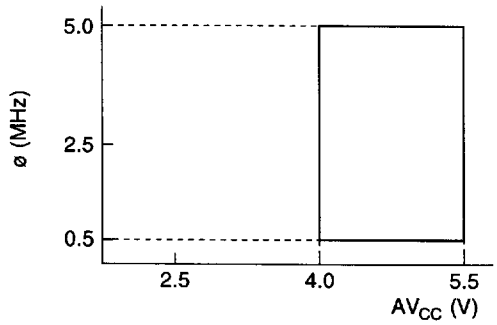


• Subactive mode
• Subsleep mode (except CPU)
• Watch mode (except CPU)

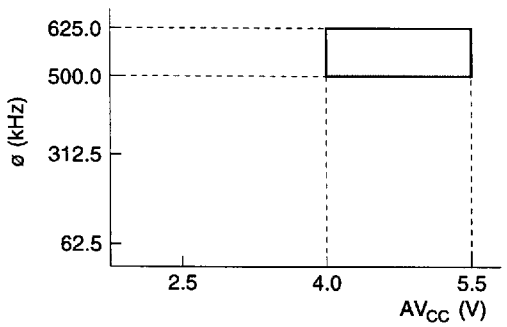


• Active mode (medium speed)

3. Analog power supply voltage vs. A/D converter operating range



• Active (high speed) mode
• Sleep mode



• Active (medium speed) mode

14.2.2 DC Characteristics

Table 14-2 lists the DC characteristics.

Table 14-2 DC Characteristics

V_{CC} = 2.5 V to 5.5 V, AV_{CC} = 2.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = 0 to +75°C, including subactive mode, unless otherwise indicated.

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	$\overline{RES}$, $\overline{NMI}$, $\overline{WKP_0}$ to $\overline{WKP_7}$, $\overline{IRQ_0}$ to $\overline{IRQ_4}$, TMIF, TMIG, SCK_1, SCK_3, $\overline{ADTRG}$	0.8 V_{CC}	—	V_{CC} +0.3	V	V_{CC} = 4.0 V to 5.5 V	
			0.9 V_{CC}	—	V_{CC} +0.3			
		SI_1, RXD	0.7 V_{CC}	—	V_{CC} +0.3	V	V_{CC} = 4.0 V to 5.5 V	
			0.8 V_{CC}	—	V_{CC} +0.3			
		OSC_1	V_{CC} –0.5	—	V_{CC} +0.3	V	V_{CC} = 4.0 V to 5.5 V	
			V_{CC} –0.3	—	V_{CC} +0.3			
		$P1_0$ to $P1_7$ $P2_0$ to $P2_7$ $P5_0$ to $P5_7$ $P6_0$ to $P6_7$ $P7_0$ to $P7_7$	0.7 V_{CC}	—	V_{CC} +0.3	V	V_{CC} = 4.0 V to 5.5 V	
		$P8_0$ to $P8_7$ $P9_0$ to $P9_7$ PA_0 to PA_3 PD_0 to PD_7 PE_0 to PE_3	0.8 V_{CC}	—	V_{CC} +0.3			
		PB_0 to PB_7	0.7 V_{CC}	—	AV_{CC} +0.3	V	V_{CC} = 4.0 V to 5.5 V	
			0.8 V_{CC}	—	AV_{CC} +0.3			
Input low voltage	V_{IL}	$\overline{RES}$, $\overline{NMI}$, $\overline{WKP_0}$ to $\overline{WKP_7}$, $\overline{IRQ_0}$ to $\overline{IRQ_4}$, TMIF, TMIG, SCK_1, SCK_3, $\overline{ADTRG}$	–0.3	—	0.2 V_{CC}	V	V_{CC} = 4.0 V to 5.5 V	
			–0.3	—	0.1 V_{CC}			
		SI_1, RXD	–0.3	—	0.3 V_{CC}	V	V_{CC} = 4.0 V to 5.5 V	
			–0.3	—	0.2 V_{CC}			
		OSC_1	–0.3	—	0.5	V	V_{CC} = 4.0 V to 5.5 V	
			–0.3	—	0.3			

Note: Connect pin TEST to V_{SS}.

Table 14-2 DC Characteristics (cont)

V_{CC} = 2.5 V to 5.5 V, AV_{CC} = 2.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = 0 to +75°C, including subactive mode, unless otherwise indicated.

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Test Condition	Note
Input low voltage	V_{IL}	$P1_0$ to $P1_7$ $P2_0$ to $P2_7$ $P5_0$ to $P5_7$ $P6_0$ to $P6_7$ $P7_0$ to $P7_7$ $P8_0$ to $P8_7$	–0.3	—	0.3 V_{CC}	V	V_{CC} = 4.0 V to 5.5 V	
		$P9_0$ to $P9_7$ PA_0 to PA_3 PB_0 to PB_7 PD_0 to PD_7 PE_0 to PE_3	–0.3	—	0.2 V_{CC}			
Output high voltage	V_{OH}	$P1_0$ to $P1_7$ $P2_0$ to $P2_7$ $P5_0$ to $P5_7$	V_{CC} – 1.0	—	—	V	V_{CC} = 4.0 V to 5.5 V $-I_{OH}$ = 1.0 mA	
		$P6_0$ to $P6_7$ $P7_0$ to $P7_7$ $P8_0$ to $P8_7$	V_{CC} – 0.5	—	—		V_{CC} = 4.0 V to 5.5 V $-I_{OH}$ = 0.5 mA	
		$P9_0$ to $P9_7$ PA_0 to PA_3 PD_0 to PD_7 PE_0 to PE_3	V_{CC} – 0.5	—	—		$-I_{OH}$ = 0.1 mA	
Output low voltage	V_{OL}	$P5_0$ to $P5_7$ $P6_0$ to $P6_7$ $P7_0$ to $P7_7$ $P8_0$ to $P8_7$ $P9_0$ to $P9_7$ PA_0 to PA_3 PD_0 to PD_7 PE_0 to PE_3	—	—	0.5		I_{OL} = 0.4 mA	
		$P1_0$ to $P1_7$ $P2_0$ to $P2_7$	—	—	1.5		V_{CC} = 4.0 V to 5.5 V I_{OL} = 10 mA	
			—	—	0.6		V_{CC} = 4.0 V to 5.5 V I_{OL} = 1.6 mA	
			—	—	0.5		I_{OL} = 0.4 mA	

Note: Connect pin TEST to V_{SS}.

Table 14-2 DC Characteristics (cont)

V_{CC} = 2.5 V to 5.5 V, AV_{CC} = 2.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = 0 to +75°C, including subactive mode, unless otherwise indicated.

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Test Condition	Note
Input leakage current	$\|I_{IL}\|$	$\overline{RES}$, $\overline{NMI}$	—	—	20	µA	V_{IN} = 0.5 V to V_{CC} – 0.5 V	3
			—	—	1			2
		OSC_1 $P1_0$ to $P1_7$ $P2_0$ to $P2_7$ $P5_0$ to $P5_7$ $P6_0$ to $P6_7$ $P7_0$ to $P7_7$ $P8_0$ to $P8_7$ $P9_0$ to $P9_7$ PA_0 to PA_3 PD_0 to PD_7 PE_0 to PE_3	—	—	1	µA	V_{IN} = 0.5 V to V_{CC} – 0.5 V	
		PB_0 to PB_7	—	—	1		V_{IN} = 0.5 V to AV_{CC} – 0.5 V	
Pull-up MOS current	$-I_P$	$P1_0$ to $P1_7$ $P2_0$ to $P2_7$	50	—	300	µA	V_{CC} = 5 V, V_{IN} = 0 V	
		$P5_0$ to $P5_7$ $P6_0$ to $P6_7$	—	35	—	µA	V_{CC} = 2.7 V, V_{IN} = 0 V	Reference value
Input capacitance	C_{IN}	All input pins except power supply pins	—	—	15	pF	f = 1 MHz, V_{IN} = 0 V, T_a = 25°C	
		$\overline{RES}$	—	—	60			3
		$\overline{NMI}$	—	—	30			

Notes: 2. Applies to HD6433875N, HD6433876N, and HD6433877N.
3. Applies to HD6473877N.

Table 14-2 DC Characteristics (cont)

V_{CC} = 2.5 V to 5.5 V, AV_{CC} = 2.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = 0 to +75°C, including subactive mode, unless otherwise indicated.

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Test Condition	Notes
Active mode current dissipation	I_{OPE1}	V_{CC}	—	12	24	mA	Active mode (high speed), V_{CC} = 5 V, f_{osc} = 10 MHz	4, 5
	I_{OPE2}	V_{CC}	—	2.5	5	mA	Active mode (medium speed), V_{CC} = 5 V, f_{osc} = 10 MHz	4, 5
Sleep mode current dissipation	I_{SLEEP}	V_{CC}	—	5	10	mA	V_{CC} = 5 V, f_{osc} = 10 MHz	4, 5
Subactive mode current dissipation	I_{SUB}	V_{CC}	—	50	130	µA	V_{CC} = 2.5 V, 32-kHz crystal oscillator ($ø_{SUB}$ = ø w/2)	4, 5
			—	40	—	µA	V_{CC} = 2.5 V, 32-kHz crystal oscillator ($ø_{SUB}$ = ø w/8)	Reference value 4, 5
Subsleep mode current dissipation	I_{SUBSP}	V_{CC}	—	40	90	µA	V_{CC} = 2.5 V, 32-kHz crystal oscillator ($ø_{SUB}$ = ø w/2)	4, 5
Watch mode current dissipation	I_{WATCH}	V_{CC}	—	—	6	µA	V_{CC} = 2.7 V, 32-kHz crystal oscillator	4, 5
Standby mode current dissipation	I_{STBY}	V_{CC}	—	—	5	µA	32-kHz crystal oscillator not used	4, 5
RAM data retaining voltage	V_{RAM}	V_{CC}	2	—	—	V		

Notes: 4. Pin states during current measurement are shown below.

Mode	Other Pins	Internal State	Oscillator Pins
Active mode (high and medium speed)	V_{CC}	Operates	System clock oscillator: Crystal Subclock oscillator: Pin X_1 = V_{CC}
Sleep mode	V_{CC}	Only timer operates$_C$	
Subactive mode	V_{CC}	Operates	System clock oscillator: Crystal Subclock oscillator: Crystal
Subsleep mode	V_{CC}	Only timer operates, CPU stops	
Watch mode	V_{CC}	Only time-base clock$_C$ operates, CPU stops	
Standby mode	V_{CC}	CPU and timers all stop	System clock oscillator: Crystal Subclock oscillator: Pin X_1 = V_{CC}

Notes: 5. Excludes current in pull-up MOS transistors and output buffers.

Table 14-2 DC Characteristics (cont)

V_{CC} = 2.5 V to 5.5 V, AV_{CC} = 2.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = 0 to +75°C, including subactive mode, unless otherwise indicated.

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Test Condition
Allowable output low current (per pin)	I_{OL}	Output pins except in ports 1 and 2	—	—	2	mA	V_{CC} = 4.0 V to 5.5 V
		Ports 1 and 2	—	—	10		V_{CC} = 4.0 V to 5.5 V
		All output pins	—	—	0.5		
Allowable output low current (total)	ΣI_{OL}	Output pins except in ports 1 and 2	—	—	40	mA	V_{CC} = 4.0 V to 5.5 V
		Ports 1 and 2	—	—	80		V_{CC} = 4.0 V to 5.5 V
		All output pins	—	—	20		
Allowable output high current (per pin)	$-I_{OH}$	All output pins	—	—	2	mA	V_{CC} = 4.0 V to 5.5 V
			—	—	0.2		
Allowable output high current (total)	$\Sigma-I_{OH}$	All output pins	—	—	15	mA	V_{CC} = 4.0 V to 5.5 V
			—	—	10		

14.2.3 AC Characteristics

Table 14-3 lists the control signal timing, and tables 14-4 and 14-5 list the serial interface timing.

Table 14-3 Control Signal Timing

V_{CC} = 2.5 V to 5.5 V, AV_{CC} = 2.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = 0 to +75°C, including subactive mode, unless otherwise specified.

Item	Symbol	Applicable Pins	Min	Typ	Max	Units	Test Condition	Note
System clock oscillation frequency	f_{OSC}	OSC_1, OSC_2	2	—	10	MHz	V_{CC} = 4.0 V to 5.5 V	
			2	—	5			
OSC clock ($ø_{OSC}$) cycle time	t_{OSC}	OSC_1, OSC_2	100	—	1000	ns	V_{CC} = 4.0 V to 5.5 V	1
			200	—	1000			Figure 14-3
System clock (ø) cycle time	t_{cyc}		2	—	16	t_{OSC}		1
			—	—	2000	ns		
Subclock oscillation frequency	f_W	X_1, X_2	—	32.768	—	kHz		
Watch clock cycle time ($ø_W$)	t_W	X_1, X_2	—	30.5	—	µs		
Subclock ($ø_{SUB}$) cycle time	t_{subcyc}		2	—	8	t_W		2
Instruction cycle time			2	—	—	t_{cyc} t_{subcyc}		
Oscillation stabilization time (crystal oscillator)	t_{rc}	OSC_1, OSC_2	—	—	40	ms	V_{CC} = 4.0 V to 5.5 V	
			—	—	60			
Oscillation stabilization time	t_{rc}	X_1, X_2	—	—	2	s		
External clock high width	t_{CPH}	OSC_1	40	—	—	ns	V_{CC} = 4.0 V to 5.5 V	Figure 14-3
			80	—	—			
External clock low width	t_{CPL}	OSC_1	40	—	—	ns	V_{CC} = 4.0 V to 5.5 V	Figure 14-3
			80	—	—			
External clock rise time	t_{CPr}		—	—	15	ns	V_{CC} = 4.0 V to 5.5 V	
			—	—	20			
External clock fall time	t_{CPf}		—	—	15	ns	V_{CC} = 4.0 V to 5.5 V	
			—	—	20			
Pin $\overline{RES}$ low width	t_{REL}	$\overline{RES}$	10	—	—	tcyc		Figure 14-4

Notes: 1. A frequency between 1 MHz to 10 MHz is required when an external clock is input.
2. Selected with SA1 and SA0 of system clock control register 2 (SYSCR2).

Table 14-3 Control Signal Timing (cont)

V_{CC} = 2.5 V to 5.5 V, AV_{CC} = 2.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = 0 to +75°C, including subactive mode, unless otherwise specified.

Item	Symbol	Applicable Pins	Min	Typ	Max	Units	Test Condition	Reference Figure
Input pin high width	t_{IH}	$\overline{NMI}$, $\overline{IRQ_0}$ to $\overline{IRQ_4}$, $\overline{WKP_0}$ to $\overline{WKP_7}$, $\overline{ADTRG}$, TMIF, TMIG	2	—	—	t_{cyc} t_{subcyc}		Figure 14-5
Input pin low width	t_{IL}	$\overline{NMI}$, $\overline{IRQ_0}$ to $\overline{IRQ_4}$, $\overline{WKP_0}$ to $\overline{WKP_7}$, $\overline{ADTRG}$, TMIF, TMIG	2	—	—	t_{cyc} t_{subcyc}		Figure 14-5

Table 14-4 Serial Interface Timing (SCI1)

V_{CC} = 2.5 V to 5.5 V, AV_{CC} = 2.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = 0 to +75°C, unless otherwise specified.

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Test Condition	Reference Figure
Input serial clock cycle time	t_{scyc}	SCK_1	2	—	—	t_{cyc}		Figure 14-6
Input serial clock high width	t_{SCKH}	SCK_1	0.4	—	—	t_{scyc}		Figure 14-6
Input serial clock low width	t_{SCKL}	SCK_1	0.4	—	—	t_{scyc}		Figure 14-6
Input serial clock rise time	t_{SCKr}	SCK_1	—	—	60	ns	V_{CC} = 4.0 V to 5.5 V	Figure 14-6
			—	—	80			
Input serial clock fall time	t_{SCKf}	SCK_1	—	—	60	ns	V_{CC} = 4.0 V to 5.5 V	Figure 14-6
			—	—	80			
Serial output data delay time	t_{SOD}	SO_1	—	—	200	ns	V_{CC} = 4.0 V to 5.5 V	Figure 14-6
			—	—	350			
Serial input data setup time	t_{SIS}	SI_1	200	—	—	ns	V_{CC} = 4.0 V to 5.5 V	Figure 14-6
			400	—	—			
Serial input data hold time	t_{SIH}	SI_1	200	—	—	ns	V_{CC} = 4.0 V to 5.5 V	Figure 14-6
			400	—	—			

Table 14-5 Serial Interface Timing (SCI3)

V_{CC} = 2.5 V to 5.5 V, AV_{CC} = 2.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = 0 to +75°C, unless otherwise specified.

Item		Symbol	Min	Typ	Max	Unit	Test Condition	Reference Figure
Input clock cycle	Asynchronous	t_{scyc}	4	—	—	t_{cyc}		Figure 14-7
	Synchronous		6	—	—			
Input clock pulse width		t_{SCKW}	0.4	—	0.6	t_{scyc}		Figure 14-7
Transmit data delay time (synchronous mode)		t_{TXD}	—	—	1	t_{cyc}	V_{CC} = 4.0 V to 5.5 V	Figure 14-8
			—	—	1			
Receive data setup time (synchronous mode)		t_{RXS}	200	—	—	ns	V_{CC} = 4.0 V to 5.5 V	Figure 14-8
			400	—	—			
Receive data hold time (synchronous mode)		t_{RXH}	200	—	—	ns	V_{CC} = 4.0 V to 5.5 V	Figure 14-8
			400	—	—			

14.2.4 A/D Converter Characteristics

Table 14-6 shows the A/D converter characteristics.

Table 14-6 A/D Converter Characteristics

$AV_{CC} = V_{CC} = 4.0$ V to 5.5 V, $AV_{SS} = V_{SS} = 0.0$ V, $T_a = 0$ to +75°C, unless otherwise specified.

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Test Condition	Note
Analog power supply voltage	AV_{CC}	AV_{CC}	4.0	—	5.5	V		1
	AV_{ref}	AV_{ref}	2.5	—	AV_{CC} + 0.3	V		
Analog input voltage	AV_{IN}	AN_0 to AN_7	–0.3	—	AV_{CC} + 0.3	V		
Analog power supply current	AI_{OPE}	AV_{CC}, AV_{ref}	—	—	1.5	mA	AV_{CC} = 5.0 V	4
	AI_{STOP1}	AV_{CC}, AV_{ref}	—	150	—	µA		2, 4 Reference value
	AI_{STOP2}	AV_{CC}, AV_{ref}	—	—	5	µA		3, 4
Analog input capacitance	C_{AIN}	AN_0 to AN_7	—	—	30	pF		
Allowable signal source impedance	R_{AIN}		—	—	10	kΩ		
Resolution (data length)			—	—	8	bit		
Non-linearity error			—	—	±2.0	LSB		
Quantization error			—	—	±0.5	LSB		
Absolute accuracy			—	—	±2.5	LSB	AV_{ref} = 4.0 V to 5.5 V	
			—	—	±4.0	LSB	AV_{ref} = 2.5 V to 5.5 V	
Conversion time			12.4	—	248	µs	AV_{CC} = 4.5 V to 5.5 V	
			24.8	—	248	µs	AV_{CC} = 4.0 V to 5.5 V	

Notes: 1. Set $AV_{CC} = V_{CC}$ when the A/D converter is not used.
2. AI_{STOP1} is the current in active and sleep modes while the A/D converter is idle.
3. AI_{STOP2} is the current at reset and in standby, watch, subactive, and subsleep modes while the A/D converter is idle.
4. Indicates the current when AV_{CC} and AV_{REF} are common pins.

14.2.5 DTMF and Multitone Generator Characteristics

Table 14-7 lists the DTMF generator and multitone generator characteristics.

Table 14-7 DTMF Characteristics

V_{CC} = 2.5 V to 5.5 V, AV_{CC} = 2.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = 0 to +75°C, unless otherwise specified

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Test Condition	Note
Reference level supply voltage	VT_{ref}	VT_{ref}	3.0	—	V_{CC} + 0.3	V		
DTMF output voltage (row)	V_{OR}	TONED	750	990	—	mVrms	VT_{ref} – GND = 2.5 V R_L = 100 kΩ	Figure 14-1 1
DTMF output voltage (column)	V_{OC}	TONED	780	1040	—	mVrms	VT_{ref} – GND = 2.5 V R_L = 100 kΩ	Figure 14-1 1
DTMF output distortion	%DISDT	TONED	—	3	7	%	VT_{ref} – GND = 2.5 V R_L = 100 kΩ	Figure 14-1
DTMF output level	dB_{CR}	TONED	—	2.5	—	dB	VT_{ref} – GND = 2.5 V R_L = 100 kΩ	Figure 14-1

Notes: 1. Vor and Voc indicate the output voltage during single wave output.

Table 14-8 Multitone Generator Characteristics

V_{CC} = 3.0 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = 0 to +75°C, unless otherwise specified

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Test Condition	Note
Reference level supply voltage	VT_{ref}	VT_{ref}	3.0	—	V_{CC} + 0.3	V		
MTG output voltage	V_{OMT}	TONEM	720	960	—	mVrms	VT_{ref} – GND = 3.0 V R_L = 100 kΩ Sine wave output	Figure 14-2 2
MTG output distortion	%DISMT	TONEM	—	1	3	%	VT_{ref} – GND = 3.0 V R_L = 100 kΩ Sine wave output	Figure 14-2 2

Note:2. TONEM output is voltage-driven, so avoid high-current loads.

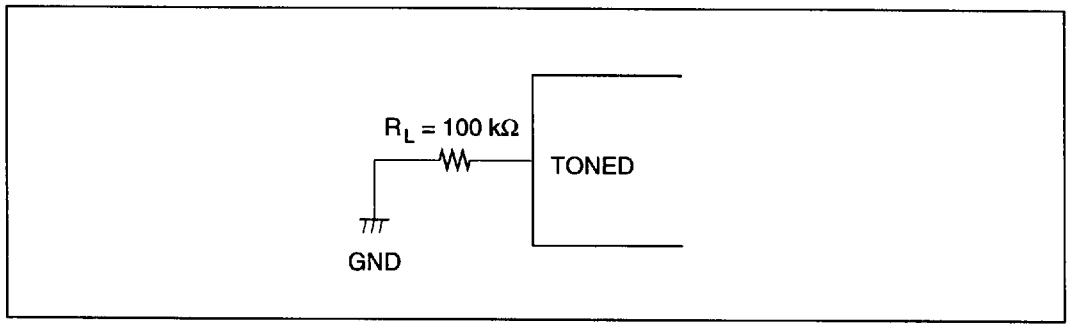


Figure 14-1 TONED Load Circuit

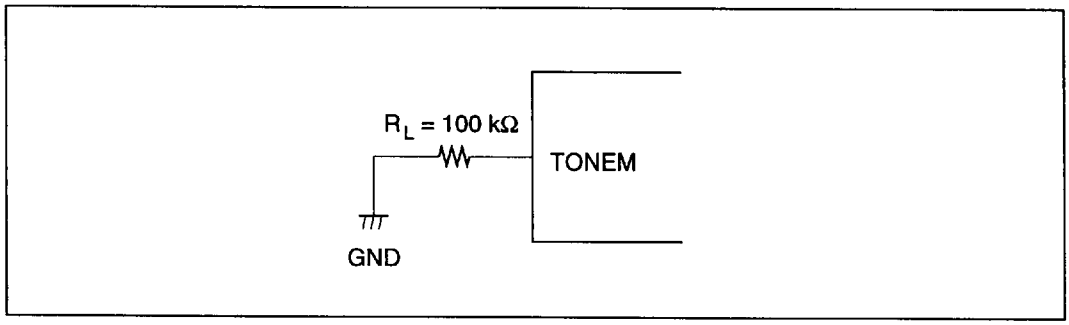


Figure 14-2 TONEM Load Circuit

14.3 Operation Timing

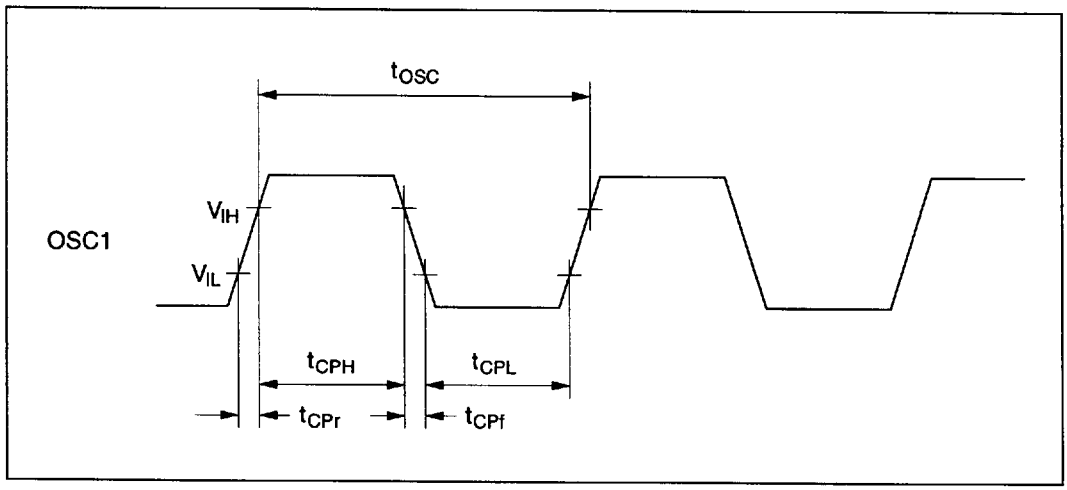


Figure 14-3 System Clock Input Timing

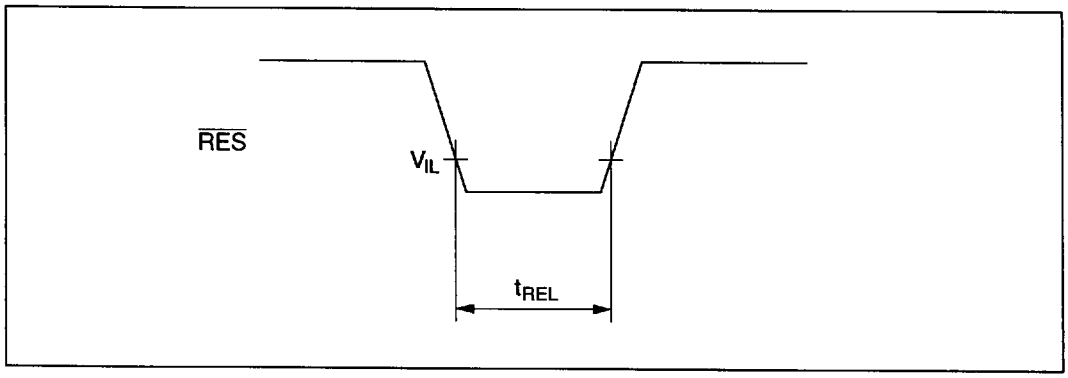


Figure 14-4 $\overline{\text{RES}}$ Low Width Timing

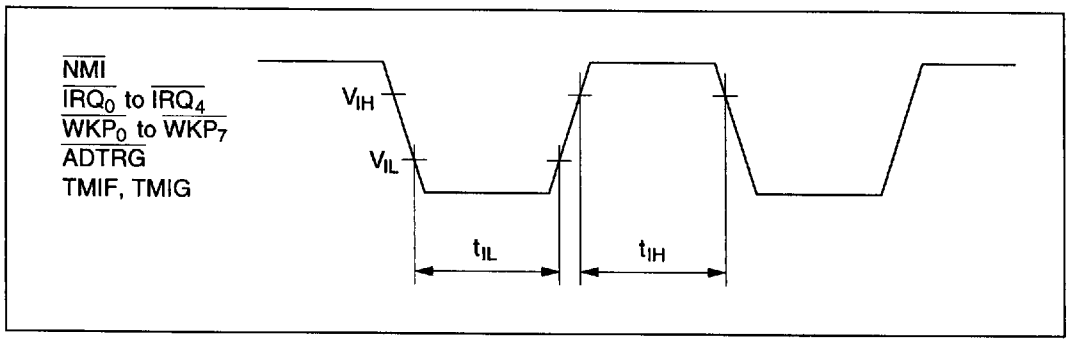
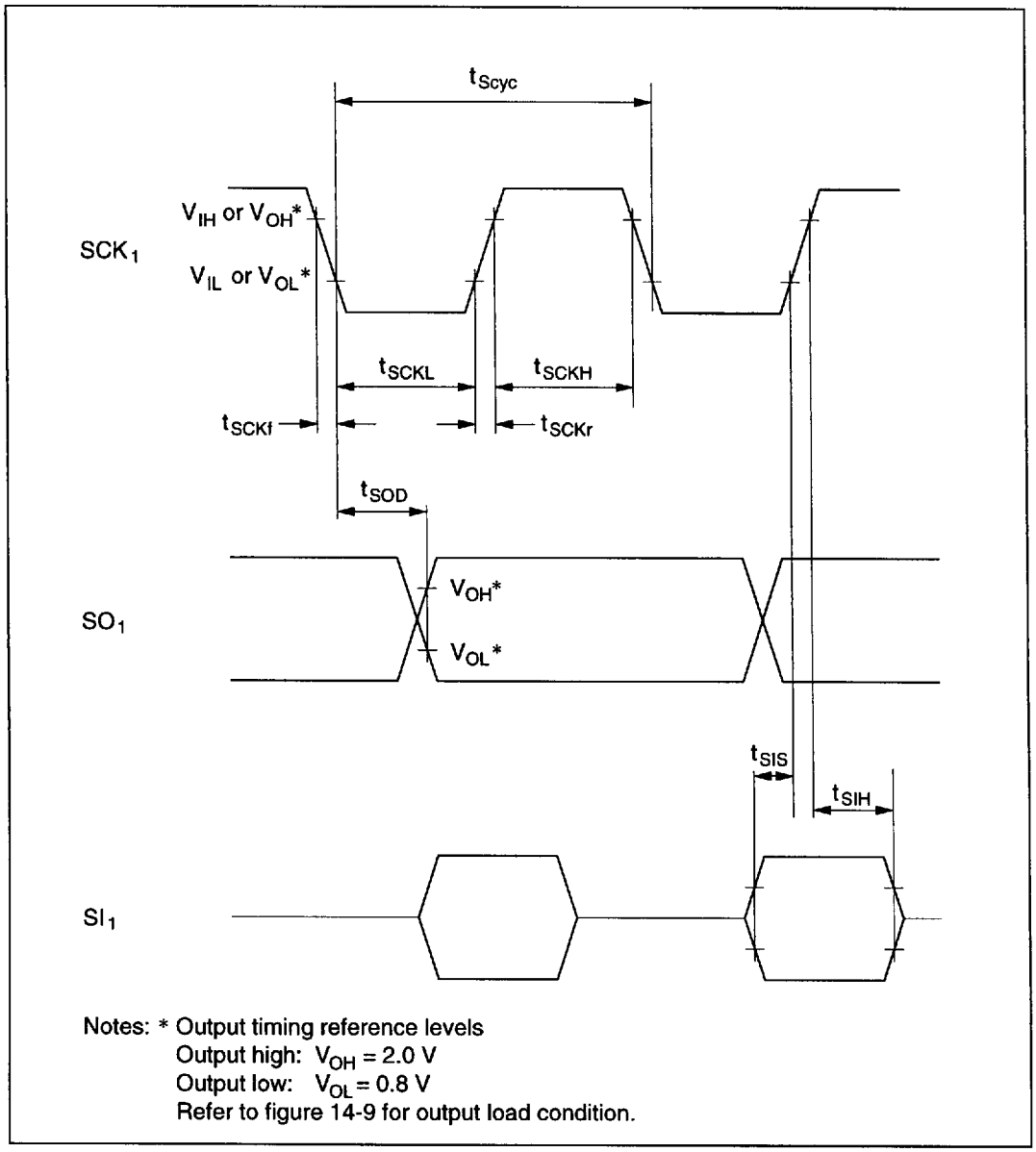


Figure 14-5 Input Timing



Notes: * Output timing reference levels
Output high: V_{OH} = 2.0 V
Output low: V_{OL} = 0.8 V
Refer to figure 14-9 for output load condition.

Figure 14-6 Serial Interface 1 Input/Output Timing

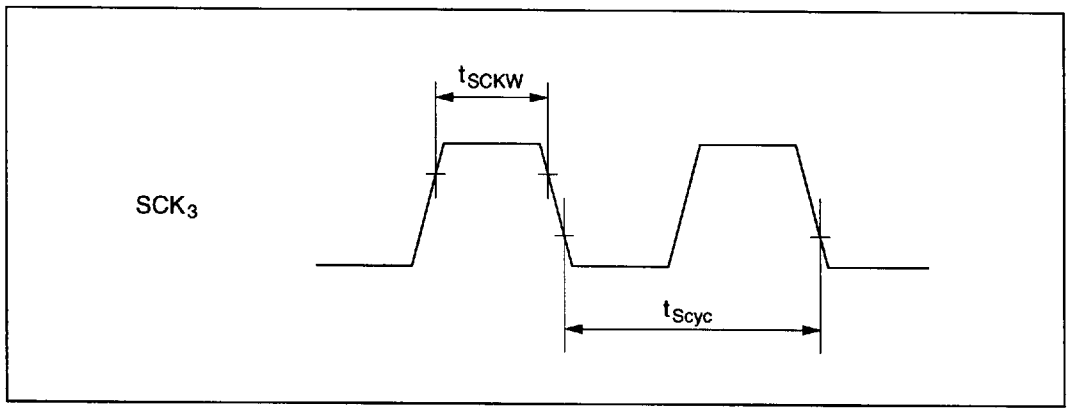
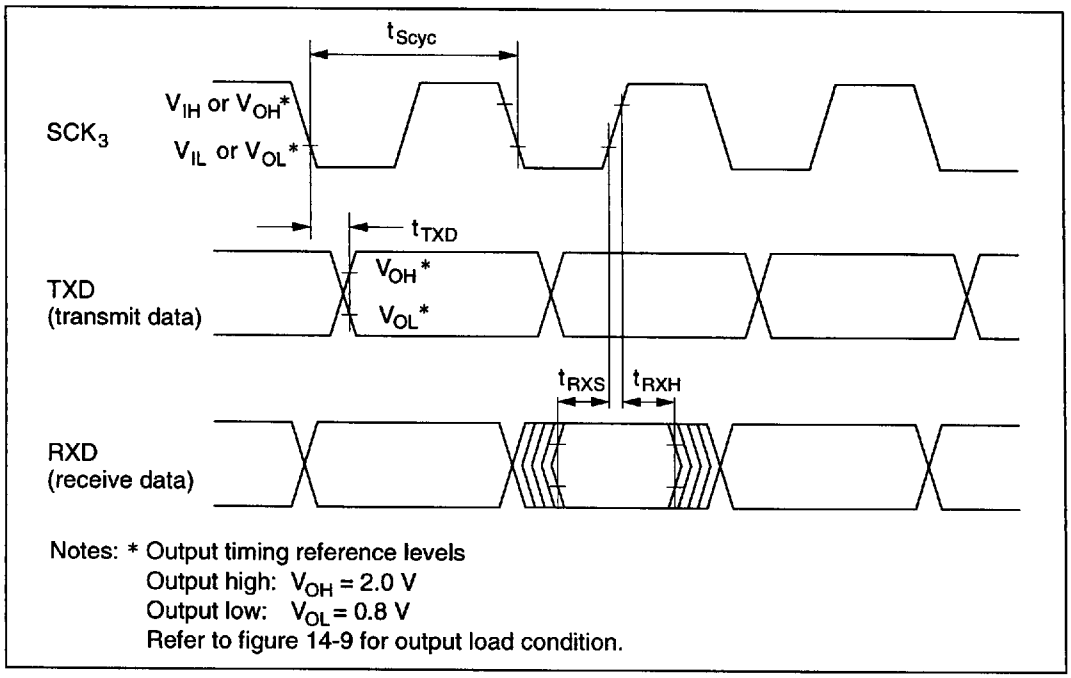


Figure 14-7 SCK_3 Input Clock Timing



Notes: * Output timing reference levels
Output high: V_{OH} = 2.0 V
Output low: V_{OL} = 0.8 V
Refer to figure 14-9 for output load condition.

Figure 14-8 Input/Output Timing of Serial Interface 3 in Synchronous Mode

14.4 Output Load Circuits

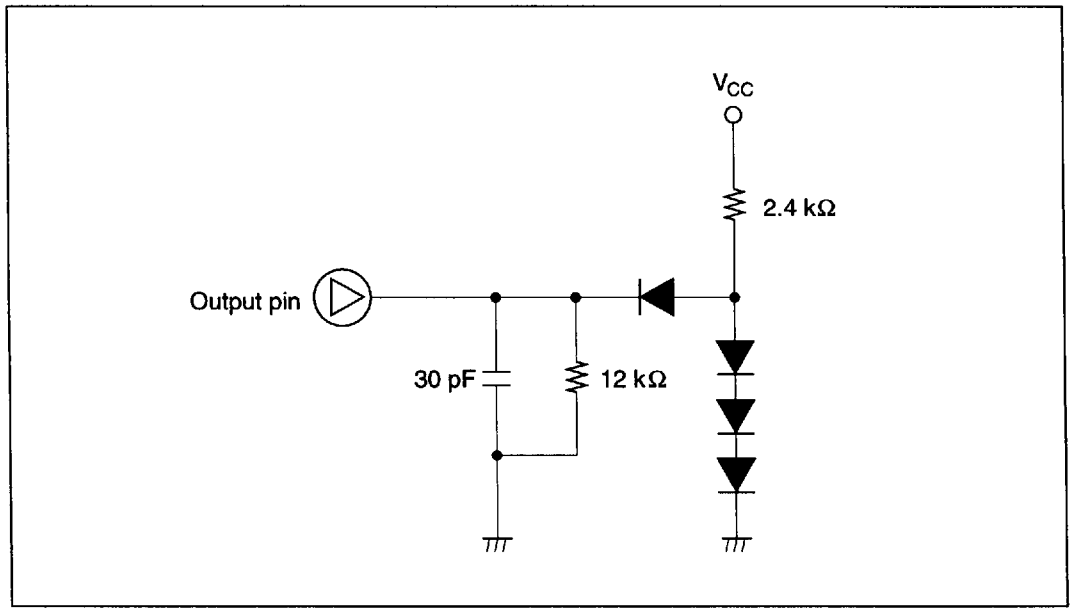


Figure 14-9 Output Load Condition