
HB56U232BA/SBA Series

2,097,152-word $\times$ 32-bit High Density Dynamic RAM Module

HITACHI

ADE-203-721B (Z)

Rev. 2.0

May. 26, 1997

Description

The HB56U232BA/SBA is a $2M \times 32$ dynamic RAM module, mounted 4 pieces of 16-Mbit DRAM (HM5117805) sealed in SOJ package. The HB56U232BA/SBA offers Extended Data Out (EDO) Page Mode as a high speed access time. An outline of the HB56U232BA/SBA is 72-pin single in-line package. Therefore, the HB56U232BA/SBA makes high density mounting possible without surface mount technology. The HB56U232BA/SBA provides common data inputs and outputs. Decoupling capacitors are mounted on the module board.

Features

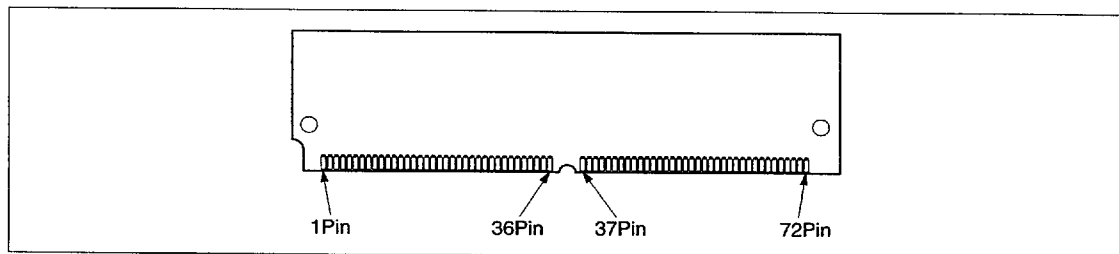
- 72-pin single in-line package
 - Outline: 107.95 mm (Length) $\times$ 25.40 mm (Height) $\times$ 5.28 mm (Thickness)
 - Lead pitch: 1.27 mm
- Single 5 V ($\pm 5\%$) supply
- High speed
 - Access time: $t_{RAC} = 50/60/70$ ns (max)
- Low power dissipation
 - Active mode: 2.31/2.10/1.89 W (max)
 - Standby mode (TTL): 42 mW (max)
(CMOS): 3.15 mW (max) (L-version)
- EDO page mode capability
- Refresh period
 - 2048 refresh cycles: 32 ms
128 ms (L-version)
- 3 variations of refresh
 - $\overline{RAS}$ -only refresh
 - $\overline{CAS}$ -before- $\overline{RAS}$ refresh
 - Hidden refresh
- TTL compatible

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Ordering Information

Type No.	Access time	Package	Contact pad
HB56U232BA-5N	50 ns	72-pin SIP socket type	Gold
HB56U232BA-6N	60 ns		
HB56U232BA-7N	70 ns		
HB56U232BA-5NL	50 ns		
HB56U232BA-6NL	60 ns		
HB56U232BA-7NL	70 ns		
HB56U232SBA-5N	50 ns	72-pin SIP socket type	Solder
HB56U232SBA-6N	60 ns		
HB56U232SBA-7N	70 ns		
HB56U232SBA-5NL	50 ns		
HB56U232SBA-6NL	60 ns		
HB56U232SBA-7NL	70 ns		

Pin Arrangement



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Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V _{ss}	19	A10	37	NC	55	DQ11
2	DQ0	20	DQ4	38	NC	56	DQ27
3	DQ16	21	DQ20	39	V _{ss}	57	DQ12
4	DQ1	22	DQ5	40	CAS0	58	DQ28
5	DQ17	23	DQ21	41	CAS2	59	V _{cc}
6	DQ2	24	DQ6	42	CAS3	60	DQ29
7	DQ18	25	DQ22	43	CAS1	61	DQ13
8	DQ3	26	DQ7	44	RAS0	62	DQ30
9	DQ19	27	DQ23	45	NC	63	DQ14
10	V _{cc}	28	A7	46	NC	64	DQ31
11	NC	29	NC	47	WE	65	DQ15
12	A0	30	V _{cc}	48	NC	66	NC
13	A1	31	A8	49	DQ8	67	PD1
14	A2	32	A9	50	DQ24	68	PD2
15	A3	33	NC	51	DQ9	69	PD3
16	A4	34	RAS2	52	DQ25	70	PD4
17	A5	35	NC	53	DQ10	71	NC
18	A6	36	NC	54	DQ26	72	V _{ss}

Pin Description

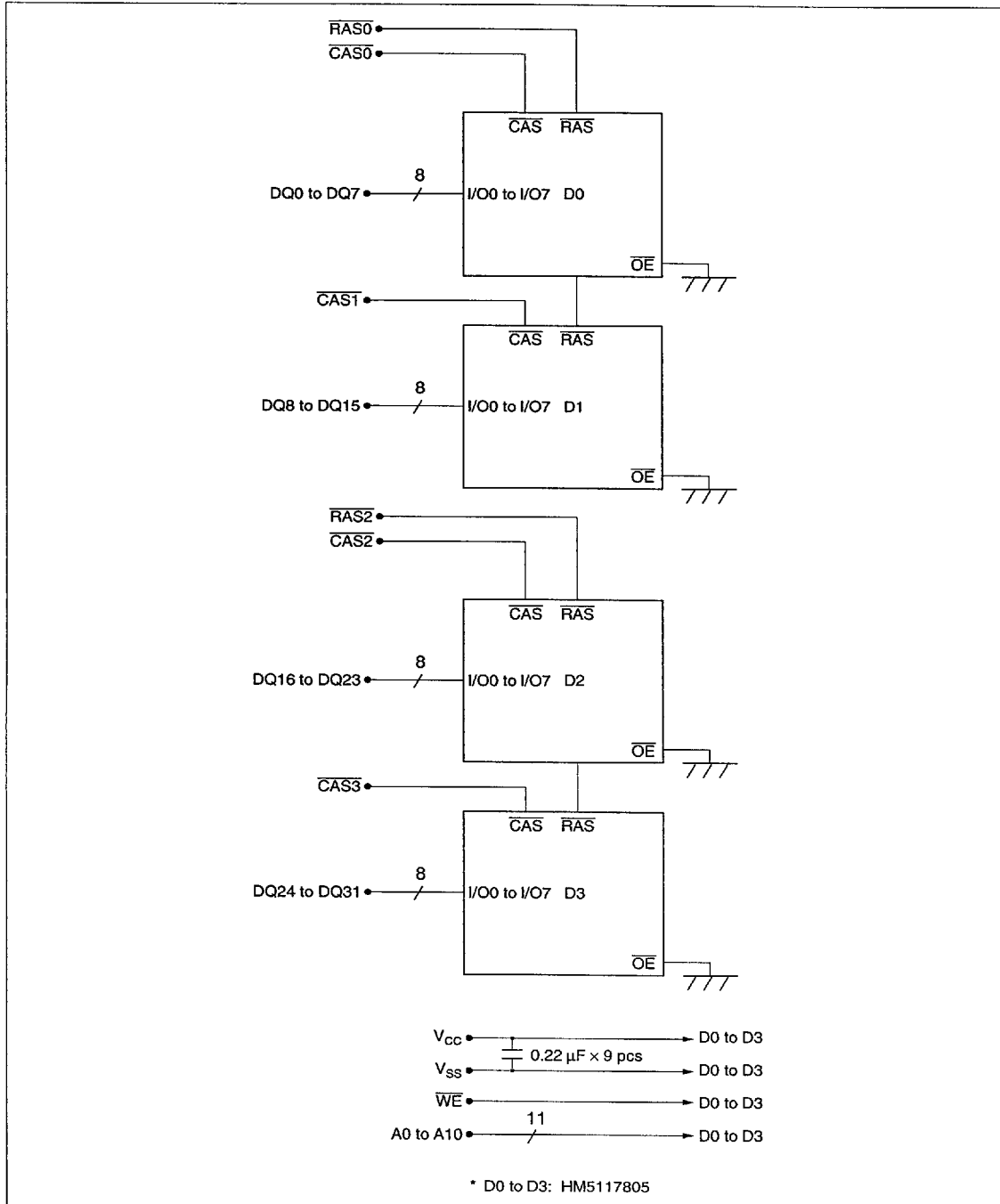
Pin name	Function
A0 to A10	Address inputs: • Row address: A0 to A10 • Column address: A0 to A9 • Refresh address: A0 to A10
DQ0 to DQ31	Data-in/Data-out
CAS0 to CAS3	Column address strobe
RAS0, RAS2	Row address strobe
WE	Read/Write enable
V _{cc}	Power supply
V _{ss}	Ground
PD1 to PD4	Presence detect pin
NC	No connection

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Presence Detect Pin Arrangement

Pin No.	Pin name	Function		
		50 ns	60 ns	70 ns
67	PD1	NC	NC	NC
68	PD2	NC	NC	NC
69	PD3	V _{ss}	NC	V _{ss}
70	PD4	V _{ss}	NC	NC

Block Diagram



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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	-1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_t	4	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C

Recommended DC Operating Conditions ($T_a = 0$ to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	-1.0	—	0.8	V	1

Note: 1. All voltage referred to V_{SS} .

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DC Characteristics ($T_a = 0 \text{ to } 70^\circ\text{C}$, $V_{CC} = 5 \text{ V} \pm 5\%$, $V_{SS} = 0 \text{ V}$)

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Test conditions	Notes
		Min	Max	Min	Max	Min	Max			
Operating current	I_{CC1}	—	440	—	400	—	360	mA	$t_{RC} = \text{min}$	1, 2
Standby current	I_{CC2}	—	8	—	8	—	8	mA	TTL interface, $\overline{RAS}, \overline{CAS} = V_{IH}$, Dout = High-Z	
		—	4	—	4	—	4	mA	CMOS interface, $\overline{RAS}, \overline{CAS} \geq V_{CC} - 0.2 \text{ V}$, Dout = High-Z	
Standby current (L-version)	I_{CC2}	—	0.6	—	0.6	—	0.6	mA	CMOS interface, $\overline{RAS}, \overline{CAS} \geq V_{CC} - 0.2 \text{ V}$, Dout = High-Z	
$\overline{RAS}$ -only refresh current	I_{CC3}	—	440	—	400	—	360	mA	$t_{RC} = \text{min}$	2
Standby current	I_{CC5}	—	20	—	20	—	20	mA	$\overline{RAS} = V_{IH}$, $\overline{CAS} = V_{IL}$, Dout = enable	1
$\overline{CAS}$ -before- $\overline{RAS}$ refresh current	I_{CC6}	—	440	—	400	—	360	mA	$t_{RC} = \text{min}$	
EDO page mode current	I_{CC7}	—	400	—	360	—	340	mA	$t_{HPC} = \text{min}$	1, 3
Battery backup current (Standby with CBR refresh) (L-version)	I_{CC10}	—	2	—	2	—	2	mA	CMOS interface, Dout = High-Z, CBR refresh: $t_{RC} = 62.5 \mu\text{s}$, $t_{RAS} \leq 0.3 \mu\text{s}$	4
Input leakage current	I_{LI}	-10	10	-10	10	-10	10	μA	$0 \text{ V} \leq V_{in} \leq 5.5 \text{ V}$	
Output leakage current	I_{LO}	-10	10	-10	10	-10	10	μA	$0 \text{ V} \leq V_{out} \leq 5.5 \text{ V}$, Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = -2 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while $\overline{RAS} = V_{IL}$.

3. Address can be changed once or less while $\overline{CAS} = V_{IH}$.

4. $\overline{CAS} = L$ ($\leq 0.2 \text{ V}$) while $\overline{RAS} = L$ ($\leq 0.2 \text{ V}$).

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Capacitance ($T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	40	pF	1
Input capacitance ($\overline{WE}$)	C_{I2}	—	48	pF	1
Input capacitance ($\overline{RAS}$)	C_{I3}	—	29	pF	1
Input capacitance ($\overline{CAS}$)	C_{I4}	—	22	pF	1
I/O capacitance (DQ)	$C_{I/O}$	—	22	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. $\overline{CAS} = V_{IH}$ to disable Dout.

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AC Characteristics ($T_a = 0$ to 70°C , $V_{CC} = 5\text{ V} \pm 5\%$, $V_{SS} = 0\text{ V}$) ^{*1, *2, *18}

Test Conditions

- Input rise and fall times: 2 ns
- Input level: 0 V, 3.0V
- Input timing reference levels: 0.8 V, 2.4 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, and Refresh Cycles (Common parameters)

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84	—	104	—	124	—	ns	
RAS precharge time	t_{RP}	30	—	40	—	50	—	ns	
CAS precharge time	t_{CP}	7	—	10	—	13	—	ns	
RAS pulse width	t_{RAS}	50	10000	60	10000	70	10000	ns	
CAS pulse width	t_{CAS}	7	10000	10	10000	13	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	7	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	7	—	10	—	13	—	ns	
RAS to CAS delay time	t_{RCD}	11	37	14	45	14	52	ns	3
RAS to column address delay time	t_{RAD}	9	25	12	30	12	35	ns	4
RAS hold time	t_{RSH}	10	—	13	—	13	—	ns	
CAS hold time	t_{CSH}	35	—	40	—	45	—	ns	
CAS to RAS precharge time	t_{CRP}	5	—	5	—	5	—	ns	
CAS delay time from Din	t_{DZC}	0	—	0	—	0	—	ns	
Transition time (rise and fall)	t_T	2	50	2	50	2	50	ns	5
Refresh period (2,048 cycles)	t_{REF}	—	32	—	32	—	32	ms	
Refresh period (2,048 cycles) (L-version)	t_{REF}	—	128	—	128	—	128	ms	

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Read Cycle

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	50	—	60	—	70	ns	6, 7
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	13	—	15	—	18	ns	7, 8, 15
Access time from address	t_{AA}	—	25	—	30	—	35	ns	7, 9, 15
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	0	—	ns	10
Read command hold time from $\overline{\text{RAS}}$	t_{RCHR}	50	—	60	—	70	—	ns	
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	5	—	5	—	5	—	ns	10
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	25	—	30	—	35	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	t_{CAL}	15	—	18	—	23	—	ns	
$\overline{\text{CAS}}$ to output in low-Z	t_{CLZ}	0	—	0	—	0	—	ns	
Output data hold time	t_{OH}	3	—	3	—	3	—	ns	19
Output buffer turn-off time	t_{OFF}	—	13	—	15	—	15	ns	11, 19
$\overline{\text{CAS}}$ to Din delay time	t_{CDD}	13	—	15	—	18	—	ns	
Output data hold time from $\overline{\text{RAS}}$	t_{OHR}	3	—	3	—	3	—	ns	19
Output buffer turn-off time to $\overline{\text{RAS}}$	t_{OFR}	—	13	—	15	—	15	ns	19
Output buffer turn-off to $\overline{\text{WE}}$	t_{WEZ}	—	13	—	15	—	15	ns	
$\overline{\text{WE}}$ to Din delay time	t_{WED}	13	—	15	—	18	—	ns	
$\overline{\text{RAS}}$ to Din delay time	t_{RDD}	13	—	15	—	18	—	ns	
$\overline{\text{RAS}}$ to next $\overline{\text{CAS}}$ delay time	t_{RNCD}	50	—	60	—	70	—	ns	

Write Cycle

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	12
Write command hold time	t_{WCH}	7	—	10	—	13	—	ns	
Write command pulse width	t_{WP}	7	—	10	—	10	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	13
Data-in hold time	t_{DH}	7	—	10	—	13	—	ns	13

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Refresh Cycle

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
CAS setup time (CBR refresh cycle)	t_{CSR}	5	—	5	—	5	—	ns	
CAS hold time (CBR refresh cycle)	t_{CHR}	7	—	10	—	10	—	ns	
WE setup time (CBR refresh cycle)	t_{WRP}	0	—	0	—	0	—	ns	
WE hold time (CBR refresh cycle)	t_{WRH}	7	—	10	—	10	—	ns	
RAS precharge to CAS hold time	t_{RPC}	5	—	5	—	5	—	ns	

EDO Page Mode Cycle

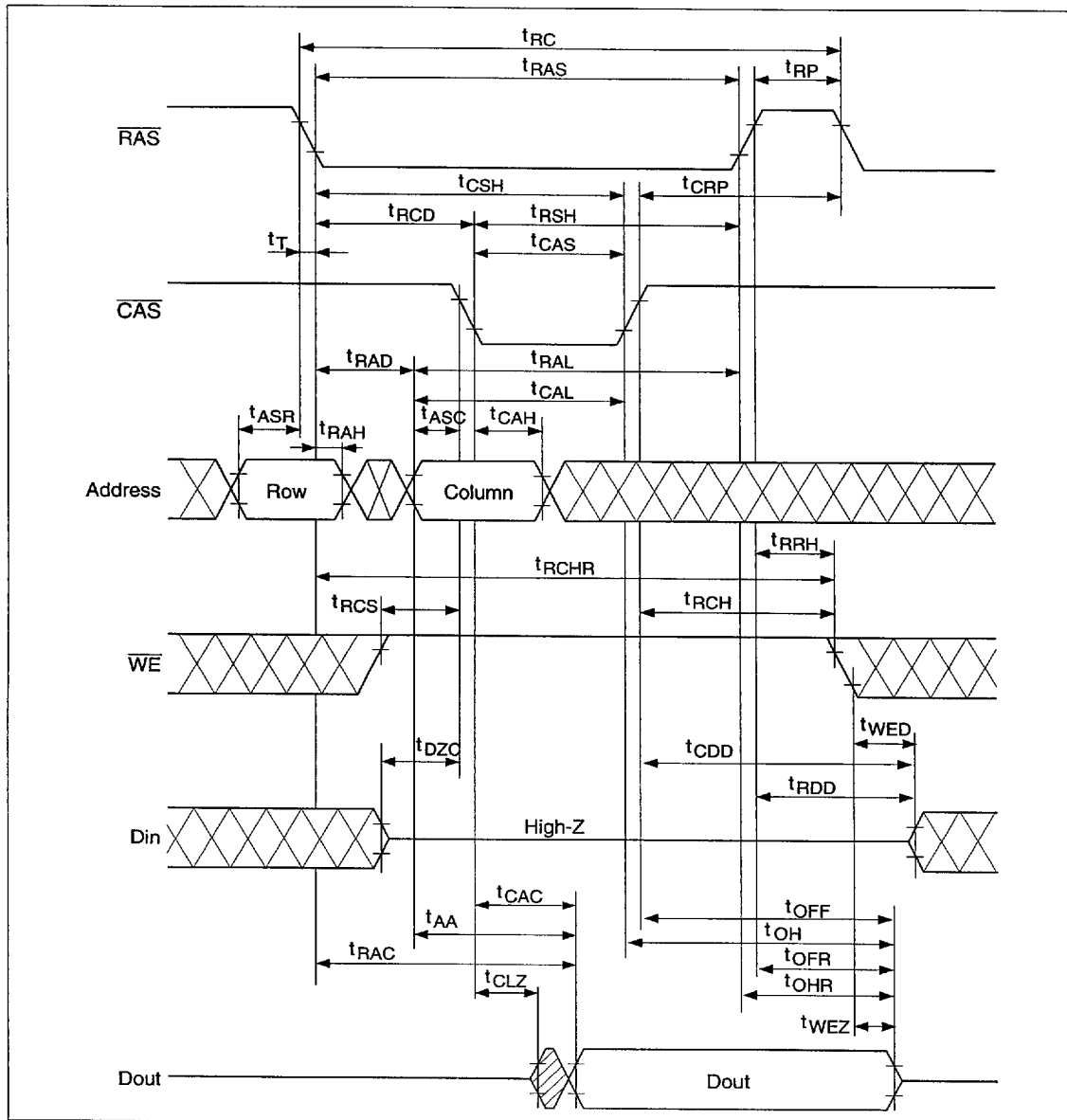
Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
EDO page mode cycle time	t_{HPC}	20	—	25	—	30	—	ns	16
EDO page mode RAS pulse width	t_{RASP}	—	100000	—	100000	—	100000	ns	14
Access time from CAS precharge	t_{CPA}	—	28	—	35	—	40	ns	7, 15
RAS hold time from CAS precharge	t_{CPRH}	28	—	35	—	40	—	ns	
Output data hold time from CAS low	t_{DOH}	3	—	3	—	3	—	ns	7, 15
Read command hold time from CAS precharge	t_{RCHC}	28	—	35	—	40	—	ns	

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- Notes:
1. AC measurements assume $t_T = 2 \text{ ns}$.
 2. An initial pause of $200 \mu\text{s}$ is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{\text{RAS}}$ -only refresh cycle or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles are required.
 3. Operation with the $t_{\text{RCD}} (\text{max})$ limit insures that $t_{\text{RAC}} (\text{max})$ can be met, $t_{\text{RCD}} (\text{max})$ is specified as a reference point only; if $t_{\text{RCD}} \geq t_{\text{RCD}} (\text{max}) + t_{\text{AA}} (\text{max}) - t_{\text{CAC}} (\text{max})$, then access time is controlled exclusively by t_{CAC} .
 4. Operation with the $t_{\text{RAD}} (\text{max})$ limit insures that $t_{\text{RAC}} (\text{max})$ can be met, $t_{\text{RAD}} (\text{max})$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{\text{RAD}} (\text{max})$ limit, then access time is controlled exclusively by t_{AA} .
 5. $V_{\text{IH}} (\text{min})$ and $V_{\text{IL}} (\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between $V_{\text{IH}} (\text{min})$ and $V_{\text{IL}} (\text{max})$.
 6. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}} (\text{max})$ and $t_{\text{RAD}} \leq t_{\text{RAD}} (\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 7. Measured with a load circuit equivalent to 1 TTL loads and 100 pF .
 8. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}} (\text{max})$ and $t_{\text{RCD}} + t_{\text{CAC}} (\text{max}) \geq t_{\text{RAD}} + t_{\text{AA}} (\text{max})$.
 9. Assumes that $t_{\text{RAD}} \geq t_{\text{RAD}} (\text{max})$ and $t_{\text{RCD}} + t_{\text{CAC}} (\text{max}) \leq t_{\text{RAD}} + t_{\text{AA}} (\text{max})$.
 10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
 11. $t_{\text{OFF}} (\text{max})$ defines the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
 12. Early write cycle only ($t_{\text{WCS}} \geq t_{\text{WCS}} (\text{min})$).
 13. These parameters are referred to $\overline{\text{CAS}}$ leading edge in early write cycles.
 14. t_{RASp} defines $\overline{\text{RAS}}$ pulse width in EDO page mode cycles.
 15. Access time is determined by the longest among t_{AA} , t_{CAC} and t_{CPA} .
 16. $t_{\text{HPC}} (\text{min})$ can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles.
 17. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large $V_{\text{CC}} / V_{\text{SS}}$ line noise, which causes to degrade $V_{\text{IH}} \text{ min.} / V_{\text{IL}} \text{ max level.}$
 18. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
 19. Data output turns off and becomes high impedance from later rising edge of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$. Hold time and turn off time are specified by the timing specifications of later rising edge of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ between t_{OHR} and t_{OH} , and between t_{OFFR} and t_{OFF} .
 20. XXX: H or L (H: $V_{\text{IH}} (\text{min}) \leq V_{\text{IN}} \leq V_{\text{IH}} (\text{max})$, L: $V_{\text{IL}} (\text{min}) \leq V_{\text{IN}} \leq V_{\text{IL}} (\text{max})$)
 ///////////////: Invalid Dout
 When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL} .

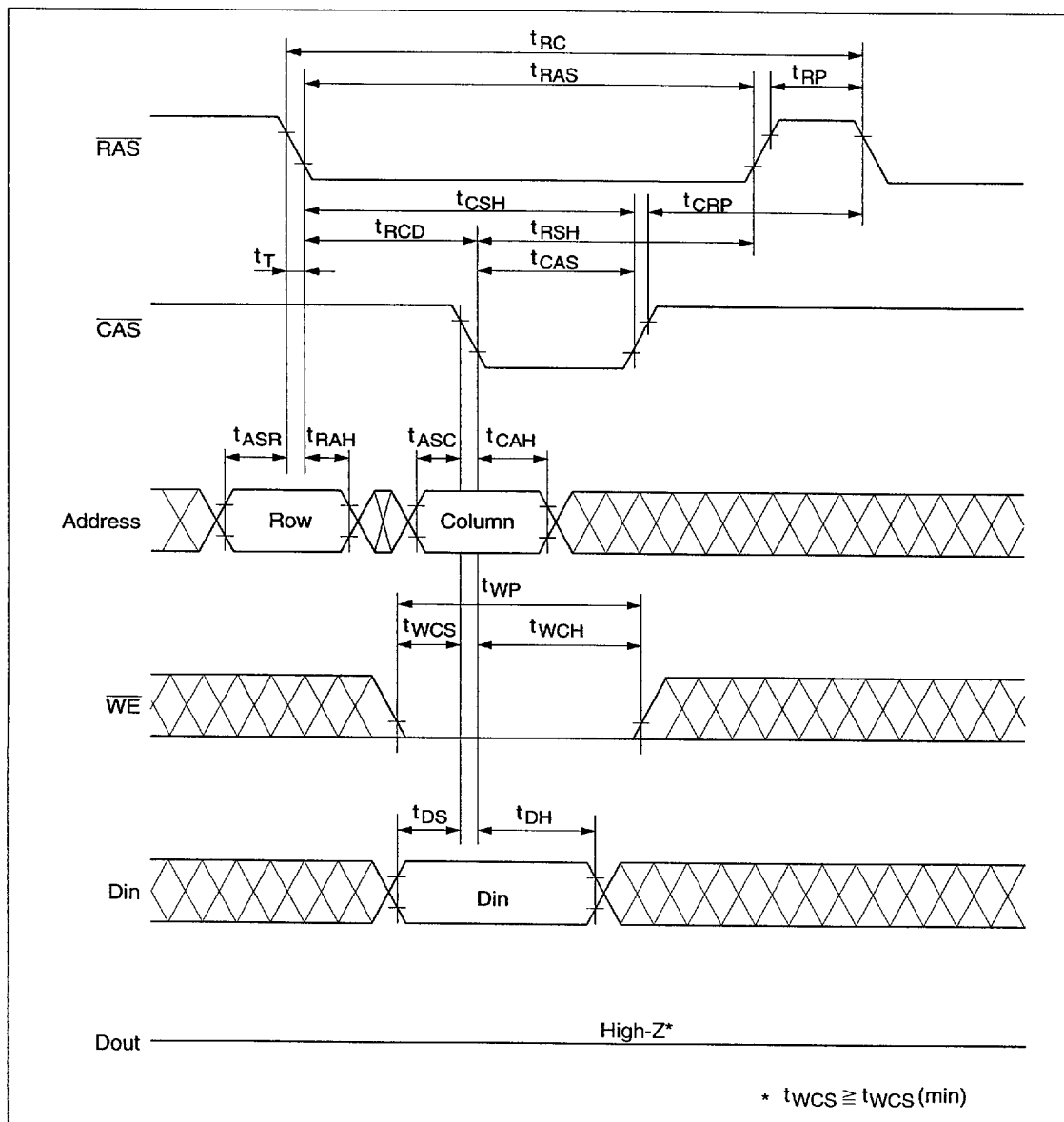
Timing Waveforms*20

Read Cycle

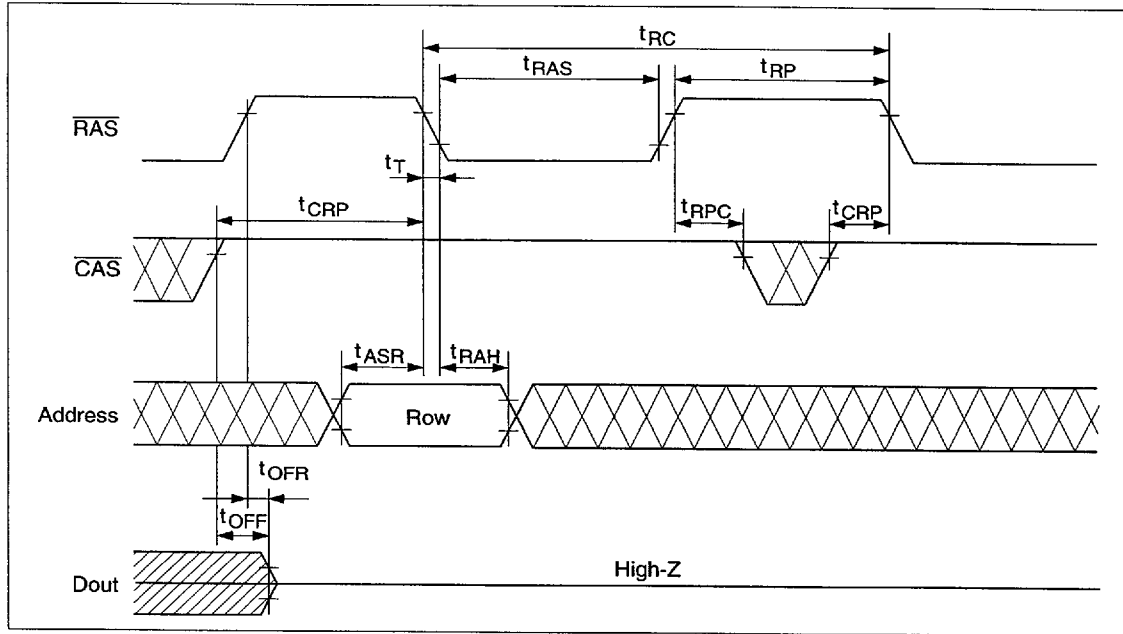


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Early Write Cycle

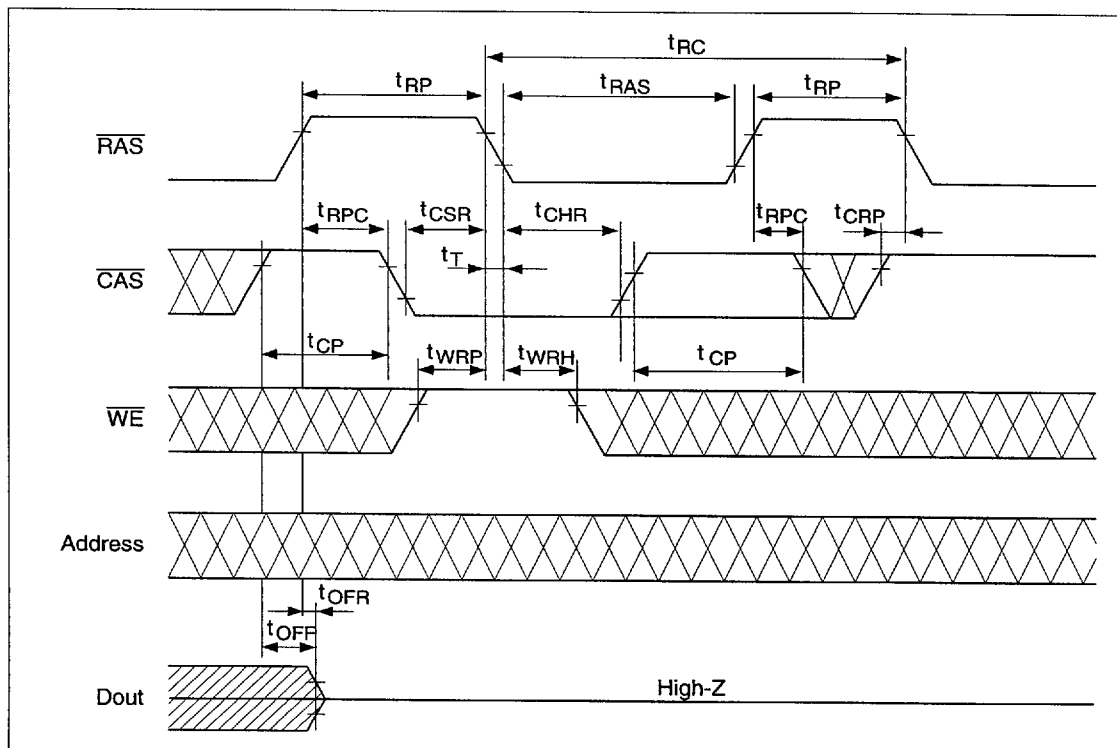


RAS-Only Refresh Cycle

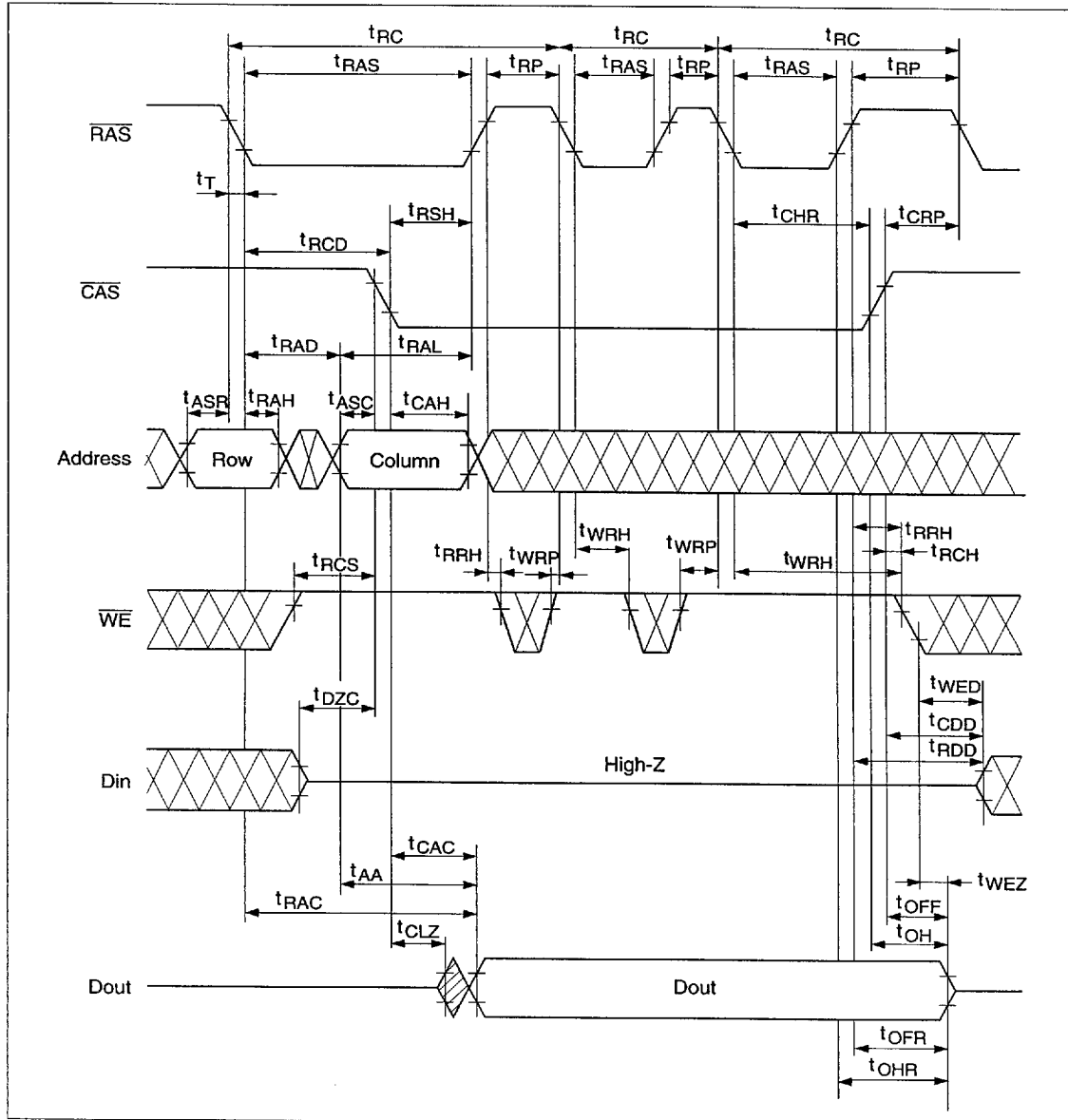


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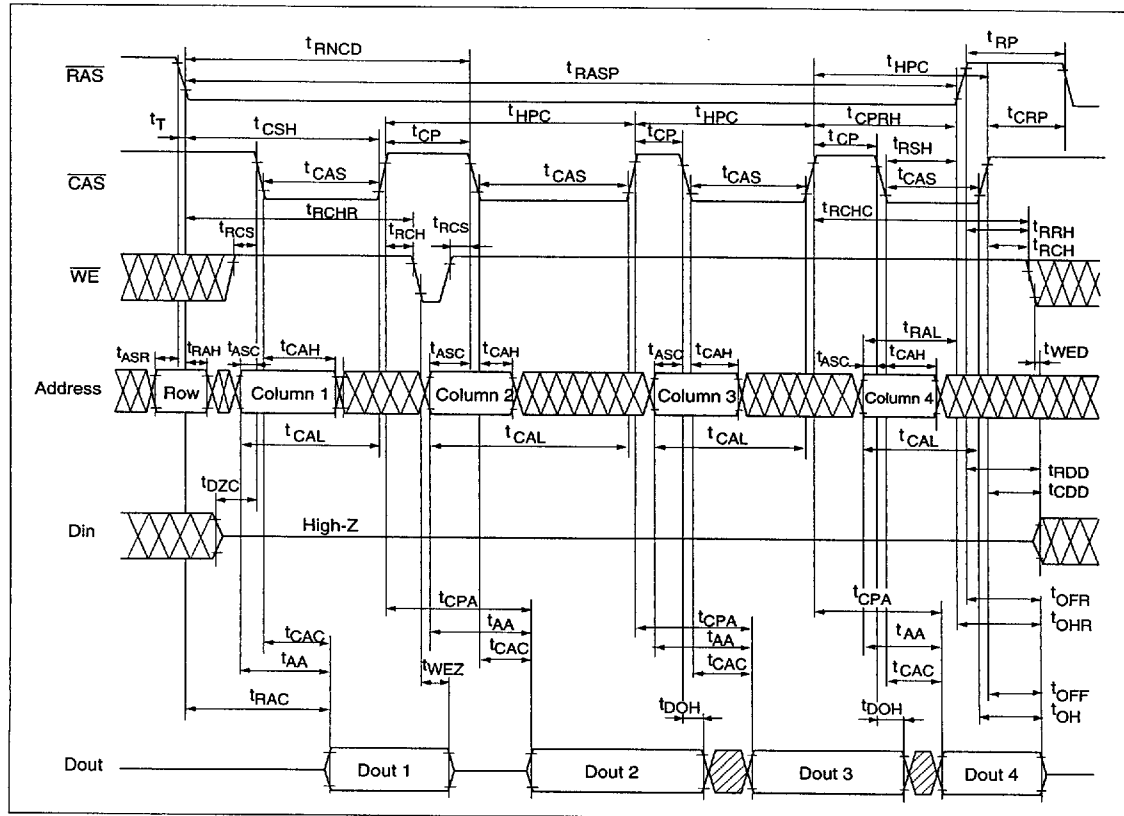
$\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh Cycle



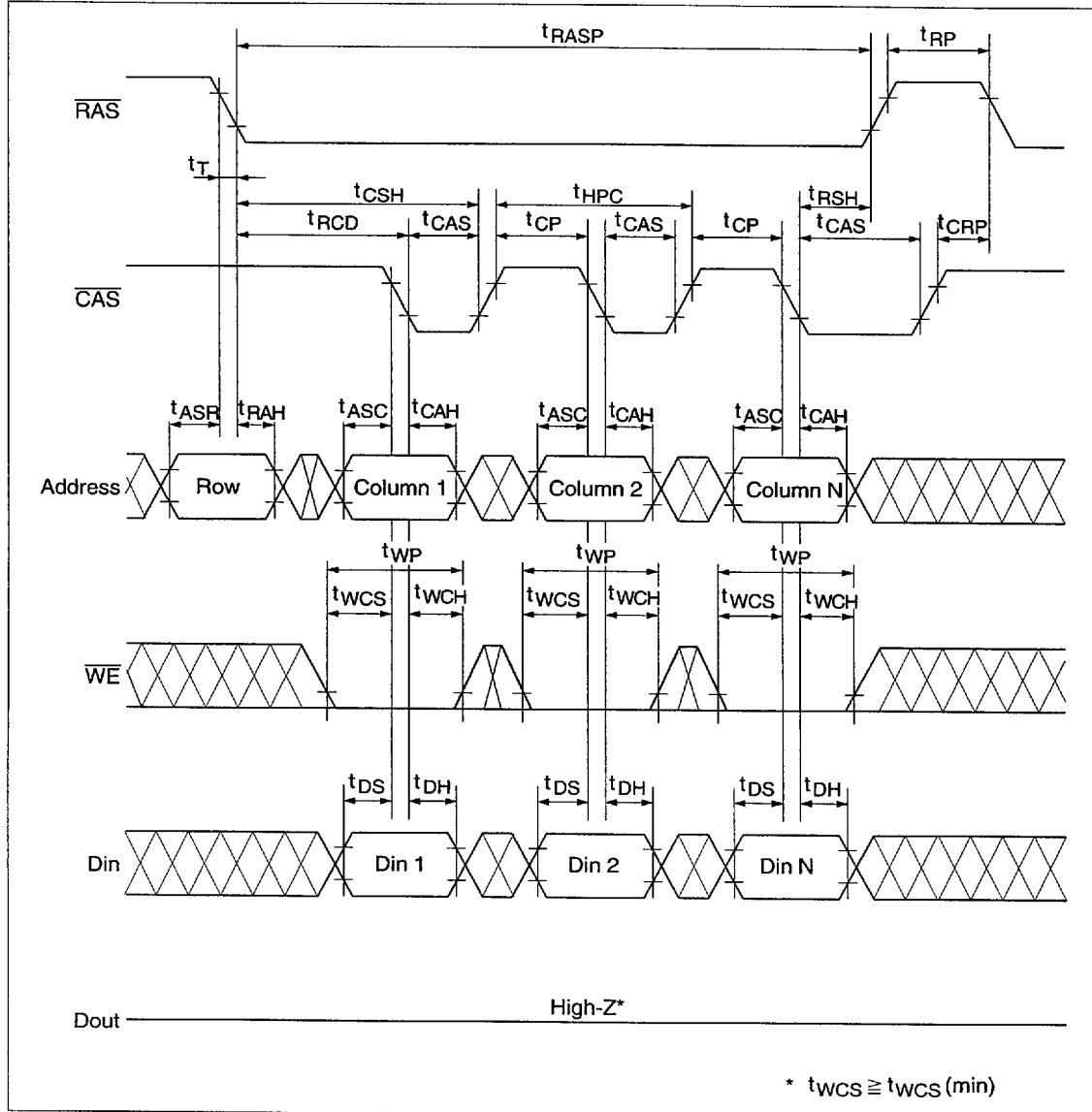
Hidden Refresh Cycle



EDO Page Mode Read Cycle



EDO Page Mode Early Write Cycle



HB56U232BA/SBA Series

Physical Outline

