



Description

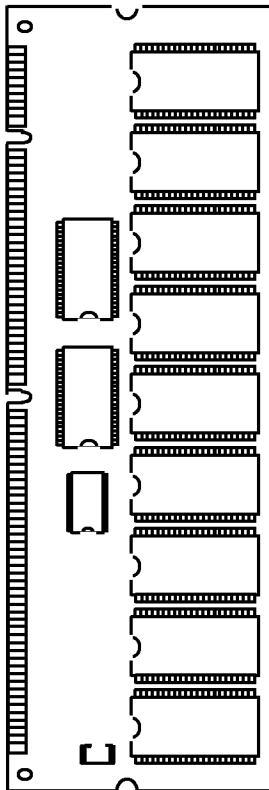
The GMM27333230ATG is a 32M x 72bits Synchronous Dynamic RAM MODULE which is assembled 18 pieces of 32M x 4bits Synchronous DRAMs in 54 pin TSOP II, 2 pieces of 16 bits Register in 48 pin TSSOP, one clock distribution PLL in 24 pin SOP and one 2048 bit EEPROM in 8 pin TSSOP package mounted on a 168 pin printed circuit board with decoupling capacitors. The GMM27333230ATG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

The GMM27333230ATG provides common data inputs and outputs.

Features

- * PC133/PC100/PC66 Compatible
-75(133MHz)/-8(125MHz)
-7K(PC100,2-2-2)/-7J(PC100,3-2-2)/-10K(PC66)
- * 3.3V +/- 0.3V Power supply
- * Maximum Clock frequency
100 / 125 / 133 MHz
- * LVTTTL Interface
- * Burst read/write operation and burst read/
single write operation capability
- * Programmable burst length ;
1, 2, 4, 8, Full page
- * Programmable burst sequence
Sequential / Interleave
- * Full Page burst length capability
Sequential burst
Burst stop capability
- * Programmable CAS Latency ; 2, 3
- * CKE power down mode
- * Input / Output data masking
- * 4096 Refresh Cycles / 64ms
- * Auto refresh / Self refresh Capability
- * Serial Presence Detect with EEPROM

GMM27333230ATG (Double Side)



Pin Name

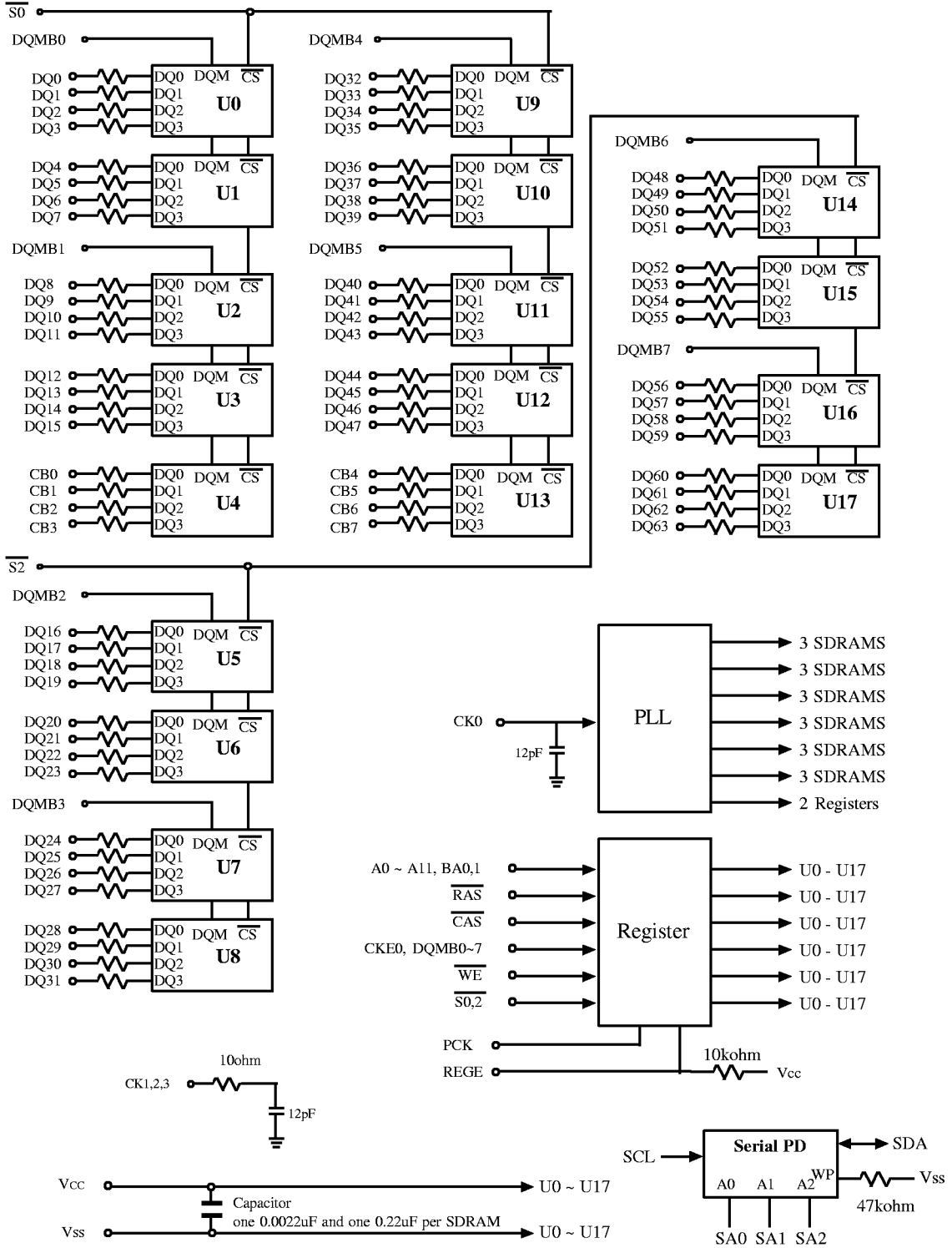
CK0, 1, 2, 3	Clock input
CKE0	Clock Enable
S0, 2	Chip Select
RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Write Enable
A0 ~ A11	Address input
BA0,1	Bank Address input
REGE	Register Enable
DQ0 ~ 63	Data input / output
CB0 ~ 7	Check Bits
DQMB0 ~ 7	Data input / output Mask
VCC	Power for internal circuit
VSS	Ground for internal circuit
NC	No Connect
VREF	Power Supply for Reference
SDA	Serial Data input/ output
SCL	Serial Clock
SA0 ~ 2	Address in EEPROM
WP	Write Protect for SPD
DU	Don't Use

Pin Configuration

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	Vss	29	DQMB1	57	DQ18	85	Vss	113	DQMB5	141	DQ50
2	DQ0	30	$\overline{S0}$	58	DQ19	86	DQ32	114	$\overline{*S1}$	142	DQ51
3	DQ1	31	DU	59	Vcc	87	DQ33	115	\overline{RAS}	143	Vcc
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vcc	34	A2	62	*VREF, NC	90	Vcc	118	A3	146	*VREF, NC
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	Vcc	69	DQ24	97	DQ41	125	CK1	153	DQ56
14	DQ10	42	CK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{S2}$	73	Vcc	101	DQ45	129	$\overline{*S3}$	157	Vcc
18	Vcc	46	DQMB2	74	DQ28	102	Vcc	130	DQMB6	158	DQ60
19	DQ14	47	DQMB3	75	DQ29	103	DQ46	131	DQMB7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	Vcc	77	DQ31	105	CB4	133	Vcc	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	CK2	107	Vss	135	NC	163	CK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	SA0
26	\overline{Vcc}	54	Vss	82	SDA	110	\overline{Vcc}	138	Vss	166	SA1
27	WE	55	DQ16	83	SCL	111	\overline{CAS}	139	DQ48	167	SA2
28	DQMB0	56	DQ17	84	Vcc	112	DQMB4	140	DQ49	168	Vcc

* These pins are not used in this module

Block Diagram



Pin Description

Pin Name	DESCRIPTION
CK0, 1, 2, 3 (input pins)	CK is the master clock input to this pin. The other input signals are referred at CK rising edge.
CKE0 (input pin)	This pin determines whether or not the next CK is valid. If CKE is High, the next CK rising edge is valid. If CKE is Low, the next CK rising edge is invalid. This pin is used for power-down and clock suspend modes.
$\overline{S0, 2}$ (input pins)	When \overline{S} is Low, the command input cycle becomes valid. When \overline{S} is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.
\overline{RAS} , \overline{CAS} and \overline{WE} (input pins)	Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.
A0 ~ A11 (input pins)	Row address (AX0 to AX11) is determined by A0 to A11 level at the bank active command cycle CK rising edge. Column address is determined by A0 to A9 and A11 level at the read or write command cycle CK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by BA0 is precharged.
BA0,1 (input pin)	BA0,1 are bank select signal. If BA0 is Low and BA1 is High, bank 0 is selected. If BA0 is High and BA1 is Low, bank 1 is selected. If BA0 is Low and BA1 is High, bank 2 is selected. If BA0 is High and BA1 is High, bank 3 is selected.
DQ0 ~ DQ63 CB0 ~ CB7 (I/O pins)	Data is input and output from these pins. These pins are the same as those of a conventional DRAMs. Data is not latched in the register.
DQMB0 ~ DQMB7 (input pins)	DQMB controls input/output buffers. Read operation: If DQMB is High, The output buffer becomes High-Z. If the DQMB is Low, the output buffer becomes Low-Z. Write operation: If DQMB is High, the previous data is held (the new data is not written). If DQMB is Low, the data is written.
Vcc (power supply pins)	3.3 V is applied. (Vcc is for the internal circuit)
Vss (power supply pins)	Ground is connected. (Vss is for the internal circuit)
REGE	If REGE input is high, permits the DIMM to operate in `registered mode`. If REGE input is low, permits the DIMM to operate in `buffered mode`.
NC	No Connection pins.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to Vss	V _T	-0.5 to V _{CC} +0.5 (≤ 4.6 (max))	V	1
Supply voltage relative to Vss	V _{CC}	-0.5 to +4.6	V	1
Short circuit output current	I _{OUT}	50	mA	
Power dissipation	P _T	1.0	W	
Operating temperature	T _{opr}	0 to +70	C	
Storage temperature	T _{stg}	-55 to +125	C	

Notes : 1. Respect to Vss

Recommended DC Operating Conditions (T_a = 0 to + 70C)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V _{CC} , V _{CCQ}	3.0	3.6	V	1
	V _{SS} , V _{SSQ}	0	0	V	
Input high voltage	V _{IH}	2.0	V _{CC} + 0.3	V	1, 2
Input low voltage	V _{IL}	-0.3	0.8	V	1,3

Notes : 1. All voltage referred to Vss.

2. V_{IH} (max) = 5.6V for pulse width ≤ 3ns

3. V_{IL} (min) = -2.0V for pulse width ≤ 3ns

Registered DIMM Operation

1. All control and address signals are registered on-DIMM register and hence delayed by one cycle in arriving at the SDRAMs. But data is not registered in the register.
2. CAS latency defines the delay from when a READ command is registered on a rising clock edge to when the data from that READ command becomes available at the outputs. Do not confuse DIMM CAS latency with the SDRAM CAS latency which is one clock less.

DC Characteristics (Ta = 0 to 70C, Vcc, Vccq = 3.3 V +/- 0.3 V, Vss, Vssq = 0 V)

Parameter	Symbol	- 75	- 8	- 7K	- 7J	- 10K	Unit	Test conditions	Notes	
		Max	Max	Max	Max	Max				
Operating current	Icc1	1800	1700			1600	mA	Burst length= 1 trc = min	1, 2, 3	
Standby current in power down	Icc2P	36					mA	CKE = VIL, tck = 12 ns	5	
Standby current in power down (input signal stable)	Icc2PS	18					mA	CKE=VIL, tck= Infinity	6	
Standby current in non power down (CAS Latency=2)	Icc2N	230					mA	CKE,CS = VIH, tck = 12ns	4	
Standby current in non power down (input signal stable)	Icc2NS	210					mA	CKE,CS = VIH, tck = Infinity	4	
Active standby current in power down	Icc3P	85					mA	CKE = VIL, tck = 12 ns, DQ = High-Z	1,2,5	
Active standby current in power down (input signal stable)	Icc3PS	75					mA	CKE = VIL, tck = Infinity	2,6	
Active standby current in non power down	Icc3N	480					mA	CKE,CS = VIH, tck = 12 ns, DQ = High-Z	1,2,4	
Active standby current in non power down (input signal stable)	Icc3NS	420					mA	CKE,CS = VIH, tck = Infinity	2,8	
Burst operating current	(CL= 2)	Icc4	1800	1800	1800	1500	1500	mA	tck = min BL = 4	1,2,3
	(CL= 3)	Icc4	2100	1950	1800	1800	1800			
Refresh current	Icc5	3600	3600	3400	3400	3200	mA	trc = min	3	
Self refresh current	Icc6	35					mA	VIH >=Vcc - 0.2 VIL <=0.2V	7	

Parameter	Symbol	- 75, - 8, - 7K, -7J, -10K		Unit	Test conditions	Notes
		Min	Max			
Input leakage current	I _{LI}	-1	1	uA	0<=V _{in} <=V _{CC}	
Output leakage current	I _{LO}	-1.5	1.5	uA	0<=V _{out} <=V _{CC} DQ = disable	
Output high voltage	V _{OH}	2.4	-	V	I _{OH} = -2 mA	
Output low voltage	V _{OL}	-	0.4	V	I _{OL} =2 mA	

- Notes :
1. I_{CC} depends on output load condition when the device is selected. I_{CC} (max) is specified at the output open condition.
 2. One bank operation.
 3. Addresses are changed once per one cycle.
 4. Addresses are changed once per two cycles.
 5. After Power down mode, CLK operating current.
 6. After Power down mode, no CLK operating current.
 7. After self refresh mode set, self refresh current.
 8. Input signals are V_{IH} or V_{IL} fixed.

Capacitance (Ta = 25C, V_{CC}, V_{CCQ} = 3.3V +/- 0.3V)

Symbol	Parameter	Min	Max	Unit	Notes
C _{I1}	Input capacitance (A0 ~ A10, BA0)	-	TBD	pF	1, 3
C _{I2}	Input capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, CKE)	-	TBD	pF	1, 3
C _{I3}	Input capacitance (CK0, CK1, CK2, CK3)	-	TBD	pF	1, 3
C _{I4}	Input capacitance ($\overline{\text{S0}}$, $\overline{\text{S2}}$)	-	TBD	pF	1, 3
C _{I5}	Input capacitance (DQMB1)	-	TBD	pF	1, 3
C _{I6}	Input capacitance (DQMB0, 2, 3, 4, 5, 6, 7)	-	TBD	pF	1, 3
C _{I/O}	I/O capacitance (DQ0 ~ 63, CB0 ~ 7)	-	TBD	pF	1, 2, 3

- Note :
1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
 2. DQMB = V_{IH} to disable Dout.
 3. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 70C, Vcc, Vccq = 3.3 V +/- 0.3 V, Vss, Vssq = 0 V)

Parameter	Symbol	- 75		- 8		- 7K		- 7J		- 10K		Unit	Notes	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
System clock cycle time	(CL=2)	t _{CK}	12	-	12	-	10	-	15	-	15	-	ns	1
	(CL=3)	t _{CK}	7.5	-	8	-	10	-	10	-	10	-		
CLK high pulse width	t _{CKH}	2.5	-	3	-	3	-	3	-	3	-	ns	1	
CLK low pulse width	t _{CKL}	2.5	-	3	-	3	-	3	-	3	-	ns	1	
Access time from CLK	(CL=2)	t _{AC}	-	6	-	6	-	6	-	8	-	9	ns	1, 2
	(CL=3)	t _{AC}	-	5.4	-	6	-	6	-	6	-	8		
Data-out hold time	t _{OH}	2.7	-	3	-	3	-	3	-	3	-	ns	1, 2	
CLK to Data-out low impedance	t _{LZ}	1.5	-	2	-	2	-	2	-	2	-	ns	1, 2, 3	
CLK to Data-out high impedance (CL = 2,3)	t _{HZ}	-	5.4	-	6	-	6	-	6	-	7	ns	1, 4	
Data-in setup time	t _{DS}	1.5	-	2	-	2	-	2	-	2	-	ns	1	
Data-in hold time	t _{DH}	0.8	-	1	-	1	-	1	-	1	-	ns	1	
Address setup time	t _{AS}	1.5	-	2	-	2	-	2	-	2	-	ns	1	
Address hold time	t _{AH}	0.8	-	1	-	1	-	1	-	1	-	ns	1	
CKE setup time	t _{CES}	1.5	-	2	-	2	-	2	-	2	-	ns	1, 5	
CKE setup time for power down exit	t _{CESP}	1.5	-	2	-	2	-	2	-	2	-	ns	1	
CKE hold time	t _{CEH}	0.8	-	1	-	1	-	1	-	1	-	ns	1	
Command ($\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, DQM) setup time	t _{CS}	1.5	-	2	-	2	-	2	-	2	-	ns	1	
Command ($\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, DQM) hold time	t _{CH}	0.8	-	1	-	1	-	1	-	1	-	ns	1	
Ref/Active to Ref/Active command period	t _{RC}	65	-	68	-	70	-	70	-	90	-	ns	1	
Active to Precharge command period	t _{RAS}	45	120000	48	120000	50	120000	50	120000	60	120000	ns	1	
Active command to column command (same bank)	t _{RCD}	20	-	20	-	20	-	20	-	30	-	ns	1	
Precharge to active command period	t _{RP}	20	-	20	-	20	-	20	-	30	-	ns	1	

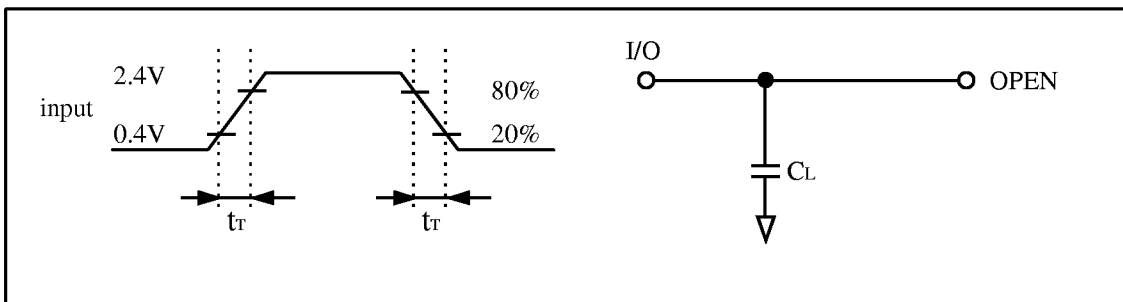
AC Characteristics (Ta = 0 to 70C, Vcc, Vccq = 3.3 V +/- 0.3 V, Vss, Vssq = 0 V)
(Continued)

Parameter	Symbol	- 75		- 8		- 7K		- 7J		- 10K		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write recovery or data-in to precharge lead time	t _{RWL}	7.5	-	8	-	10	-	10	-	15	-	ns	1
Active (a) to Active (b) command period	t _{RRD}	15	-	16	-	20	-	20	-	20	-	ns	1
Refresh period	t _{REF}	-	64	-	64	-	64	-	64	-	64	ms	
PLL Stabilization time	t _{STAB}	200	-	200	-	200	-	200	-	200	-	us	6

- Notes :
1. AC measurement assumes $t_r = 1ns$. Reference level for timing of input signals is 1.40V. If t_r is longer than 1ns, transition time compensation should be considered.
 2. Access time is measured at 1.40V. Load condition is $C_L = 50pF$ without termination.
 3. t_{LZ} (min) defines the time at which the outputs achieves the low impedance state.
 4. t_{HZ} (max) defines the time at which the outputs achieves the high impedance state.
 5. t_{CES} define CKE setup time to CKE rising edge except Power down exit command.
 6. The on-DIMM PLL must be given enough clock cycles to stabilize (t_{STAB}) before any operation can be guaranteed.

Test Condition

- Input and output-timing reference levels: 1.4V
- Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency

Parameter		-75		-8		-7K		-7J		-10K		Notes	
frequency(MHz)	Symbol	133	83	125	83	100	100	100	66	100	66		
t _{CK} (ns)		7.5	12	8	12	10	10	10	15	10	15		
Active command to column command (same bank)		t _{RCD}	3	2	3	2	2	2	2	2	3	2	1
Active command to active command (same bank)		t _{RC}	9	6	9	6	7	7	7	6	9	6	= [t _{RAS} + t _{RP}], 1
Active command to Precharge command (same bank)		t _{RAS}	6	4	6	4	5	5	5	4	6	4	1
Precharge command to active command (same bank)		t _{RP}	3	2	3	2	2	2	2	2	3	2	1
Write recovery or last data-in to Precharge command (same bank)		t _{RWL}	1	1	1	1	1	1	1	1	1	1	1
Active command to active command (different bank)		t _{RRD}	2	2	2	2	2	2	2	2	2	2	1
Self refresh exit time		t _{SREX}	1	1	1	2	1	1	1	2	2	2	
Last data in to active command (Auto Precharge, same bank)		t _{APW}	4	3	4	3	3	3	3	3	5	3	= [t _{RWL} + t _{RP}], 1
Self refresh exit to command input		t _{SEC}	9	6	9	6	7	7	7	6	9	6	= [t _{RC}]
Precharge command to high impedance	(CL=2)	t _{HZP}	-	2	-	2	2	2	-	2	-	2	
	(CL=3)	t _{HZP}	3	3	3	3	3	3	3	3	3	3	
Last data out to active command (auto Precharge) (same bank)		t _{APR}	1	1	1	1	1	1	1	1	1	1	
Last data out to Precharge (early Precharge)	(CL=2)	t _{EP}	-	-1	-	-1	-1	-1	-	-1	-	-1	
	(CL=3)	t _{EP}	-2	-2	-2	-2	-2	-2	-2	-2	-2	-2	
Column command to column command		t _{CCD}	1	1	1	1	1	1	1	1	1	1	
Write command to data in latency		t _{WCD}	0	0	0	0	0	0	0	0	0	0	
DQM to data in		t _{DD}	0	0	0	0	0	0	0	0	0	0	
DQM to data out		t _{DD}	2	2	2	2	2	2	2	2	2	2	
CKE to CLK disable		t _{CLE}	1	1	1	1	1	1	1	1	1	1	
Register set to active command		t _{RSA}	1	1	1	1	1	1	1	1	1	1	
CS̄ to command disable		t _{CDD}	0	0	0	0	0	0	0	0	0	0	
Power down exit to command input		t _{PEC}	1	1	1	1	1	1	1	1	1	1	

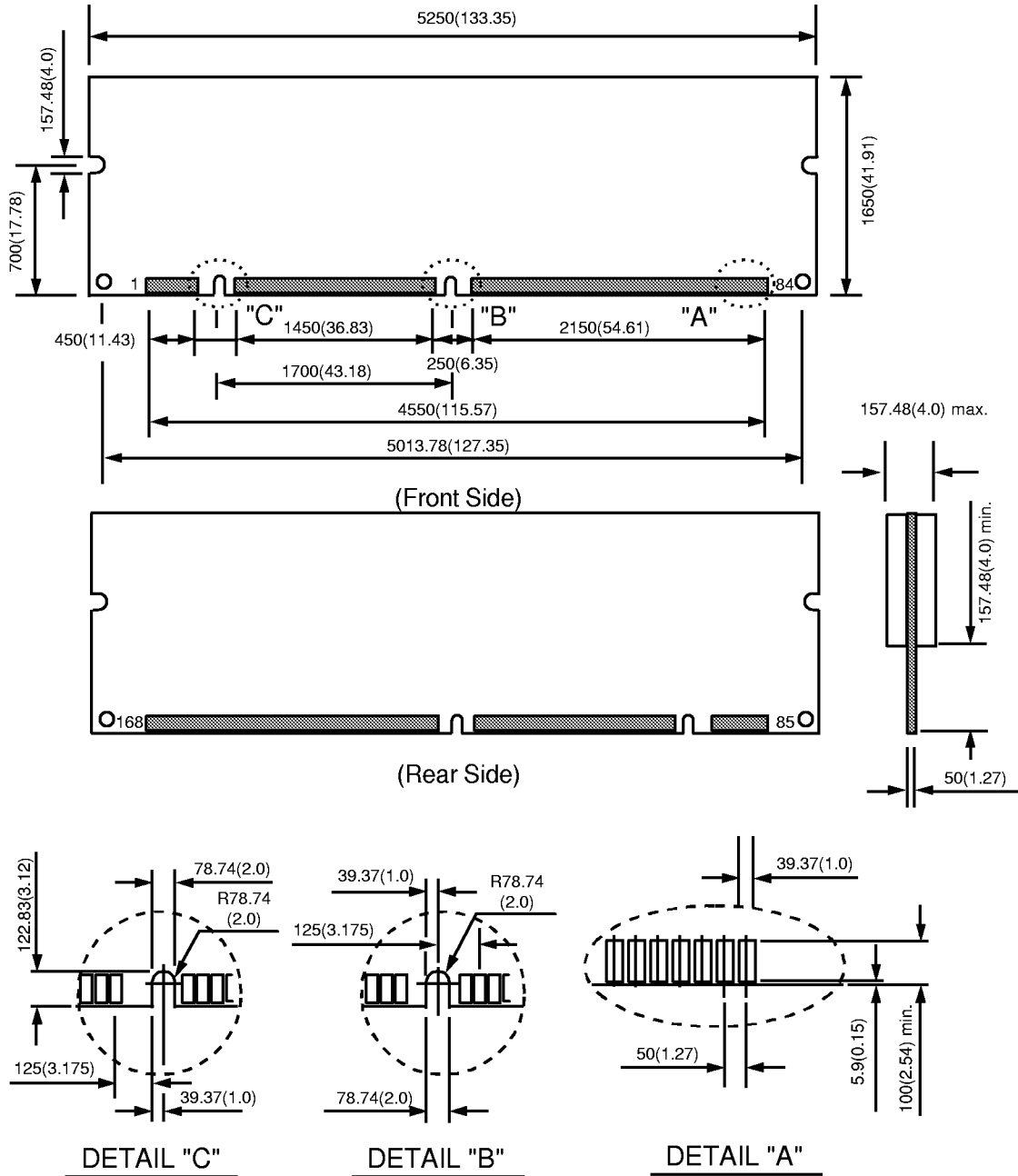
Relationship Between Frequency and Minimum Latency

Parameter		Symbol	-75		- 8		- 7K		- 7J		- 10K		Notes
frequency(MHz)			133	83	125	83	100	100	100	66	100	66	
t _{CK} (ns)			7.5	12	8	12	10	10	10	15	10	15	
Burst stop to output valid data hold	(CL=2)	I _{BSR}	-	1	-	1	1	1	-	1	-	1	
	(CL=3)	I _{BSR}	2	2	2	2	2	2	2	2	2	2	
Burst stop to output high impedance	(CL=2)	I _{BSH}	-	2	-	2	2	2	-	2	-	2	
	(CL=3)	I _{BSH}	3	3	3	3	3	3	3	3	3	3	
Burst stop to write data ignore		I _{BSW}	0	0	0	0	0	0	0	0	0	0	

Notes : 1. I_{RCD} to I_{RRD} are recommended value.

Package Dimension

Unit: mil (mm)
 * (1 mil = 1/1000 inches)



NOTE : 1. Tolerances on all dimensions +/-5 (0.127) unless otherwise specified.
 2. Thickness includes Plating and / or Metallization.