2-W Stereo Audio Power Amplifier with Four Selectable Gain Settings

DESCRIPTOIN

The EUA5312 is a stereo audio power amplifier. When driving 1 W into 8–Ω speakers, the EUA5312 has less than 0.8% THD+N across its specified frequency range. Included within this device is integrated depop circuitry that virtually eliminates transients that cause noise in the speakers.

Amplifier gain is internally configured and controlled by way of two terminals (GAIN0 and GAIN1). BTL gain settings of 6 dB, 10 dB, 15.6 dB, and 21.6 dB are provided, while SE gain is always configured as 4.1 dB for headphone drive. An internal input MUX allows two sets of stereo inputs to the amplifier .The HP/$\overline{\text{LINE}}$ terminal allows the user to select which MUX input is active, regardless of whether the amplifier is in SE or BTL mode. In notebook applications, where internal speakers are driven as BTL and the line outputs (often headphone drive) are required to be SE, the EUA5312 automatically switches into SE mode when the SE/$\overline{\text{BTL}}$ input is activated, and this reduces the gain to 4.1 dB.

The EUA5312 consumes only 6mA of supply current during normal operation.

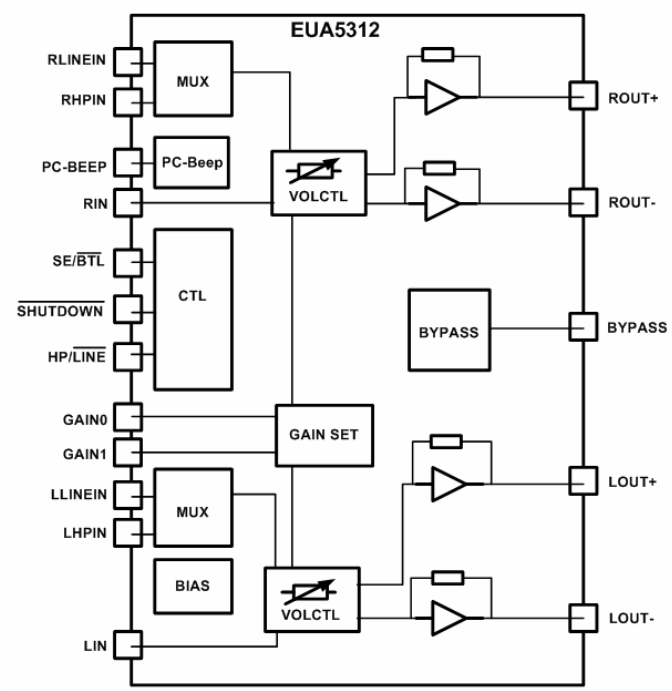
FEATURES

- 2W per Channel Output Power Into 3-Ω Load
- Internal Gain Control, Which Eliminates External Gain-Setting Components
- Input MUX Select Terminal
- PC-Beep Input
- Depop Circuitry Integrated
- Two Input Modes Allowable with Single-Ended or Fully Differential Input
- Low Supply Current and Shutdown Current
- Thermal Shutdown Protection
- TSSOP-24 with Thermal Pad
- RoHS Compliant and 100% Lead (Pb)-Free

APPLICATIONS

- Notebook Computers
- Multimedia Monitors
- Digital Radios and Portable TVs

Block Diagram



Typical Application Circuit

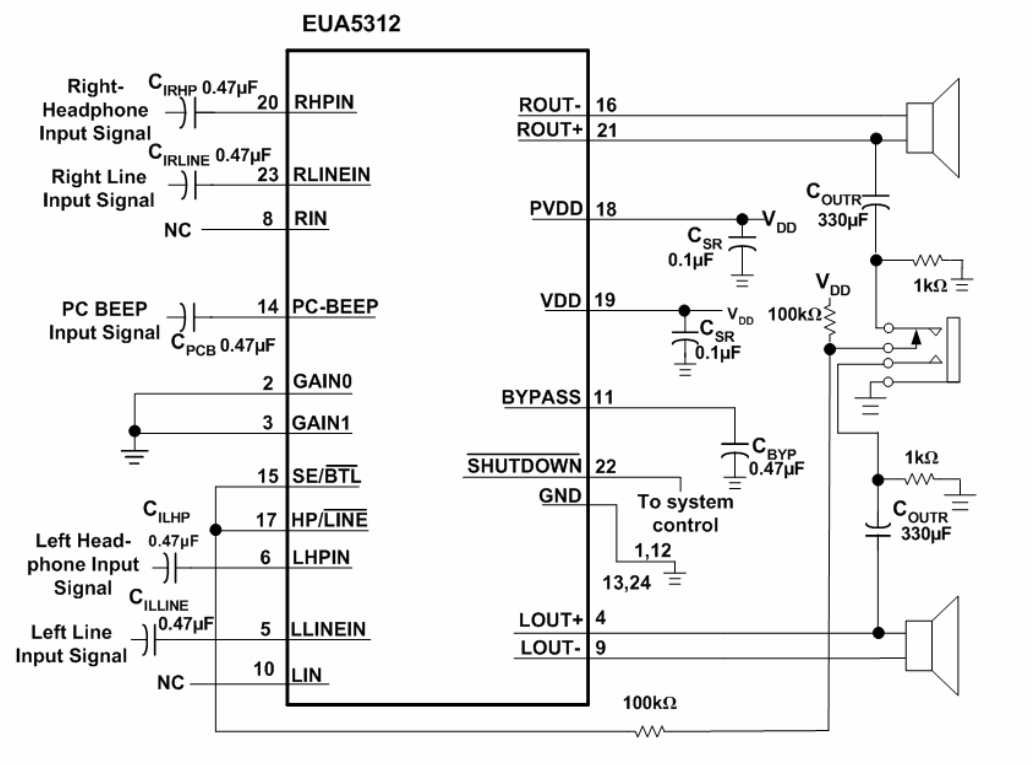


Figure 1. Application circuit using single-ended inputs and input MUX

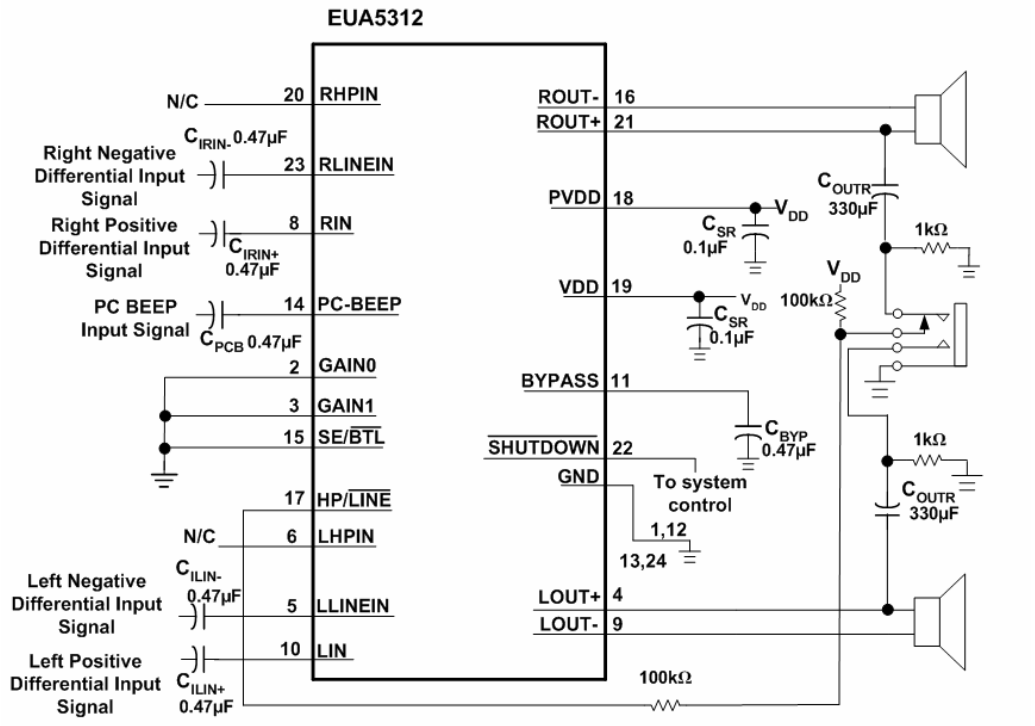
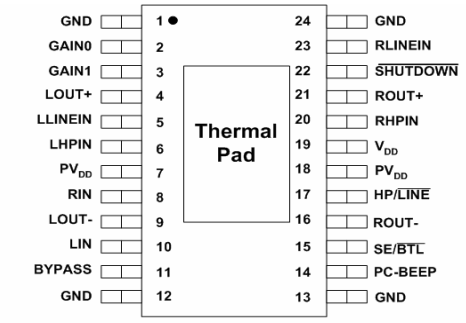


Figure 2. Application circuit using differential input

Pin Configurations

Package	Pin Configurations(Top View)
TSSOP-24 with a Thermal Pad exposure on the bottom of the package	

Pin Description

PIN	PIN	I/O	DESCRIPTION
BYPASS	11		Tap to voltage divider for internal mid-supply bias generator
GAIN0	2	I	Bit 0 of gain control
GAIN1	3	I	Bit 1 of gain control
GND	1,12 13,24		Ground connection for circuitry. Connected to thermal pad.
LHPIN	6	I	Left channel headphone input, selected when SE/$\overline{\text{BTL}}$ is held high.
LIN	10	I	Common left input for fully differential input. AC ground for single-ended inputs.
LLINEIN	5	I	Left channel line input, selected when SE/$\overline{\text{BTL}}$ is held low.
LOUT+	4	O	Left channel positive output in BTL mode and positive output in SE mode.
LOUT-	9	O	Left channel negative output in BTL mode and high-impedance in SE mode.
PC-BEEP	14	I	The input for PC Beep mode. PC-BEEP is enabled when a > 1-V (peak-to-peak) square wave is input to PC-BEEP or PCB ENABLE is high.
HP/$\overline{\text{LINE}}$	17	I	HP/$\overline{\text{LINE}}$ is the input MUX control input. When the HP/$\overline{\text{LINE}}$ terminal is held high, the headphone inputs (LHPIN or RHPIN [6, 20]) are active. When the HP/$\overline{\text{LINE}}$ terminal is held low, the line BTL inputs (LLINEIN or RLINEIN [5, 23]) are active.
PV_{DD}	7,18	I	Power supply for output stage.
RHPIN	20	I	Right channel headphone input, selected when SE/$\overline{\text{BTL}}$ is held high
RIN	8	I	Common right input for fully differential input. AC ground for single-ended inputs.
RLINEIN	23	I	Right channel line input, selected when SE/$\overline{\text{BTL}}$ is held low.
ROUT+	21	O	Right channel positive output in $\overline{\text{BTL}}$ mode and positive output in SE mode.
ROUT-	16	O	Right channel negative output in $\overline{\text{BTL}}$ mode and high-impedance in SE mode.
$\overline{\text{SHUTDOWN}}$	22	I	When held low, this terminal place the entire device, except PC-BEEP detect circuitry, in shutdown mode.
SE/$\overline{\text{BTL}}$	15	I	Input and output MUX control. When this terminal is held high, the LHPIN or RHPIN and SE output is selected. When this terminal is held low, the LLINEIN or RLINEIN and $\overline{\text{BTL}}$ output are selected.
V_{DD}	19	I	Analog V_{DD} input supply. This terminal needs to be isolated from PV_{DD} to achieve highest performance.

Ordering Information

Order Number	Package Type	Marking	Operating Temperature range
EUA5312QIR1	TSSOP 24	xxxx EUA5312	-40 °C to 85°C
EUA5312QIR0	TSSOP 24	xxxx EUA5312	-40 °C to 85°C
EUA5312QIT1	TSSOP 24	xxxx EUA5312	-40 °C to 85°C
EUA5312QIT0	TSSOP 24	xxxx EUA5312	-40 °C to 85°C

EUA5312 □ □ □ □

Lead Free Code
1: Lead Free 0: Lead

Packing
R: Tape& Reel
T: Tube

Operating temperature range
I: Industry Standard

Package Type
Q: TSSOP

Absolute Maximum Ratings

- Supply voltage, V_{DD}---------- 6V
- Input voltage, V_I---------- –0.3 V to V_{DD} +0.3 V
- Continuous total power dissipation---------- internally limited (see Dissipation Rating Table)
- Operating free-air temperature range, T_A---------- –40°C to 85° C
- Operating junction temperature range, T_J ---------- - –40°C to 150°C
- Storage temperature range, T_{stg}---------- -- –65°C to 150°C
- Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds---------- 260°C

Dissipation Rating Table

PACKAGE	$T_A \leqq 25°C$	DERATING FACTOR	T_A = 70°C	T_A = 85°C
PWP	3.76 W	33.2 mW/°C	2.4096 W	2.1 W

Recommended Operating Conditions

		Min	Max	Unit
Supply voltage, V_{DD}		4.5	5.5	V
High-level input voltage, V_{IH}	SE/$\overline{\text{BTL}}$	4		V
	$\overline{\text{SHUTDOWN}}$	2		
Low-level input voltage, V_{IL}	SE/$\overline{\text{BTL}}$		3	V
	$\overline{\text{SHUTDOWN}}$		0.8	
Operating free-air temperature, T_A		-40	85	°C

Electrical Characteristics at Specified Free-air Temperature, VDD = 5V, T_A = 25°C

Symbol	Parameter	Conditions	EUA5312			Unit
			Min.	Typ.	Max.	
$\lvert V_{OO} \rvert$	Output offset voltage (measured differentially)	V_I =0V, A_V =2 V/V			30	mV
PSRR	Power supply rejection ratio	V_{DD}= 4 V to 5 V		68		dB
$\lvert I_{IH} \rvert$	High-level input current	V_{DD}=5.5 V, V_I = V_{DD}			1	µA
$\lvert I_{IL} \rvert$	Low-level input current	V_{DD}=5.5 V, V_I = 0V			1	µA
I_{DD}	Supply current	BTL mode		6	10	mA
		SE mode		3	5	
$I_{DD(SD)}$	Supply current, shutdown mode			120	300	µA

Operating Characteristics, VDD = 5V, T_A = 25°C, R_L = 8Ω, Gain =-2V/V, BTL mode

Symbol	Parameter	Conditions		EUA5312			Unit
				Min.	Typ.	Max.	
P_O	Output power	THD=1%, RL=4Ω, f=1kHz			1.9		W
THD+N	Total harmonic distortion plus noise	P_O=1W, f=20 Hz to 15 kHz			0.75%		
B_{OM}	Maximum output power bandwidth	THD=5%			＞15		kHz
	Supply ripple rejection ratio	f =1kHz, $C_{(BYP)}$=0.47μF	BTL mode		68		dB
SNR	Signal-to-noise ratio				91		dB
V_n	Noise output voltage	$C_{(BYP)}$=0.47μF, f= 20 kHz to 20 kHz	BTL mode		71		μV_{RMS}
			SE mode		44		

Typical Characteristics (Table of Graphs)

No	Item	Figure
1	THD+N vs. Output Power	3,6,7,8,11,12,13,16, 17,18,20,23
2	THD+N vs. Output Frequency	4,5,9,10,14,15,19,22,
3	Output Noise Voltage vs. Frequency	21
4	Supply Ripple Rejection Ratio vs. Frequency	24,25
5	Crosstalk vs. Frequency	26,27
6	Shutdown Attenuation	28
7	Signal to noise ratio vs. Frequency	29
8	Closed Loop Response	30,31,32,33
9	Output Power vs. Load Resistance	34,35
10	Power Dissipation vs. Output Power	36,37

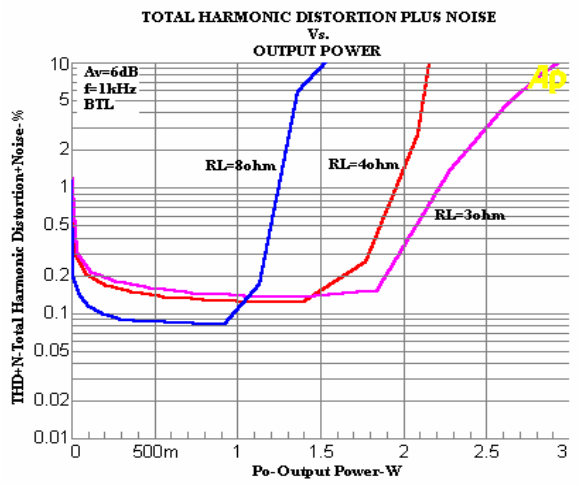


Figure 3

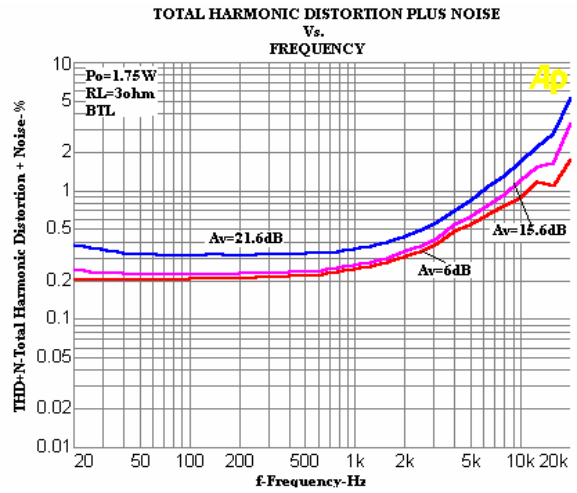


Figure 4

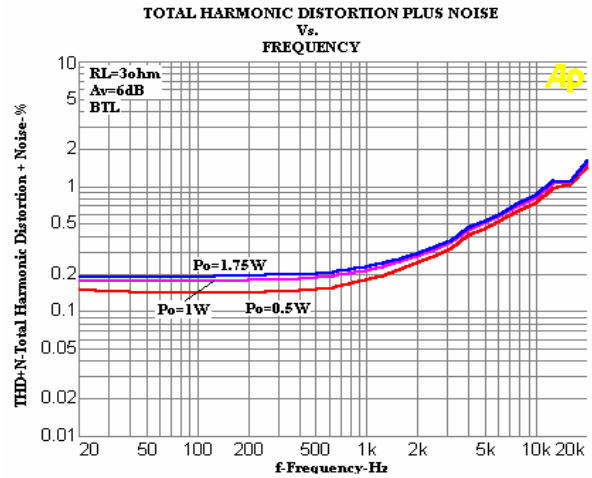


Figure 5

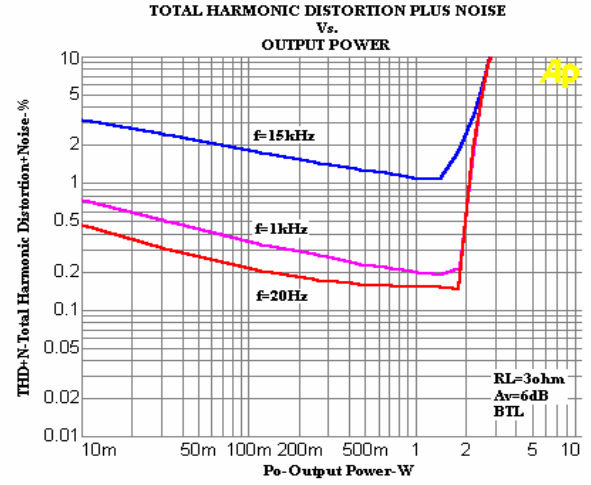


Figure 6

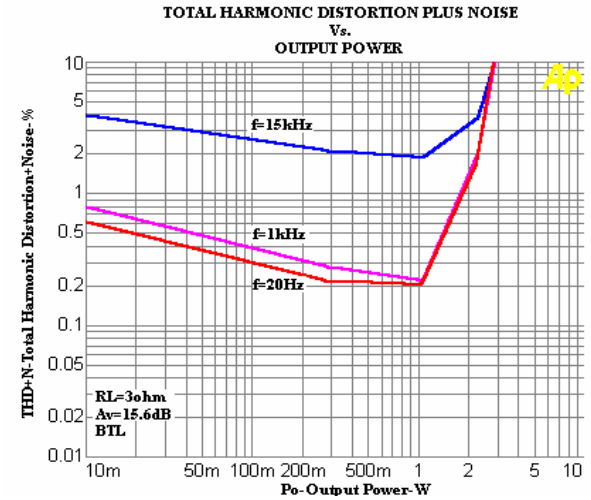


Figure 7

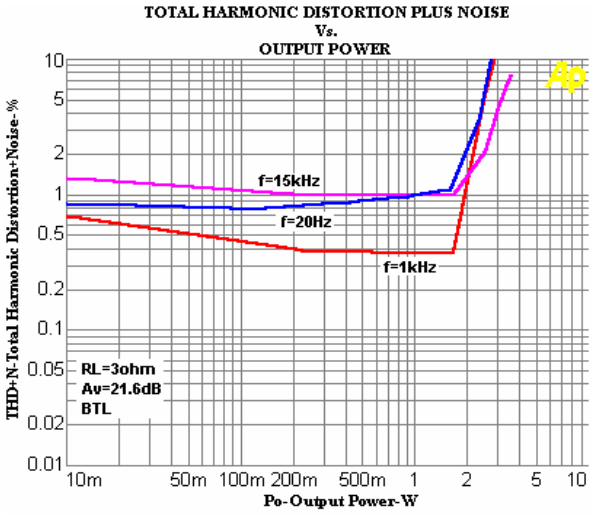


Figure 8

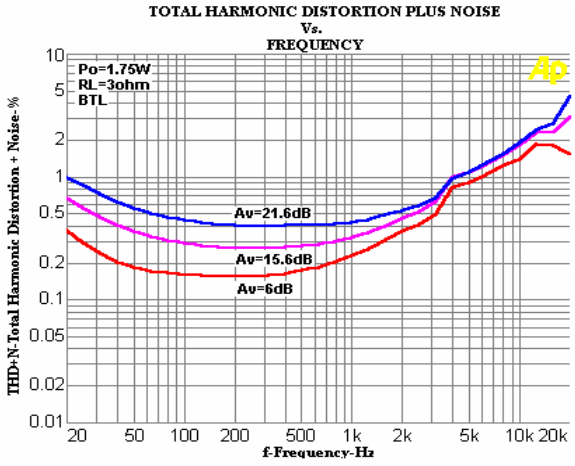


Figure 9

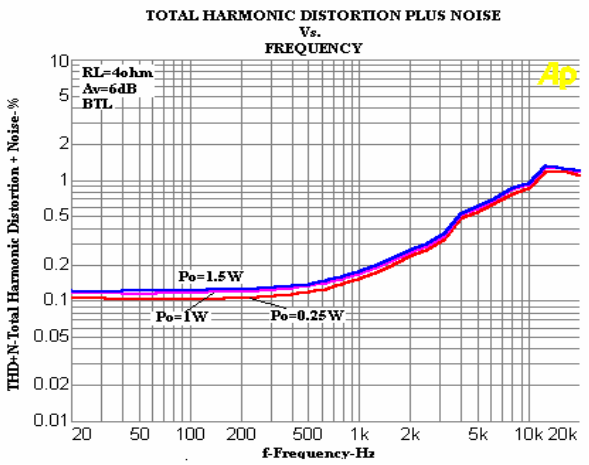


Figure 10

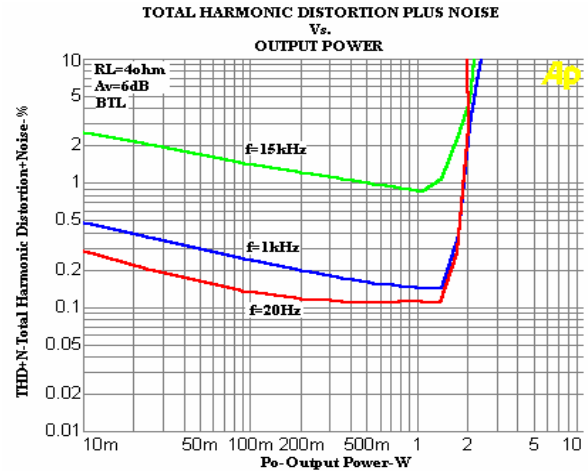


Figure 11

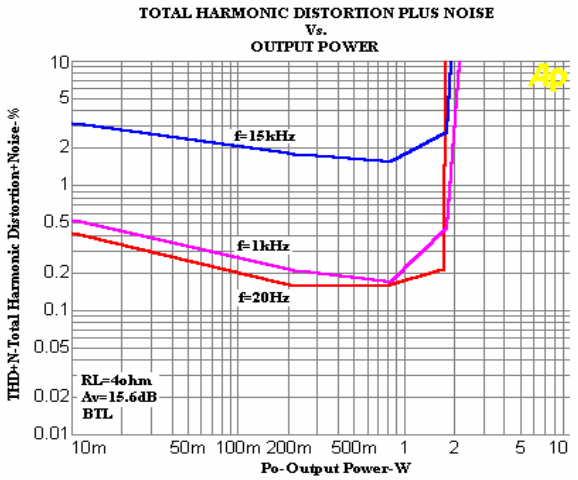


Figure 12

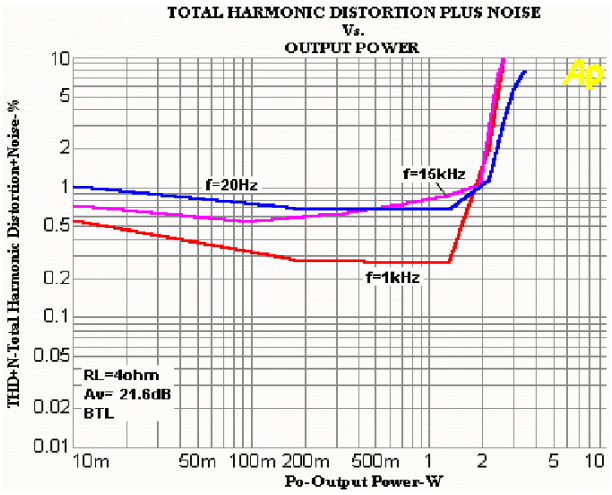


Figure 13

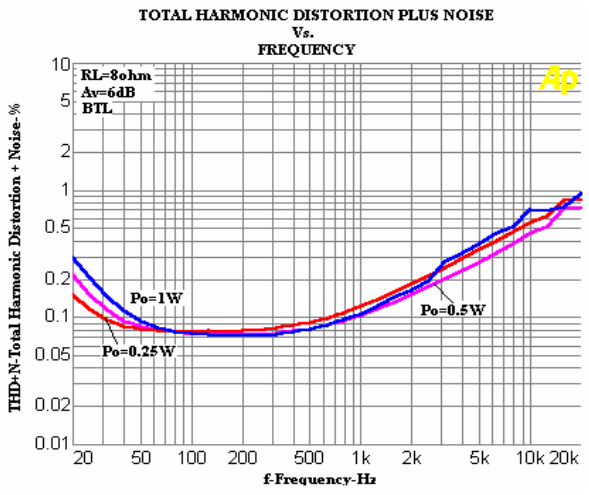


Figure 14

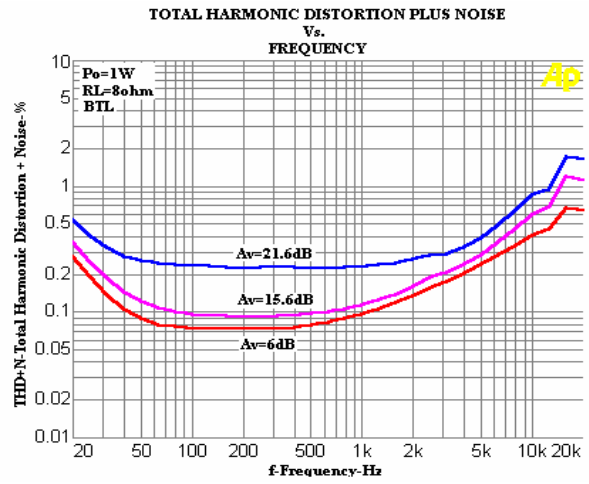


Figure 15

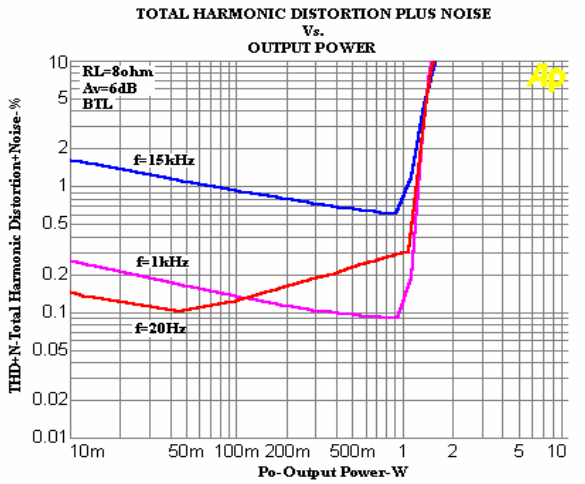


Figure 16

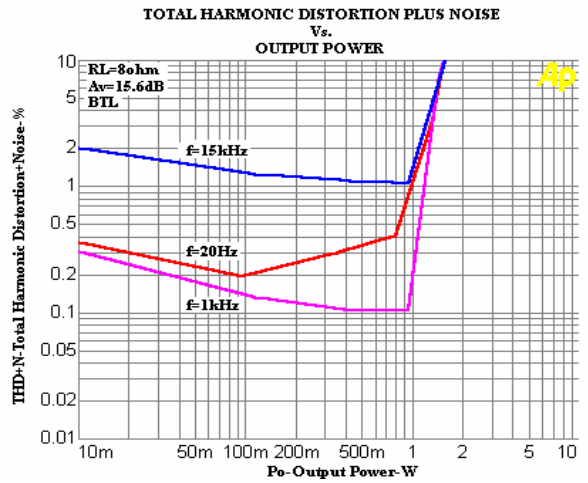


Figure 17

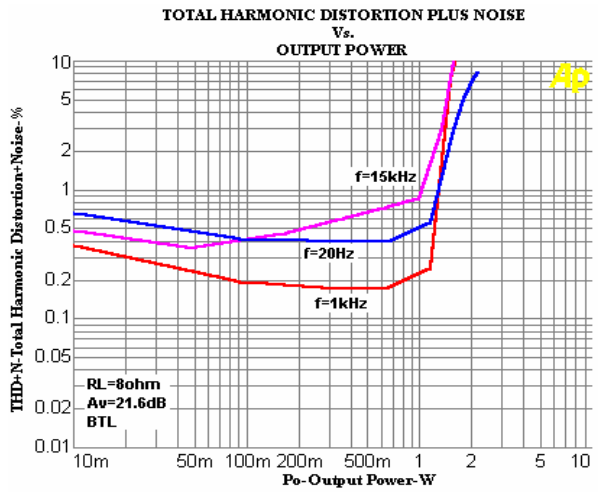


Figure 18

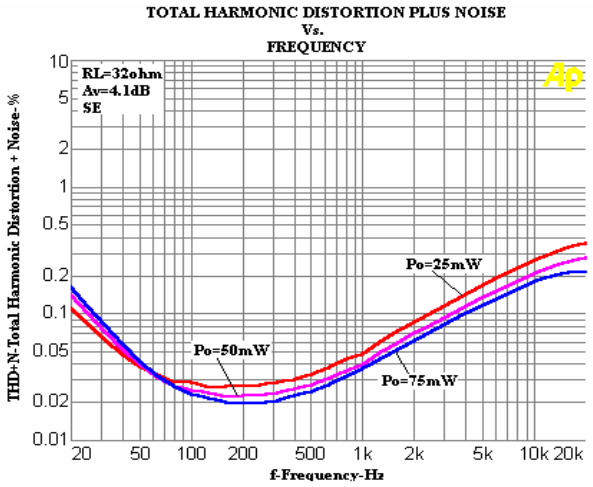


Figure 19

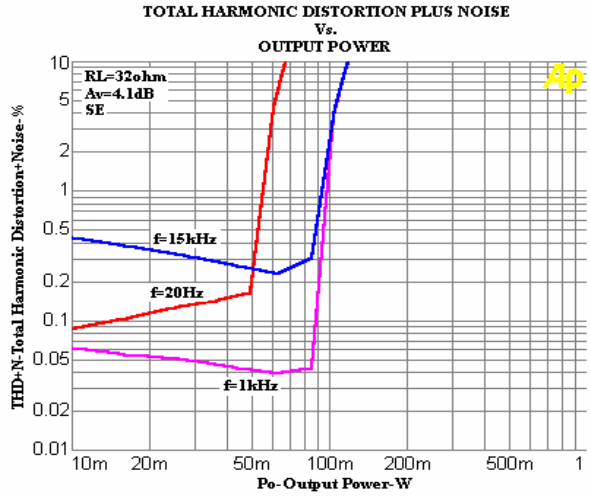


Figure 20

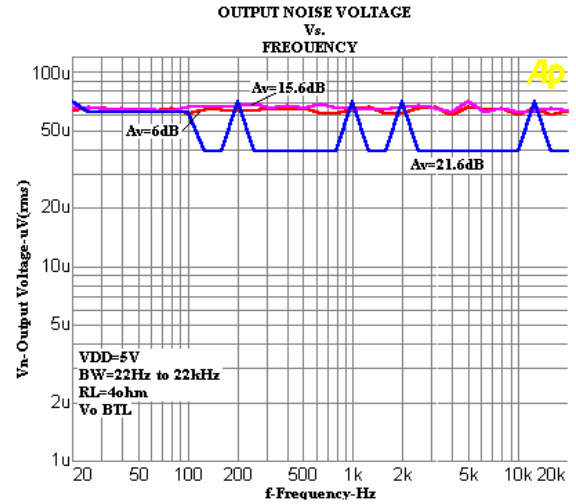


Figure 21

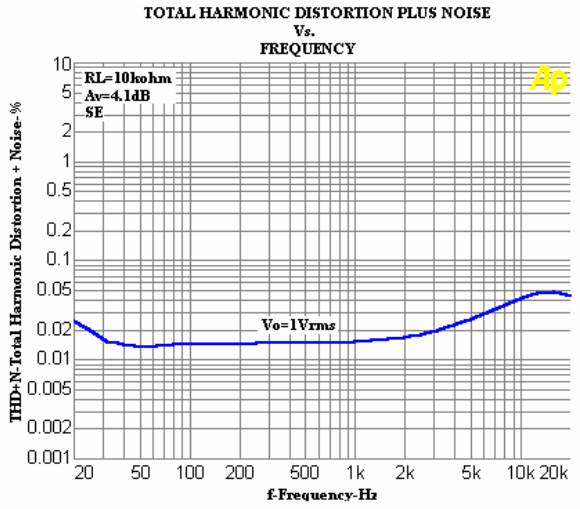


Figure 22

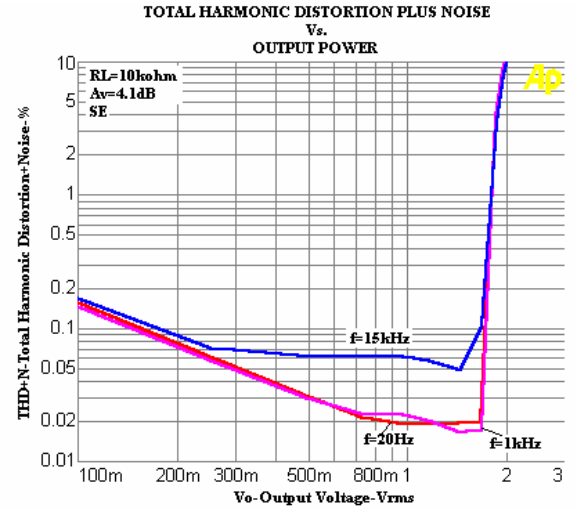


Figure 23

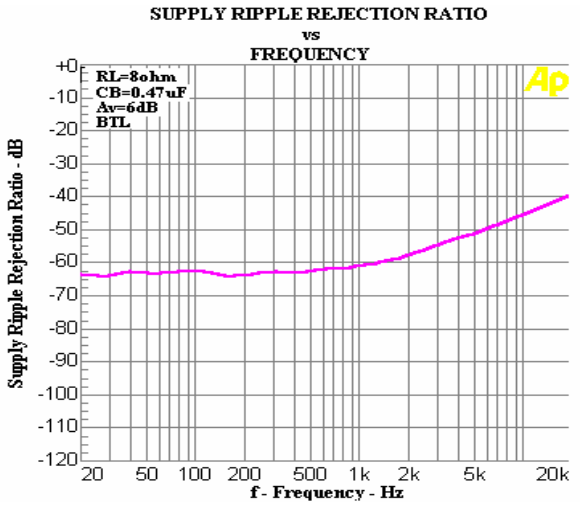


Figure 24

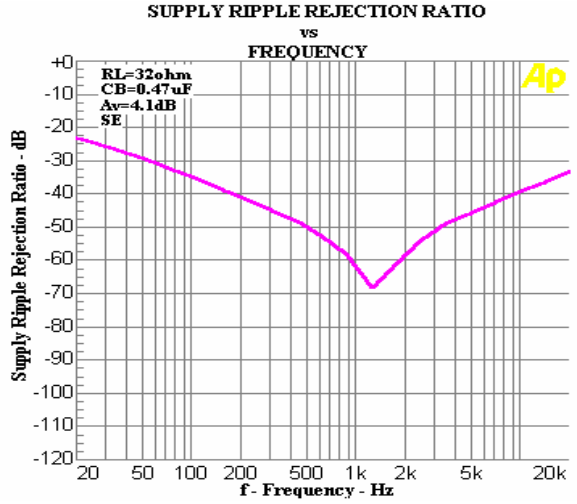


Figure 25

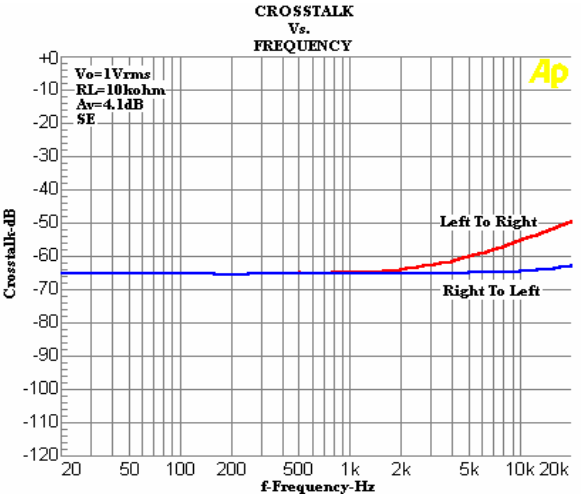


Figure 26

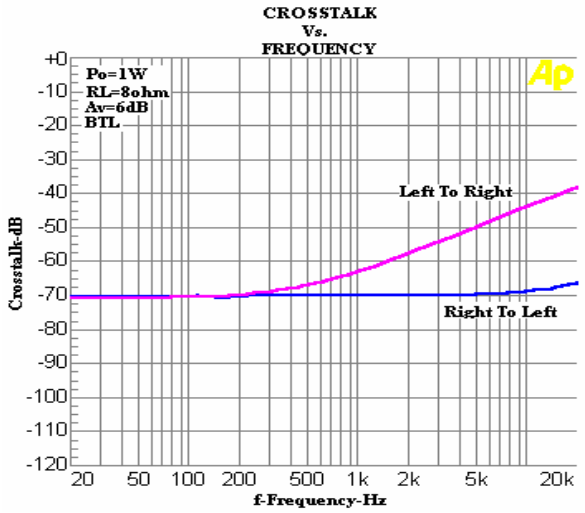


Figure 27

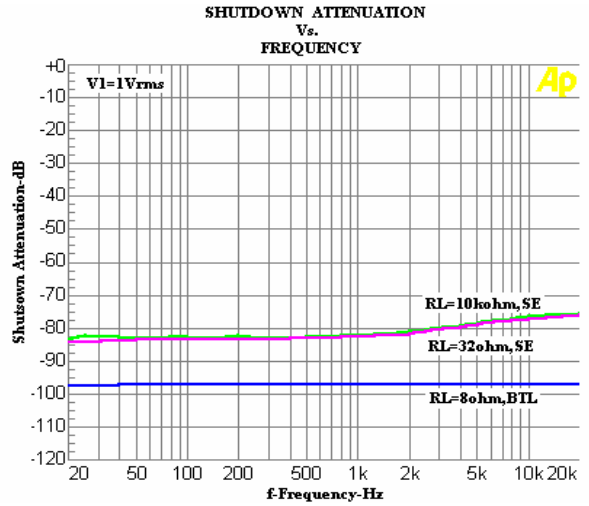


Figure 28

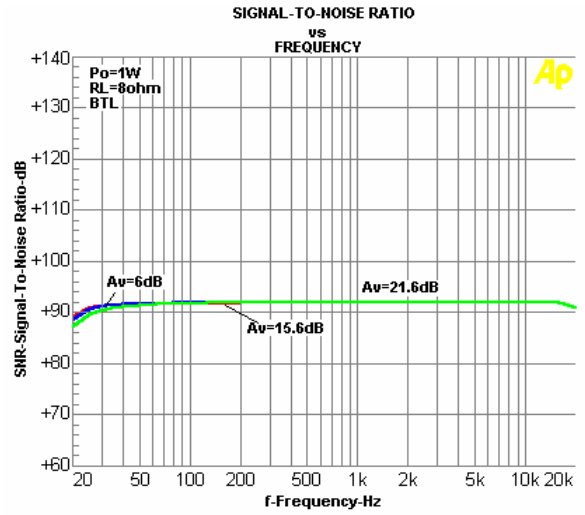


Figure 29

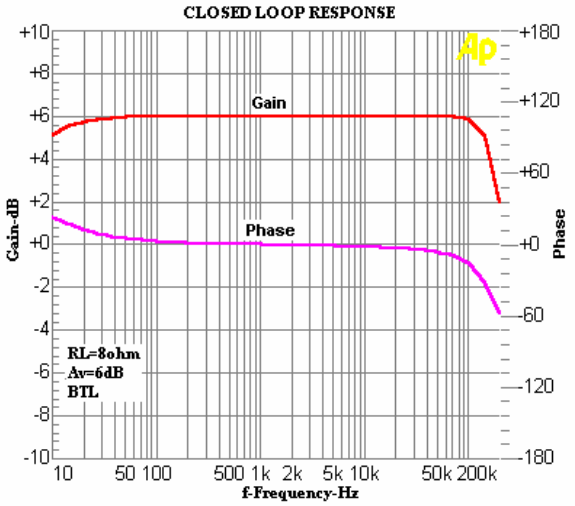


Figure 30

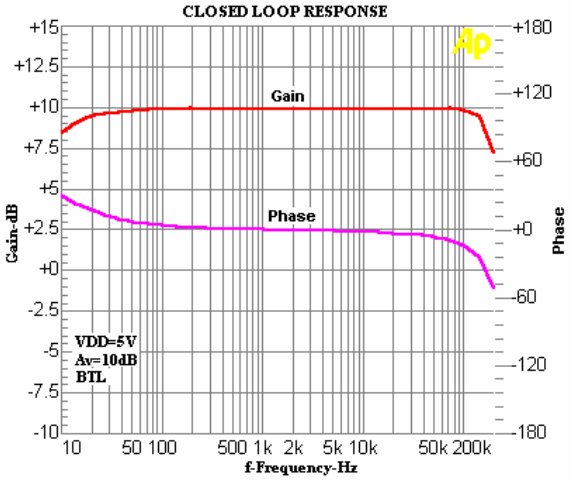


Figure 31

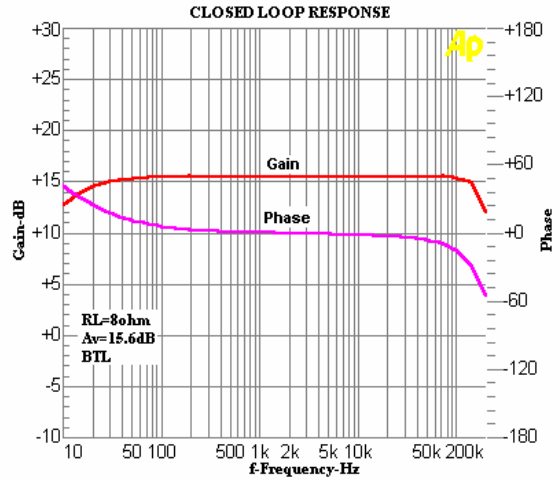


Figure 32

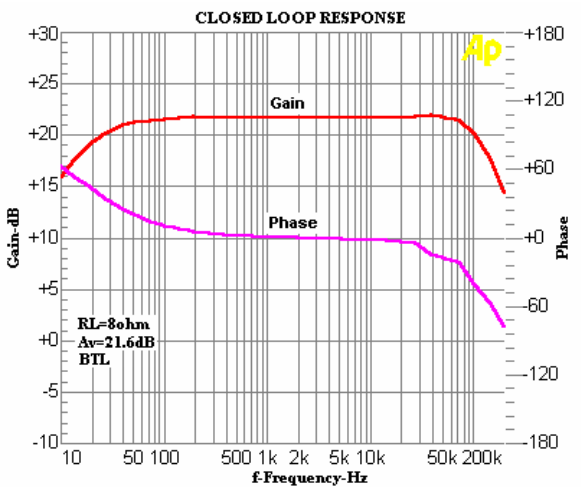


Figure 33

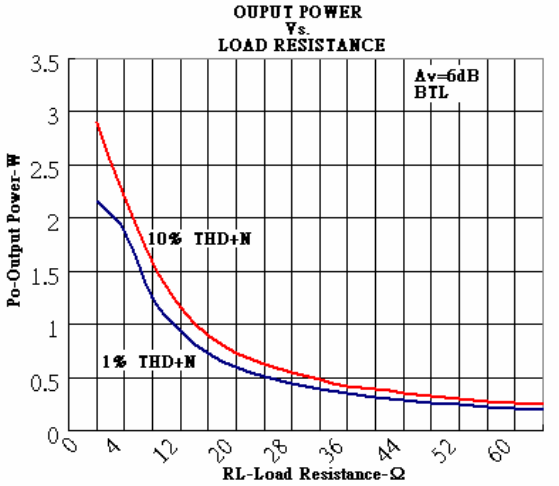


Figure 34

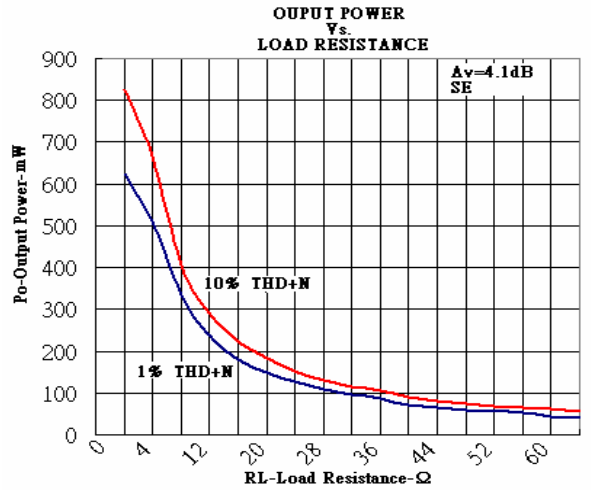


Figure 35

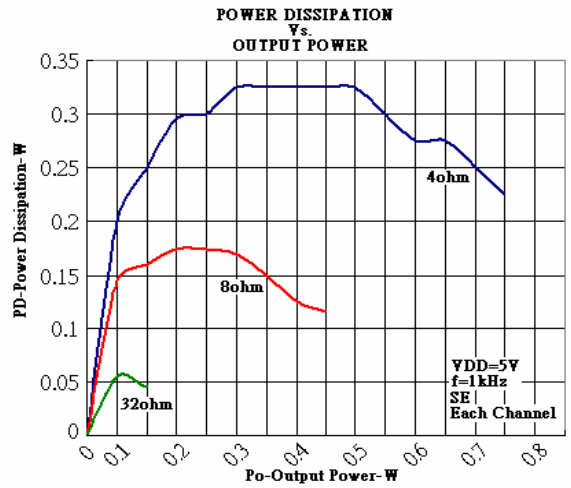


Figure 36

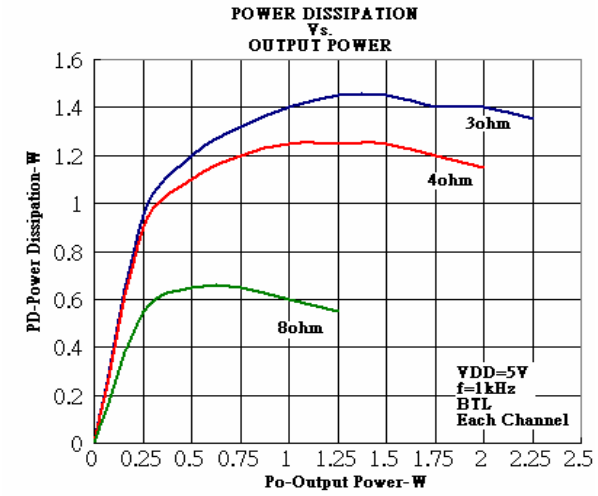


Figure 37

Application Information

Gain Setting

The gain of the EUA5312 is set by two input terminals, Gain0 and Gain1.The gains listed in Table 1 are realized by changing the taps on the input resistors inside the amplifier.

Table 1.Gain Setting

GAIN0	GAIN1	SE/$\overline{BTL}$	$A_{V(inv)}$	Z_I
0	0	0	6dB	90kΩ
0	1	0	10dB	70kΩ
1	0	0	15.6dB	45kΩ
1	1	0	21.6dB	25kΩ
X	X	1	4.1dB	

Input Resistance

Each gain setting is achieved by varying the input resistance of the amplifier, which can range from its smallest value to over 6 times that value. As a results, if a single capacitor is used in the input high pass filter, the –3 dB or cut off frequency will also change by over 6 times. If an additional resistor is connected from the input pin of the amplifier to ground, as shown in the figure below, the variation of the cut-off frequency will be much reduced.

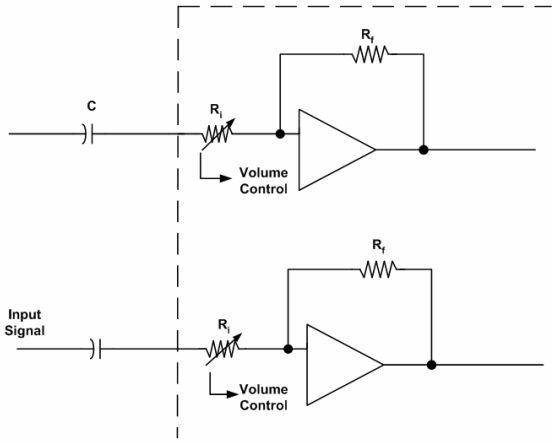


Figure 38. Input Resistor

The-3dB frequency can be calculated using equation 1:

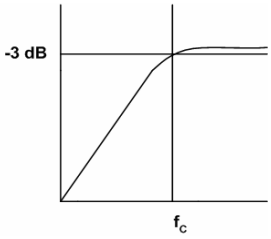
$$f_{-3dB} = \frac{1}{2\pi C (R \parallel R_i)} \quad \text{---------- (1)}$$

If the filter must be more accurate, the value of the capacitor should be increased while the value of the resistor to ground should be decreased. In addition, the order of the filter could be increased.

Input Capacitor, C_i

In the typical application an input capacitor, C_i, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_i and the input impedance of the amplifier, Z_i, from a high-pass filter with the corner frequency determined in equation 2.

$$f_{c(highpass)} = \frac{1}{2\pi Z_i C_i} \quad \text{----------(2)}$$



The value of C_i is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where Z_i is 710kΩ and the specification calls for a flat bass response down to 40Hz. Equation 2 is reconfigured as equation 3.

$$C_i = \frac{1}{2\pi Z_i f_C} \quad \text{---------- (3)}$$

In this example, C_i is 5.6nF so one would likely choose a value in the range of 5.6nF to 1μF. A further consideration for this capacitor is the leakage path from the input source through the input network (C_i) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low- leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application.

Decoupling Capacitor, (C_S)

The EUA5312 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. (ESR) ceramic capacitor, typically 0.1µF placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10µF or greater placed near the audio power amplifier is recommended.

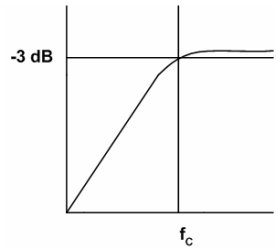
Bypass Capacitor, (C_B)

The bypass capacitor, C_B, is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, C_B determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N. Bypass capacitor, C_B, values of 0.47µF to 1µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

Output Coupling Capacitor, (C_C)

For general signal-supply SE configuration, the output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 4.

$$f_{c(high)} = \frac{1}{2\pi R_L C_C} \text{ ---------- (4)}$$



The main disadvantage, from a performance standpoint, is the load impedances are typically small, which drives the low-frequency corner higher, degrading the bass response. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 330µF is chosen and loads vary from 3Ω, 4Ω, 8Ω, 32Ω, 10kΩ, to 47kΩ. Table 2 summarizes the frequency response characteristics of each configuration.

Table2. Common Load Impedances vs Low Frequency Output characteristics in SE Mode

R_L	C_C	Lowest Frequency
3Ω	330µF	161Hz
4Ω	330µF	120Hz
8Ω	330µF	60Hz
32Ω	330µF	15Hz
10000Ω	330µF	0.05Hz
47000Ω	330µF	0.01Hz

As Table 2 indicates, most of the bass response is attenuated into a 4-Ω load and 8-Ω load is adequate, headphone response is good, and drive into line level inputs (a home stereo for example) is exceptional.

Using Low- ESR Capacitors

Low- ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

Bridged-Tied Load Versus Single-Ended Mode

Figure 39 show a Class-AB audio power amplifier (APA) in a BTL configuration. The EUA5312 BTL amplifier consists of two Class-AB amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration, but initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging $2\times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance(see equation 5)

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}} \qquad \text{Power} = \frac{V_{(rms)}^{2}}{R_L} \qquad \text{------(5)}$$

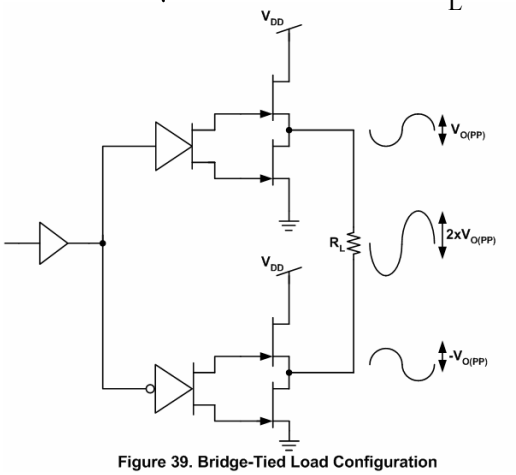


Figure 39. Bridge-Tied Load Configuration

In a typical computer sound channel operating at 5V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 250 mW to 1W. In sound power that is a 6-dB improvement—which is loudness that can be heard. In addition to increased power there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 40.

A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33µF to 1000µF) so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high pass filter network created with the speaker impedance and the coupling capacitance and is calculated with equation 6.

$$f_C = \frac{1}{2\pi R_L C_C} \text{----------(6)}$$

For example, a 68µF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

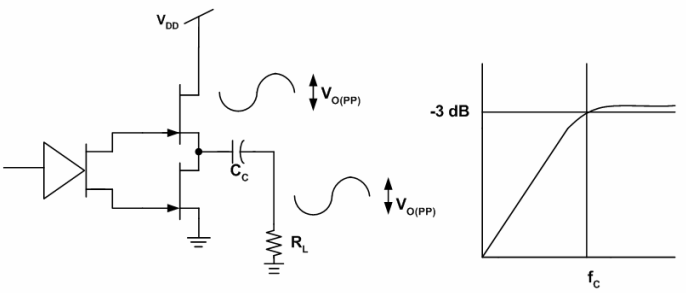


Figure 40. Single-Ended Configuration and Frequency Response

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4 ˟ the output power of the SE configuration. Internal dissipation versus output power is discussed further in the crest factor and thermal considerations section**.**

Single-Ended Operation

In SE mode the load is driven from the primary amplifier output for each channel (OUT+, terminals 21 and 4). The amplifier switches single-ended operation when the SE/$\overline{\text{BTL}}$ terminal is held high. This puts the negative outputs in a high-impedance state, and reduces the amplifier's gain to 1V/V.

Input MUX Operation

The input MUX allows two separate inputs to be applied to the amplifier. This allow the designer to choose which input is active independent of the state of the SE/$\overline{\text{BTL}}$ terminal. When the HP/$\overline{\text{LINE}}$ terminal is held high, the headphone inputs are active. When the HP/$\overline{\text{LINE}}$ terminal is held low, the line BTL inputs are active.

SE/$\overline{\text{BTL}}$ Operation

The ability of the EUA5312 to easily switch between BTL and SE modes is one of its most important cost saving features. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated. Internal to the EUA5312 , two separate amplifiers drive OUT+ and OUT- .The SE/$\overline{\text{BTL}}$ input (terminal 15) control the operation of the follower amplifier that drives LOUT- and ROUT- (terminals 9 and 16).When SE/$\overline{\text{BTL}}$ is held low, the amplifier is on and the EUA5312 is in the BTL mode. When SE/$\overline{\text{BTL}}$ is held high, the OUT- amplifiers are in a high output impedance state, which configures the EUA5312 as an SE driver from LOUT+ and ROUT+ (terminals 4 and 21). I_{DD} is reduced by approximately one-half in SE mode. Control of the SE/$\overline{\text{BTL}}$ input can be from a logic-level CMOS source or, more typically, from a resistor divider network as shown in Figure 41.

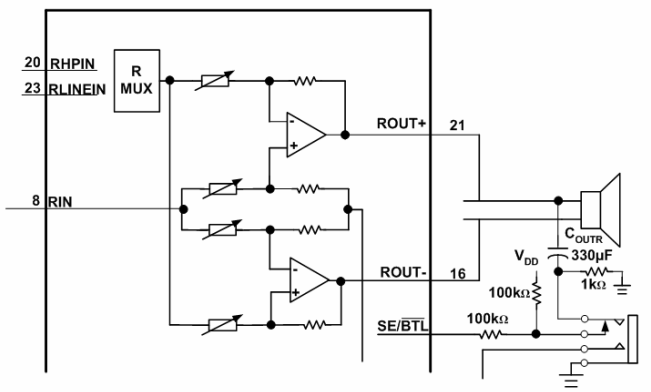


Figure 41. Resistor Divider Network Circuit

Using a readily available 1/8-in. (3.5mm) stereo headphone jack, the control switch is closed when no plug is inserted. When closed the 100-kΩ /1-kΩ divider pulls the SE/$\overline{\text{BTL}}$ input low. When a plug is inserted, the 1-kΩ resistor is disconnected and the SE/$\overline{\text{BTL}}$ input is pulled high. When the input goes high, the OUT- amplifier is shut down causing the speaker to mute(virtually open-circuits the speaker).The OUT+ amplifier then drives through the output capacitor (C_O) into the headphone jack.

PC BEEP Operation

The PC BEEP input allows a system beep to be sent directly from a computer through the amplifier to the speakers with few external components. The input is activated automatically. When the PC BEEP input is active, both of the LINEIN and HPIN inputs are deselected and both the left and right channels are driven in BTL mode with the signal from PC BEEP. The gain from the PC BEEP input to the speakers is fixed at 0.3V/V and is independent of the volume setting. When the PC BEEP input is deselected, the amplifier will return to the previous operating mode and volume setting. Furthermore, if the amplifier is in shutdown mode, activating PC BEEP will take the device out of shutdown and output the PC BEEP signal, then return the amplifier to shutdown mode.

The preferred input signal is a square wave or pulse train with an amplitude of 1 V_{PP} or greater. When the signal is no longer detected, the amplifier will return to its previous operating mode and volume setting.

If it is desired to ac-couple the PC BEEP input, the value of the coupling capacitor should be chosen to satisfy equation 7:

$$C_{PCB} \geq \frac{1}{2\pi f_{PCB}(100k\Omega)} \text{--------(7)}$$

The PC BEEP input can also be dc- coupled to avoid using this coupling capacitor. The pin normally sits at midrail when no signal is present.

Shutdown Modes

The EUA 5312 employs a shutdown mode of operation designed to reduce supply current, I_{DD}, to the absolute minimum level during periods of nonuse for battery-power conservation. The $\overline{\text{SHUTDOWN}}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs to mute and the amplifier to enter a low-current state, I_{DD}=150µA. $\overline{\text{SHUTDOWN}}$ should never be left unconnected because amplifier operation would be unpredictable.

Table 6 . HP/$\overline{\text{LINE}}$, SE/$\overline{\text{BTL}}$, and Shutdown Function

Inputs			Amplifier State	
HP/$\overline{\text{LINE}}$	SE/$\overline{\text{BTL}}$	$\overline{\text{SHUTDOWN}}$	INPUT	OUTPUT
X	X	Low	X	Mute
Low	Low	High	Line	BTL
Low	High	High	Line	SE
High	Low	High	HP	BTL
High	High	High	HP	SE

X= Do not care

Thermal Pad Considerations

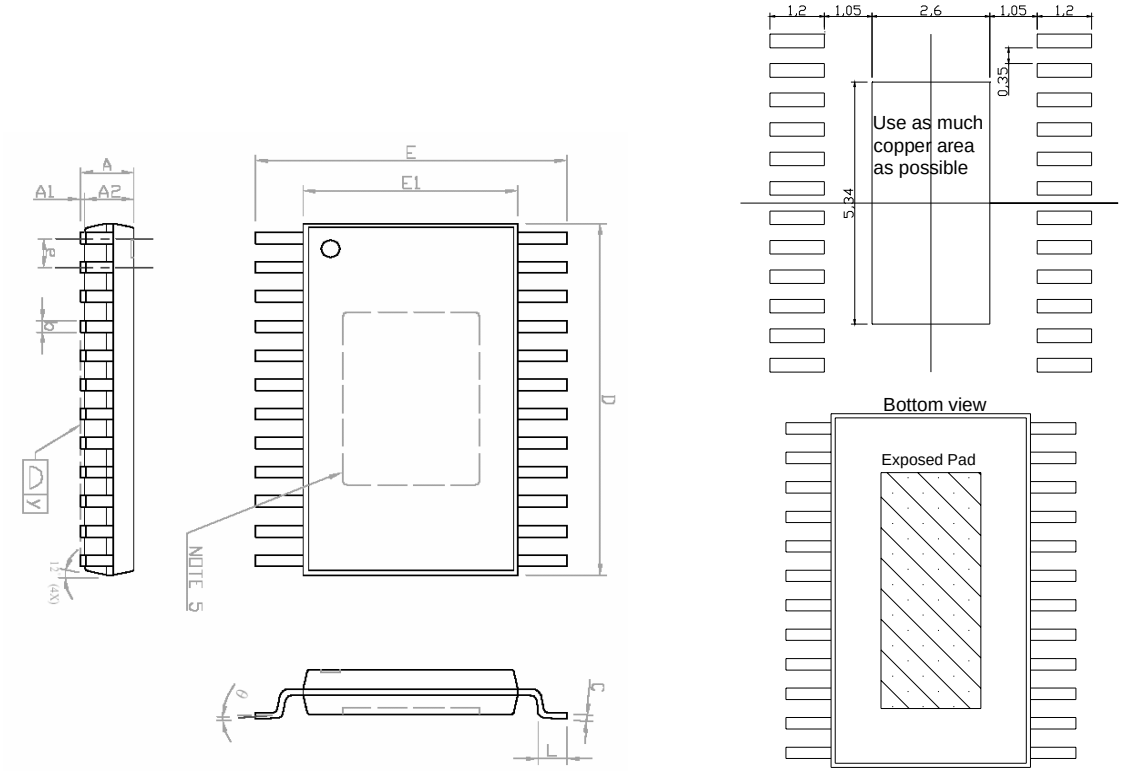
The thermal pad must be connected to ground. The package with thermal pad of the EUA5312 requires special attention on thermal design. If the thermal design issues are not properly addressed, the EUA5312 will go into thermal shutdown when driving a heavy load.

The thermal pad on the bottom of the EUA5312 should be soldered down to a copper pad on the circuit board. Heat can be conducted away from the thermal pad through the copper plane to ambient. If the copper plane is not on the top surface of the circuit board, 8 to 10 vias of 13 mil or smaller in diameter should be used to thermally couple the thermal pad to the bottom plane.

For good thermal conduction, the vias must be plated through and solder filled. The copper plane used to conduct heat away from the thermal pad should be as large as practical.

If the ambient temperature is higher than 25℃,a larger copper plane or forced-air cooling will be required to keep the EUA5312 junction temperature below the thermal shutdown temperature (150℃). In higher ambient temperature, higher airflow rate and/or larger copper area will be required to keep the IC out of thermal shutdown.

Package Information



NOTE

1. Package body sizes exclude mold flash protrusion or gate burrs
2. Tolerance ± 0.1mm unless otherwise specified
3. Coplanarity :0.1mm
4. Controlling dimension is millimeter.
5. Die pad exposure size is according to lead frame design.
6. Standard Solder Map dimension is millimeter.
7. Followed from JEDEC MO-15

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	------	------	1.15	------	------	0.045
A1	0.00	------	0.10	0.000	------	0.004
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	------	0.30	0.007	------	0.012
C	0.09	------	0.20	0.004	------	0.008
D	7.70	7.80	7.90	0.303	0.307	0.311
E	------	6.40	-----	------	0.252	------
E1	4.30	4.40	4.50	0.169	0.173	0.177
e	------	0.65	-----	------	0.026	------
L	0.45	0.60	0.75	0.018	0.024	0.030
y	------	------	0.10	------	------	0.004
θ	0	------	8	0	------	8