

FEATURES

High-Definition Multimedia Interface (HDMI®)

- All mandatory and additional 3D video formats supported
- Extended colorimetry, including sYCC601, Adobe RGB, Adobe YCC 601, and xvYCC extended gamut color
- CEC 1.4-compatible

HDMI receiver

165 MHz maximum transition-minimized differential signaling (TMDS) clock frequency

24-bit output pixel bus

High-bandwidth Digital Content Protection (HDCP) 1.4 support with internal high definition copy protocol (HDCP) keys

HDCP repeater support: up to 127 KSVs supported

Integrated consumer electronics control (CEC) controller

Programmable HDMI equalizer

5 V detect and Hot Plug™ assert for HDMI port

Audio support

S/PDIF (IEC 60958-compatible) digital audio

HDMI audio extraction support

Advanced audio mute feature

I²S, 4 streams for 8 channels

General

Interrupt controller with two interrupt outputs

Standard identification (STDI) circuit

Highly flexible 24-bit pixel output interface

Internal extended display identification data (EDID) RAM

Any-to-any 3 × 3 color space conversion (CSC) matrix

2-layer printed circuit board (PCB) design supported

76-ball, 6 mm × 6 mm, chip-scale package BGA

APPLICATIONS

Portable applications

Pico projectors

Digital video cameras

FUNCTIONAL BLOCK DIAGRAM

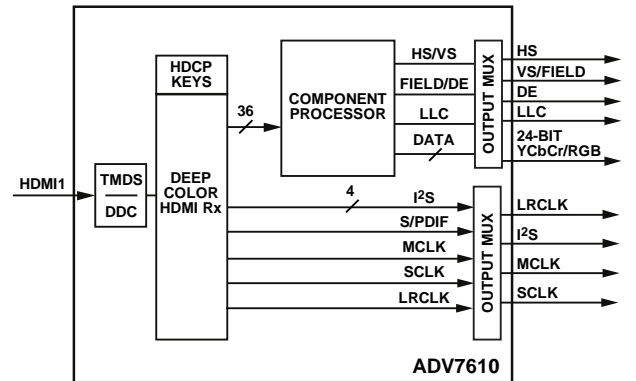


Figure 1.

10775-001

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REVISION HISTORY

12/12—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADV7610 is offered in professional (no HDCP) and industrial versions. The operating temperature range is -40°C to +85°C.

The ADV7610 is a high quality, single input HDMI-capable receiver. It incorporates an HDMI-capable receiver that supports all mandatory 3D TV defined in HDMI specification. The ADV7610 supports formats up to UXGA 60 Hz at eight bits.

It integrates a CEC controller that supports the capability discovery and control (CDC) feature.

The ADV7610 has a 4-channel stereo audio output port for the audio data extracted from the HDMI stream. The HDMI receiver has an advanced mute controller that prevents audible extraneous noise in the audio output.

The following audio formats are accessible:

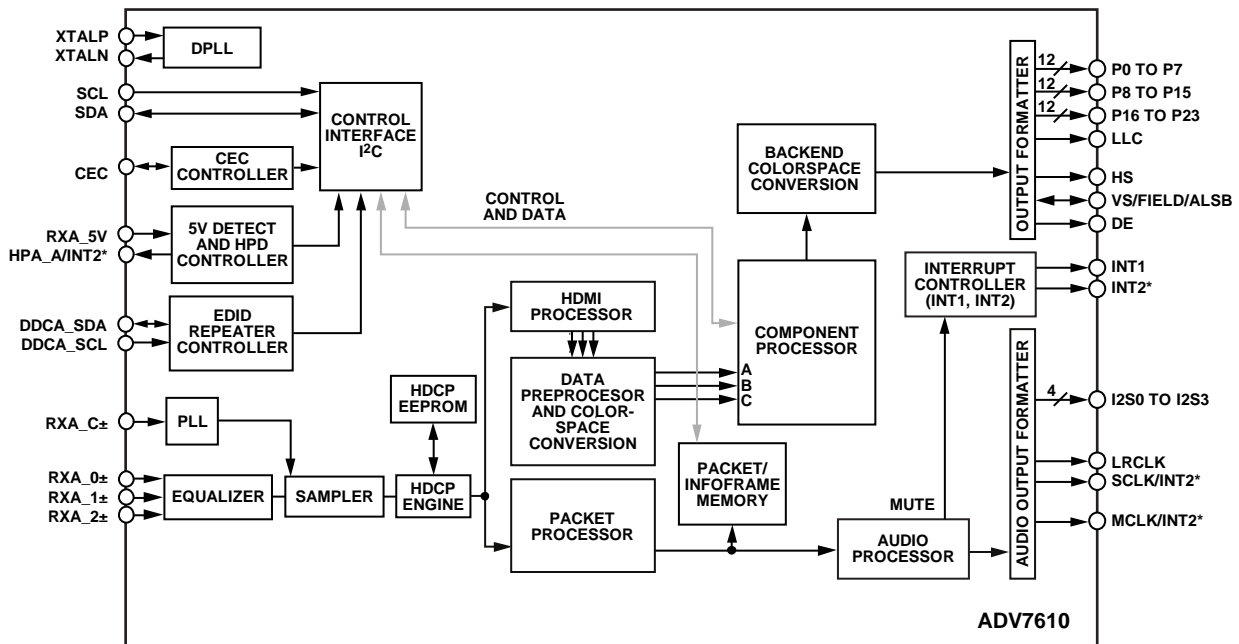
- Four streams from the I²S serializer (eight channels)
- A stream from the S/PDIF serializer (two uncompressed channels or N compressed channels, for example, AC3)
- A DST stream

The HDMI port has dedicated 5 V detect and Hot Plug assert pins. The HDMI receiver also includes an integrated equalizer that ensures the robust operation of the interface with long cables.

The ADV7610 contains one main component processor (CP) that processes the video signals from the HDMI receiver. It provides features such as contrast, brightness, saturation adjustments, STDI detection block, free run, and synchronization alignment controls.

Fabricated in an advanced CMOS process, the ADV7610 is provided in a 6 mm × 6 mm, 76-ball CSP_BGA, RoHS-compliant package and is specified over the -40°C to +85°C temperature range.

DETAILED FUNCTIONAL BLOCK DIAGRAM



*INT2 CAN BE OUTPUT ON ONE OF THE FOLLOWING PINS ONLY: SCLK/INT2, MCLK/INT2, OR HPA_A/INT2.

Figure 2. Detailed Functional Block Diagram

10775-002

SPECIFICATIONS

DVDD = 1.71 V to 1.89 V, DVDDIO = 3.14 V to 3.46 V, PVDD = 1.71 V to 1.89 V, TVDD = 3.14 V to 3.46 V, CVDD = 1.71 V to 1.89 V, T_{MIN} to T_{MAX} = -40°C to +85°C, unless otherwise noted.

ELECTRICAL CHARACTERISTICS

Table 1.

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|------------------------|--------------------------|------|------|-------|------|
| DIGITAL INPUTS¹ | | | | | | |
| Input High Voltage | V _{IH} | XTALN and XTALP | 1.2 | | | V |
| | V _{IH} | Other digital inputs | 2 | | | V |
| Input Low Voltage | V _{IL} | XTALN and XTALP | | | 0.4 | V |
| | V _{IL} | Other digital inputs | | | 0.8 | V |
| Input Current | I _{IN} | RESET pin | | ±45 | ±60 | μA |
| | | Other digital inputs | | ±10 | | μA |
| Input Capacitance | C _{IN} | | | | 10 | pF |
| DIGITAL INPUTS (5 V TOLERANT)^{1, 2} | | | | | | |
| Input High Voltage | V _{IH} | | 2.6 | | | V |
| Input Low Voltage | V _{IL} | | | | 0.8 | V |
| Input Current | I _{IN} | | -82 | | +82 | μA |
| DIGITAL OUTPUTS¹ | | | | | | |
| Output High Voltage | V _{OH} | | 2.4 | | | V |
| Output Low Voltage | V _{OL} | | | | 0.4 | V |
| High Impedance Leakage Current | I _{LEAK} | VS/FIELD/ALSB pin | | ±35 | ±60 | μA |
| | | HPA_A/INT2 pin | | | ±82 | μA |
| Other | | | 10 | | | μA |
| Output Capacitance | C _{OUT} | | | | 20 | pF |
| POWER REQUIREMENTS³ | | | | | | |
| Digital Core Power Supply | DVDD | | 1.71 | 1.8 | 1.89 | V |
| Digital I/O Power Supply | DVDDIO | | 3.14 | 3.3 | 3.46 | V |
| PLL Power Supply | PVDD | | 1.71 | 1.8 | 1.89 | V |
| Terminator Power Supply | TVDD | | 3.14 | 3.3 | 3.46 | V |
| Comparator Power Supply | CVDD | | 1.71 | 1.8 | 1.89 | V |
| Digital Core Supply Current | I _{DVDD} | UXGA 60 Hz at eight bits | | 95.7 | 188.1 | mA |
| Digital I/O Supply Current | I _{DVDDIO} | UXGA 60 Hz at eight bits | | 12.9 | 178.5 | mA |
| PLL Supply Current | I _{PVDD} | UXGA 60 Hz at eight bits | | 30.7 | 36.9 | mA |
| Terminator Supply Current | I _{TVDD} | UXGA 60 Hz at eight bits | | 50.9 | 57.6 | mA |
| Comparator Supply Current | I _{CVDD} | UXGA 60 Hz at eight bits | | 95.8 | 114.4 | mA |
| POWER-DOWN CURRENTS⁴ | | | | | | |
| Digital Core Supply Current | I _{DVDD_PD} | Power-Down Mode 1 | | 0.2 | 0.5 | mA |
| Digital I/O Supply Current | I _{DVDDIO_PD} | Power-Down Mode 1 | | 1.3 | 1.7 | mA |
| PLL Supply Current | I _{PVDD_PD} | Power-Down Mode 1 | | 1.5 | 1.8 | mA |
| Terminator Supply Current | I _{TVDD_PD} | Power-Down Mode 1 | | 0.1 | 0.3 | mA |
| Comparator Supply Current | I _{CVDD_PD} | Power-Down Mode 1 | | 1.3 | 1.7 | mA |
| Power-Up Time | t _{PWRUP} | | | 25 | | ms |

¹ Data guaranteed by characterization.

² The following pins are 5 V tolerant: DDCA_SCL, DDCA_SDA, and RXA_5V.

³ Maximum current consumption values are recorded with maximum rated voltage supply levels, Moire X video pattern, and at maximum rated temperature.

⁴ Power-Down Mode 0 (I/O map, Register 0x0C = 0x62), ring oscillator powered down (HDMI map, Register 0x48 = 0x01), and DDC pads off (HDMI map, Register 0x73 = 0x01).

DATA AND I²C TIMING CHARACTERISTICS

Table 2.

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|--|----------------------------------|--|-------|----------|-------|--------------|
| CLOCK AND CRYSTAL | | | | | | |
| Crystal Frequency, XTALP | | | | 28.63636 | | MHz |
| Crystal Frequency Stability | | | | | ±50 | ppm |
| LLC Frequency Range ¹ | | | 13.5 | | 165 | MHz |
| I ² C PORTS | | | | | | |
| SCL Frequency | | | | | 400 | kHz |
| SCL Minimum Pulse Width High ² | t ₁ | | 600 | | | ns |
| SCL Minimum Pulse Width Low ² | t ₂ | | 1.3 | | | µs |
| Start Condition Hold Time ² | t ₃ | | 600 | | | ns |
| Start Condition Setup Time ² | t ₄ | | 600 | | | ns |
| SDA Setup Time ² | t ₅ | | 100 | | | ns |
| SCL and SDA Rise Time ² | t ₆ | | | | 300 | ns |
| SCL and SDA Fall Time ² | t ₇ | | | | 300 | ns |
| Stop Condition Setup Time ² | t ₈ | | 0.6 | | | µs |
| RESET FEATURE | | | | | | |
| RESET Pulse Width | | | 5 | | | ms |
| CLOCK OUTPUTS | | | | | | |
| LLC Mark:Space Ratio ² | t ₉ :t ₁₀ | | 45:55 | | 55:45 | % duty cycle |
| DATA AND CONTROL OUTPUTS ³ | | | | | | |
| Data Output Transition Time ^{2, 4} | t ₁₁ | End of valid data to negative clock edge | | 1.0 | 2.2 | ns |
| | t ₁₂ | Negative clock edge to start of valid data | | 0.0 | 0.3 | ns |
| I ² S PORT, MASTER MODE | | | | | | |
| SCLK Mark:Space Ratio ² | t ₁₅ :t ₁₆ | | 45:55 | | 55:45 | % duty cycle |
| LRCLK Data Transition Time ² | t ₁₇ | End of valid data to negative SCLK edge | | | 10 | ns |
| LRCLK Data Transition Time ² | t ₁₈ | Negative SCLK edge to start of valid data | | | 10 | ns |
| I ² S Data Transition Time ² | t ₁₉ | End of valid data to negative SCLK edge | | | 5 | ns |
| I ² S Data Transition Time ² | t ₂₀ | Negative SCLK edge to start of valid data | | | 5 | ns |

¹ Maximum LLC frequency is limited by the clock frequency of UXGA 60 Hz at eight bits.

² Data guaranteed by characterization.

³ With the DLL block on the output clock bypassed.

⁴ DLL bypassed on the clock path.

Timing Diagrams

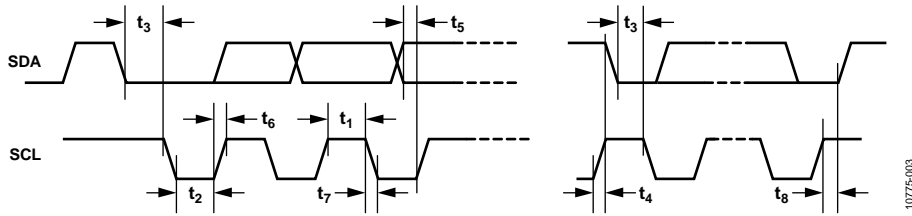


Figure 3. I²C Timing

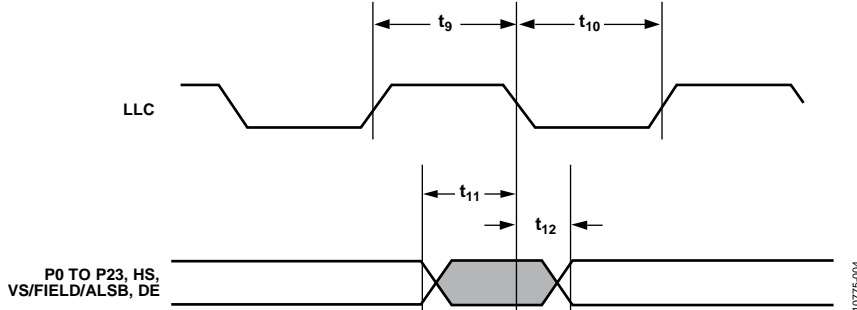


Figure 4. Pixel Port and Control SDR Output Timing

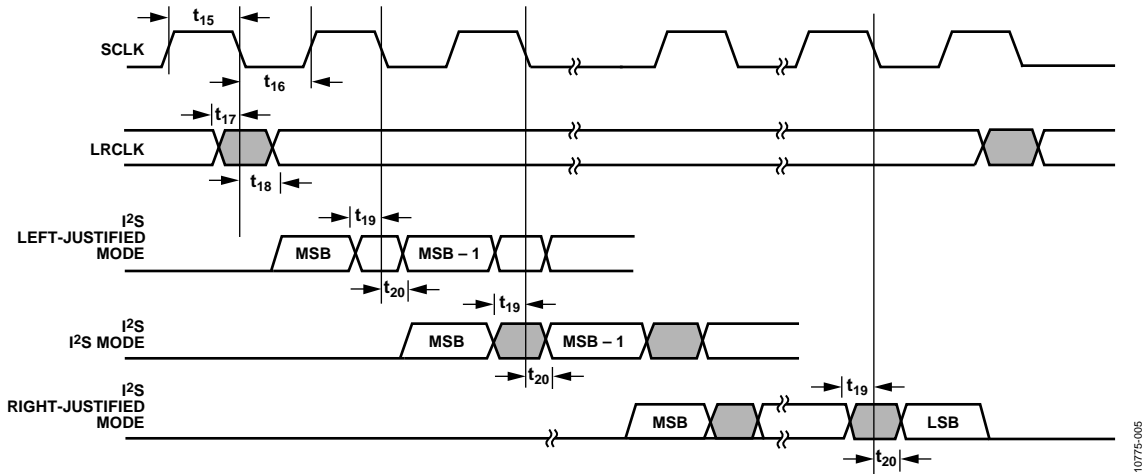


Figure 5. I²S Timing

ABSOLUTE MAXIMUM RATINGS

Table 3.

| Parameter | Rating |
|--|----------------------------------|
| DVDD to GND | 2.2 V |
| PVDD to GND | 2.2 V |
| DVDDIO to GND | 4.0 V |
| CVDD to GND | 2.2 V |
| TVDD to GND | 4.0 V |
| Digital Inputs Voltage to GND | GND – 0.3 V to DVDDIO + 0.3 V |
| 5 V Tolerant Digital Inputs to GND ¹ | 5.3 V |
| Digital Outputs Voltage to GND | GND – 0.3 V to DVDDIO + 0.3 V |
| XTALP, XTALN | GND – 0.3 V to PVDD + 0.3 V |
| SCL/SDA Data Pins to DVDDIO | DVDDIO – 0.3 V to DVDDIO + 3.6 V |
| Maximum Junction Temperature (T _{J MAX}) | 125°C |
| Storage Temperature Range | –60°C to +150°C |
| Infrared Reflow Soldering (20 sec) | 260°C |

¹ The following inputs are 3.3 V inputs but are 5 V tolerant: DDCA_SCL, DDCA_SDA, and RXA_5V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL PERFORMANCE

To reduce power consumption when using the ADV7610, turn off the unused sections of the part.

Due to the PCB metal variation and, therefore, variation in PCB heat conductivity, the value of θ_{JA} may differ for various PCBs.

The most efficient measurement solution is obtained using the package surface temperature to estimate the die temperature because this eliminates the variance associated with the θ_{JA} value.

Do not exceed the maximum junction temperature (T_{J MAX}) of 125°C. The following equation calculates the junction temperature using the measured package surface temperature, and it applies only when a heat sink is not used on the device under test (DUT):

$$T_J = T_S + (\Psi_{JT} \times W_{TOTAL})$$

where:

T_S is the package surface temperature (°C).

$\Psi_{JT} = 0.4^\circ\text{C}/\text{W}$ for the 76-ball CSP_BGA.

$$W_{TOTAL} = ((PVDD \times I_{PVDD}) + (0.05 \times TVDD \times I_{TVDD}) + (CVDD \times I_{CVDD}) + (DVDD \times I_{DVDD}) + (DVDDIO \times I_{DVDDIO}))$$

where 0.05 is 5% of the TVDD power that is dissipated on the device itself.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

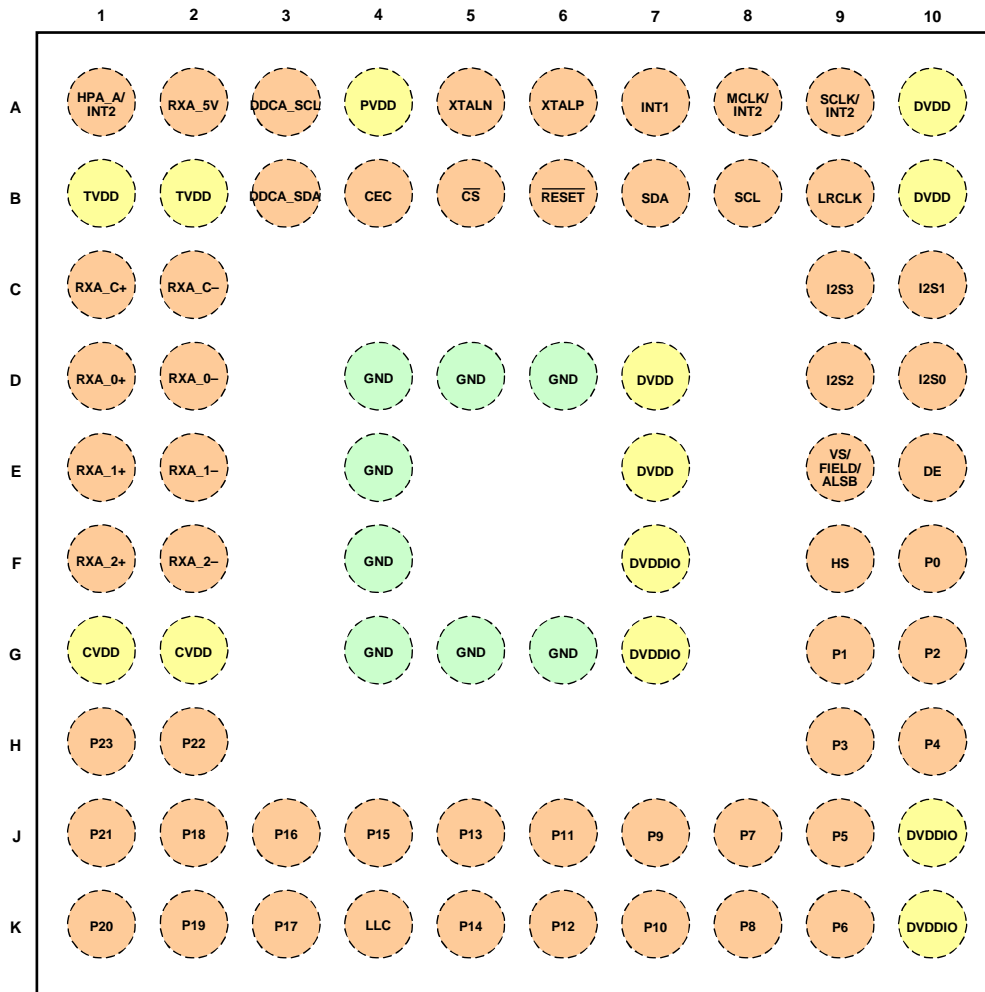


Figure 6. Pin Configuration

Table 4. Pin Function Descriptions

| Ball No. | Mnemonic | Type | Description |
|--------------------------------|------------|-----------------------|---|
| D4, D5, D6, E4, F4, G4, G5, G6 | GND | Ground | Ground. |
| A1 | HPA_A/INT2 | Miscellaneous digital | A dual function pin that can be configured to output a Hot Plug assert signal (for HDMI Port A) or an Interrupt 2 signal. |
| G1, G2 | CVDD | Power | HDMI Analog Block Supply Voltage (1.8 V). |
| B1, B2 | TVDD | Power | Terminator Supply Voltage (3.3 V). |
| F7, G7, J10, K10 | DVDDIO | Power | Digital I/O Supply Voltage (3.3 V). |
| A10, B10, D7, E7 | DVDD | Power | Digital Core Supply Voltage (1.8 V). |
| A4 | PVDD | Power | PLL Supply Voltage (1.8 V). |
| C2 | RXA_C- | HDMI input | Digital Input Clock Complement of Port A in the HDMI Interface. |
| C1 | RXA_C+ | HDMI input | Digital Input Clock True of Port A in the HDMI Interface. |
| D2 | RXA_0- | HDMI input | Digital Input Channel 0 Complement of Port A in the HDMI Interface. |
| D1 | RXA_0+ | HDMI input | Digital Input Channel 0 True of Port A in the HDMI Interface. |
| E2 | RXA_1- | HDMI input | Digital Input Channel 1 Complement of Port A in the HDMI Interface. |
| E1 | RXA_1+ | HDMI input | Digital Input Channel 1 True of Port A in the HDMI Interface. |
| F2 | RXA_2- | HDMI input | Digital Input Channel 2 Complement of Port A in the HDMI Interface. |
| F1 | RXA_2+ | HDMI input | Digital Input Channel 2 True of Port A in the HDMI Interface. |

| Ball No. | Mnemonic | Type | Description |
|------------------|---------------------------|-----------------------|--|
| H1 | P23 | Digital video output | Video Pixel Output Port. |
| H2 | P22 | Digital video output | Video Pixel Output Port. |
| J1 | P21 | Digital video output | Video Pixel Output Port. |
| K1 | P20 | Digital video output | Video Pixel Output Port. |
| K2 | P19 | Digital video output | Video Pixel Output Port. |
| J2 | P18 | Digital video output | Video Pixel Output Port. |
| K3 | P17 | Digital video output | Video Pixel Output Port. |
| J3 | P16 | Digital video output | Video Pixel Output Port. |
| K4 | LLC | Digital video output | Line Locked Output Clock for the Pixel Data the Range is 13.5 MHz to 162.5 MHz. |
| J4 | P15 | Digital video output | Video Pixel Output Port. |
| K5 | P14 | Digital video output | Video Pixel Output Port. |
| J5 | P13 | Digital video output | Video Pixel Output Port. |
| K6 | P12 | Digital video output | Video Pixel Output Port. |
| J6 | P11 | Digital video output | Video Pixel Output Port. |
| K7 | P10 | Digital video output | Video Pixel Output Port. |
| J7 | P9 | Digital video output | Video Pixel Output Port. |
| K8 | P8 | Digital video output | Video Pixel Output Port. |
| J8 | P7 | Digital video output | Video Pixel Output Port. |
| K9 | P6 | Digital video output | Video Pixel Output Port. |
| J9 | P5 | Digital video output | Video Pixel Output Port. |
| H10 | P4 | Digital video output | Video Pixel Output Port. |
| H9 | P3 | Digital video output | Video Pixel Output Port. |
| G10 | P2 | Digital video output | Video Pixel Output Port. |
| G9 | P1 | Digital video output | Video Pixel Output Port. |
| F10 | P0 | Digital video output | Video Pixel Output Port. |
| E10 | DE | Miscellaneous digital | Data Enable. DE is a signal that indicates active pixel data. |
| F9 | HS | Digital video output | Horizontal Synchronization Output Signal. |
| E9 | VS/FIELD/ALSB | Digital input/output | Vertical Synchronization Output Signal. Field Synchronization Output Signal in All Interlaced Video Modes. VS or FIELD can be configured for this pin. The ALSB allows selection of the I ² C address. |
| D10, C10, D9, C9 | I2S0 to I2S3 | Miscellaneous digital | Audio Output Pins. These pins can be configured to output S/PDIF digital audio (S/PDIF) or I ² S. |
| A9 | SCLK/INT2 | Miscellaneous digital | A dual function pin that can be configured to output an audio serial clock or an Interrupt 2 signal. |
| B9 | LRCLK | Miscellaneous digital | Audio Left/Right Clock. |
| A8 | MCLK/INT2 | Miscellaneous digital | A dual function pin that can be configured to output an audio master clock or an Interrupt 2 signal. |
| B8 | SCL | Miscellaneous digital | I ² C Port Serial Clock Input. SCL is the clock line for the control port. |
| B7 | SDA | Miscellaneous digital | I ² C Port Serial Data Input/Output Pin. SDA is the data line for the control port. |
| A7 | INT1 | Miscellaneous digital | Interrupt 1. This pin can be active low or active high. When status bits change, this pin is triggered. The events that trigger an interrupt are under user configuration. |
| B6 | $\overline{\text{RESET}}$ | Miscellaneous digital | System Reset Input. Active low. A minimum low reset pulse width of 5 ms is required to reset the ADV7610 circuitry. |
| A6 | XTALP | Miscellaneous analog | Input Pin for 28.63636 MHz Crystal or an External 1.8 V, 28.63636 MHz Clock Oscillator Source to Clock the ADV7610 . |
| A5 | XTALN | Miscellaneous analog | Crystal Input. Input pin for 28.63636 MHz crystal. |
| B4 | CEC | Digital input/output | Consumer Electronic Control Channel. |
| B5 | $\overline{\text{CS}}$ | Miscellaneous digital | Chip Select (Bar). Pulling this line high causes the I ² C state machine to ignore the I ² C transmission. |
| A3 | DDCA_SCL | HDMI input | HDCP Slave Serial Clock Port A. DDCA_SCL is a 3.3 V input that is 5 V tolerant. |
| B3 | DDCA_SDA | HDMI input | HDCP Slave Serial Data Port A. DDCA_SDA is a 3.3 V input that is 5 V tolerant. |
| A2 | RXA_5V | HDMI input | 5 V Detect Pin for Port A in the HDMI Interface. |

POWER SUPPLY SEQUENCING

POWER-UP SEQUENCE

The recommended power-up sequence of the [ADV7610](#) is to power up the 3.3 V supplies first, followed by the 1.8 V supplies. Hold reset low while the supplies are powered up.

Alternatively, the [ADV7610](#) can be powered up by asserting all supplies simultaneously. In this case, care must be taken while the supplies are being established to ensure that a lower rated supply does not rise above a higher rated supply level.

POWER-DOWN SEQUENCE

The [ADV7610](#) supplies can be deasserted simultaneously as long as a higher rated supply does not fall below a lower rated supply.

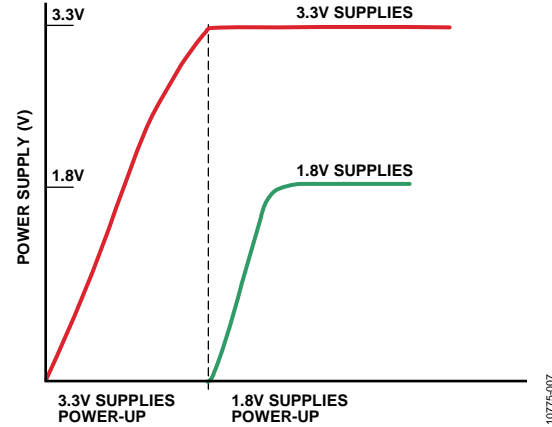


Figure 7. Recommended Power-Up Sequence

FUNCTIONAL OVERVIEW

HDMI RECEIVER

The receiver supports all mandatory and many optional 3D formats. It supports HDTV formats up to UXGA at eight bits.

The HDMI-compatible receiver on the [ADV7610](#) incorporates programmable equalization of the HDMI data signals. This equalization compensates for the high frequency losses inherent in HDMI and DVI cabling, especially at longer lengths and higher frequencies. It is capable of equalizing for cable lengths of up to 30 meters to achieve robust receiver performance.

With the inclusion of HDCP, displays can receive encrypted video content. The HDMI interface of the [ADV7610](#) allows for authentication of a video receiver, decryption of encoded data at the receiver, and renewability of that authentication during transmission, as specified by the HDCP 1.4 protocol.

The [ADV7610](#) has a synchronization regeneration block to regenerate the DE based on the measurement of the video format being displayed and to filter the horizontal and vertical synchronization signals to prevent glitches. The HDMI receiver also supports TERC4 error detection for detection of corrupted HDMI packets following a cable disconnect.

The HDMI receiver contains an audio mute controller that can detect a variety of conditions that may result in audible extraneous noise in the audio output. On detection of these conditions, the audio signal can be ramped to prevent audio clicks or pops. Audio output can be formatted to LPCM and IEC 61937.

The HDMI receiver features include:

- 162.5 MHz (UXGA at eight bits) maximum TMDS clock frequency
- 3D format support defined in the HDMI specification
- Integrated equalizer for cable lengths of up to 30 meters
- HDCP 1.4
- Internal HDCP keys
- PCM audio packet support
- TDM I²S audio packet support
- Repeater support
- Internal EDID RAM
- Hot Plug assert output pin for an HDMI port
- CEC controller

COMPONENT PROCESSOR (CP)

The [ADV7610](#) has an any-to-any 3 × 3 CSC matrix. The CSC block is placed in the output section of the component processor. The CSC enables YPrPb-to-RGB and RGB-to-YCrCb conversions. Many other standards of colorspace can be implemented using the colorspace converter.

CP features include:

- 525i, 625i, 525p, 625p, 720p, 1080i, 1080p, and other formats
- Manual adjustments including gain (contrast) and offset (brightness), hue, and saturation
- Free run output mode that provides stable timing when no video input is present
- 162.5 MHz processing rate
- Contrast, brightness, hue, and saturation controls
- Standard identification enabled by STDI block
- RGB that can be color space converted to YCrCb and decimated to a 4:2:2 format for videocentric back-end IC interfacing
- DE output signal supplied for direct connection to an HDMI/DVI transmitter

OTHER FEATURES

The [ADV7610](#) has HS, VS, FIELD, and DE output signals with programmable position, polarity, and width.

The [ADV7610](#) has programmable interrupt request output pins, including INT1 and INT2 (INT2 is accessible only via one of following pins: MCLK/INT2, SCLK/INT2, or HPA_A/INT2). It also features a low power-down mode. The I²C address of the main map is 0x98 after reset. This can be changed after reset to 0x9A if pull-up is attached to the VS/FIELD/ALSB pin and the I²C command SAMPLE_ALSB is issued.

The [ADV7610](#) is provided in a 6 mm × 6 mm, RoHS-compliant BGA package and is specified over the -40°C to +85°C temperature range.

For more detailed product information about the [ADV7610](#), contact the local Analog Devices, Inc., sales office.

PIXEL INPUT/OUTPUT FORMATTING

The output section of the [ADV7610](#) is highly flexible. The pixel output bus can support up to 24-bit 4:4:4 YCrCb. The pixel data supports both single data rate mode and double data rate mode. In SDR mode, a 16-/24-bit 4:2:2 or 24-bit 4:4:4 output is possible. In DDR mode, the pixel output port can be configured in an 8-/12-bit 4:2:2 YCrCb or 24-bit 4:4:4 RGB.

Bus rotation is supported. Table 5 and Table 6 outline the various output formats that are supported. All output modes are controlled via I²C.

PIXEL DATA OUTPUT MODES FEATURES

The output pixel port features include:

- 8-/12-bit ITU-R BT.656 4:2:2 YCrCb with embedded time codes and/or HS, VS, and FIELD output signals
- 16-/24-bit YCrCb with embedded time codes and/or HS and VS/FIELD pin timing
- 24-bit YCrCb/RGB with embedded time codes and/or HS and VS/FIELD pin timing
- DDR 8-/12-bit 4:2:2 YCrCb
- DDR 24-bit 4:4:4 RGB

Table 5. SDR 4:2:2 and 4:4:4 Output Modes

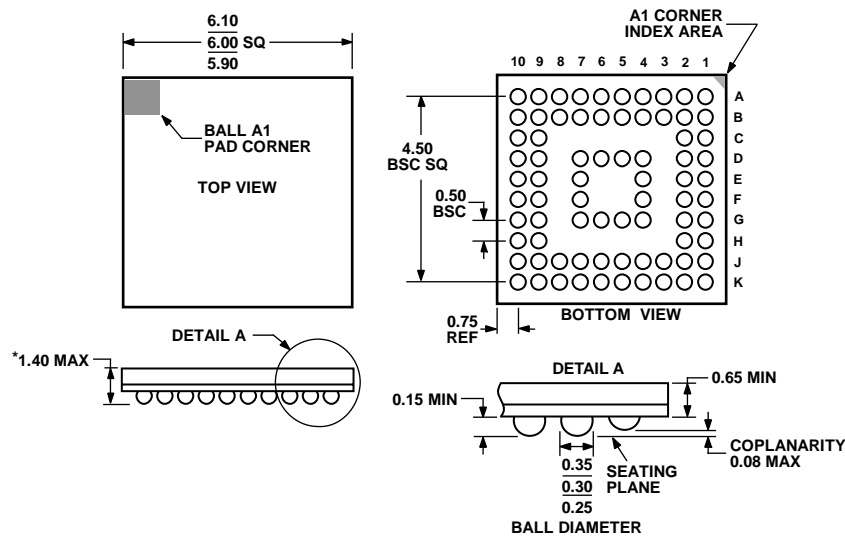
| OP_FORMAT_SEL[7:0] | SDR 4:2:2 | | | | SDR 4:4:4 |
|--------------------|-------------------------------------|--------------------------------------|--|--|----------------------------|
| | 0x0 | 0x0A | 0x80 | 0x8A | 0x40 |
| Pixel Output | 8-Bit SDR ITU-R BT.656 Mode 0 | 12-Bit SDR ITU-R BT.656 Mode 2 | 16-Bit SDR ITU-R BT.656 4:2:2 Mode 0 | 24-Bit SDR ITU-R BT.656 4:2:2 Mode 2 | 24-Bit SDR 4:4:4 Mode 0 |
| P23 | High-Z | Y3, Cb3, Cr3 | High-Z | Y3 | R7 |
| P22 | High-Z | Y2, Cb2, Cr2 | High-Z | Y2 | R6 |
| P21 | High-Z | Y1, Cb1, Cr1 | High-Z | Y1 | R5 |
| P20 | High-Z | Y0, Cb0, Cr0 | High-Z | Y0 | R4 |
| P19 | High-Z | High-Z | High-Z | Cb3, Cr3 | R3 |
| P18 | High-Z | High-Z | High-Z | Cb2, Cr2 | R2 |
| P17 | High-Z | High-Z | High-Z | Cb1, Cr1 | R1 |
| P16 | High-Z | High-Z | High-Z | Cb0, Cr0 | R0 |
| P15 | Y7, Cb7, Cr7 | Y11, Cb11, Cr11 | Y7 | Y11 | G7 |
| P14 | Y6, Cb6, Cr6 | Y10, Cb10, Cr10 | Y6 | Y10 | G6 |
| P13 | Y5, Cb5, Cr5 | Y9, Cb9, Cr9 | Y5 | Y9 | G5 |
| P12 | Y4, Cb4, Cr4 | Y8, Cb8, Cr8 | Y4 | Y8 | G4 |
| P11 | Y3, Cb3, Cr3 | Y7, Cb7, Cr7 | Y3 | Y7 | G3 |
| P10 | Y2, Cb2, Cr2 | Y6, Cb6, Cr6 | Y2 | Y6 | G2 |
| P9 | Y1, Cb1, Cr1 | Y5, Cb5, Cr5 | Y1 | Y5 | G1 |
| P8 | Y0, Cb0, Cr0 | Y4, Cb4, Cr4 | Y0 | Y4 | G0 |
| P7 | High-Z | High-Z | Cb7, Cr7 | Cb11, Cr11 | B7 |
| P6 | High-Z | High-Z | Cb6, Cr6 | Cb10, Cr10 | B6 |
| P5 | High-Z | High-Z | Cb5, Cr5 | Cb9, Cr9 | B5 |
| P4 | High-Z | High-Z | Cb4, Cr4 | Cb8, Cr8 | B4 |
| P3 | High-Z | High-Z | Cb3, Cr3 | Cb7, Cr7 | B3 |
| P2 | High-Z | High-Z | Cb2, Cr2 | Cb6, Cr6 | B2 |
| P1 | High-Z | High-Z | Cb1, Cr1 | Cb5, Cr5 | B1 |
| P0 | High-Z | High-Z | Cb0, Cr0 | Cb4, Cr4 | B0 |

Table 6. DDR 4:2:2 and 4:4:4 Output Modes

| OP_FORMAT_SEL[7:0] | DDR 4:2:2 Mode (Clock/2) | | DDR 4:2:2 Mode (Clock/2) | | DDR 4:4:4 Mode (Clock/2) ^{1,2} | |
|--------------------|--|------------|---|------------|---|------------|
| | 0x20 | | 0x2A | | 0x60 | |
| Pixel Output | 8-Bit DDR ITU-656 (Clock/2 Output) 4:2:2 Mode 0 | | 12-Bit DDR ITU-656 (Clock/2 Output) 4:2:2 Mode 2 | | 24-Bit DDR RGB (Clock/2 Output) | |
| | Clock Rise | Clock Fall | Clock Rise | Clock Fall | Clock Rise | Clock Fall |
| P23 | High-Z | High-Z | Cb3, Cr3 | Y3 | R7-0 | R7-1 |
| P22 | High-Z | High-Z | Cb2, Cr2 | Y2 | R6-0 | R6-1 |
| P21 | High-Z | High-Z | Cb1, Cr1 | Y1 | R5-0 | R5-1 |
| P20 | High-Z | High-Z | Cb0, Cr0 | Y0 | R4-0 | R4-1 |
| P19 | High-Z | High-Z | High-Z | High-Z | R3-0 | R3-1 |
| P18 | High-Z | High-Z | High-Z | High-Z | R2-0 | R2-1 |
| P17 | High-Z | High-Z | High-Z | High-Z | R1-0 | R1-1 |
| P16 | High-Z | High-Z | High-Z | High-Z | R0-0 | R0-1 |
| P15 | Cb7, Cr7 | Y7 | Cb11, Cr11 | Y11 | G7-0 | G7-1 |
| P14 | Cb6, Cr6 | Y6 | Cb12, Cr12 | Y12 | G6-0 | G6-1 |
| P13 | Cb5, Cr5 | Y5 | Cb9, Cr9 | Y9 | G5-0 | G5-1 |
| P12 | Cb4, Cr4 | Y4 | Cb8, Cr8 | Y8 | G4-0 | G4-1 |
| P11 | Cb3, Cr3 | Y3 | Cb7, Cr7 | Y7 | G3-0 | G3-1 |
| P10 | Cb2, Cr2 | Y2 | Cb6, Cr6 | Y6 | G2-0 | G2-1 |
| P9 | Cb1, Cr1 | Y1 | Cb5, Cr5 | Y5 | G1-0 | G1-1 |
| P8 | Cb0, Cr0 | Y0 | Cb4, Cr4 | Y4 | G0-0 | G0-1 |
| P7 | High-Z | High-Z | High-Z | High-Z | B7-0 | B7-1 |
| P6 | High-Z | High-Z | High-Z | High-Z | B6-0 | B6-1 |
| P5 | High-Z | High-Z | High-Z | High-Z | B5-0 | B5-1 |
| P4 | High-Z | High-Z | High-Z | High-Z | B4-0 | B4-1 |
| P3 | High-Z | High-Z | High-Z | High-Z | B3-0 | B3-1 |
| P2 | High-Z | High-Z | High-Z | High-Z | B2-0 | B2-1 |
| P1 | High-Z | High-Z | High-Z | High-Z | B1-0 | B1-1 |
| P0 | High-Z | High-Z | High-Z | High-Z | B0-0 | B0-1 |

¹-0 = even samples.²-1 = odd samples.

OUTLINE DIMENSIONS



*COMPLIANT TO JEDEC STANDARDS MO-225 WITH THE EXCEPTION TO PACKAGE HEIGHT.

Figure 8. 76-Ball Chip Scale Package Ball Grid Array [CSP_BGA] (BC-76-1)

Dimensions shown in millimeters

010807-A

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option |
|--------------------|-------------------|--|----------------|
| ADV7610BBCZ | -40°C to +85°C | 76-Ball Chip Scale Package Ball Grid Array [CSP_BGA] | BC-76-1 |
| ADV7610BBCZ-RL | -40°C to +85°C | 76-Ball Chip Scale Package Ball Grid Array [CSP_BGA], 13" Tape and Reel | BC-76-1 |
| ADV7610BBCZ-P | -40°C to +85°C | 76-Ball Chip Scale Package Ball Grid Array [CSP_BGA], NonHDCP Version | BC-76-1 |
| ADV7610BBCZ-P-RL | -40°C to +85°C | 76-Ball Chip Scale Package Ball Grid Array [CSP_BGA], 13" Tape and Reel, NonHDCP Version | BC-76-1 |

¹ Z = RoHS Compliant Part.

NOTES

NOTES

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