REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																								
SHEET																								
REV																								
SHEET																								
REV STATUS OF SHEETS	REV																							
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18					

PMIC N/A	PREPARED BY Rick C. Offiss	DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444
STANDARDIZED MILITARY DRAWING	CHECKED BY Wm Johnson	MICROCIRCUITS, DIGITAL, CMOS 4K X 4 SRAM WITH SEPARATE I/O MONOLITHIC SILICON
THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	APPROVED BY [signature]	SIZE A / CAGE CODE 67268 / 5962-88611
AMSC N/A	DRAWING APPROVAL DATE 07 DECEMBER 1988	SHEET 1 OF 18
	REVISION LEVEL	

DESC FORM 193
SEP 87

☆ U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-88611	01	K	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	See 6.4	4K X 4 CMOS SRAM with separate I/O	70 ns
02	See 6.4	4K X 4 CMOS SRAM with separate I/O	55 ns
03	See 6.4	4K X 4 CMOS SRAM with separate I/O	45 ns
04	See 6.4	4K X 4 CMOS SRAM with separate I/O	35 ns
05	See 6.4	4K X 4 CMOS SRAM with separate I/O	25 ns

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
K	F-6 (24-lead, .640" x .420" x .090"), flat package
L	D-9 (24-lead, 1.280" x .310" x .200"), dual-in-line package
3	C-4 (28-terminal, .460" x .460" x .100"), square chip carrier package

1.3 Absolute maximum ratings.

Terminal voltage range with respect to ground	-0.5 V dc to +7.0 V dc
DC output current	50 mA
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	1.0 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC}): Cases L, K, and 3	See MIL-M-38510, appendix C
Junction temperature (T_J)	+150°C 1/

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
High level input voltage range (V_{IH})	2.2 V dc to 6.0 V dc
Low level input voltage range (V_{IL})	-0.5 V dc to +0.8 V dc 2/
Case operating temperature range (T_C)	-55°C to +125°C

1/ Maximum junction temperature may be increased to +175°C during burn-in and steady-state life.

2/ Symbol V_{IL}(minimum) = -3.0 V dc for pulse width less than 20 ns.

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.4 Die overcoat. Polyimide and silicon coatings are allowable as an overcoat on the die for alpha particle protection provided that each coated microcircuit inspection lot (see MIL-M-38510) shall be subjected to and pass the internal moisture content test, (method 1018 of MIL-STD-883), the frequency of the internal water vapor testing may not be decreased unless approved by the preparing activity.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, V_{CC} = 4.5 V to 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -4.0 mA, V_{IL} = 0.8 V, V_{IH} = 2.2 V	1, 2, 3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, V_{IL} = 0.8 V, V_{IH} = 2.2 V; I_{OL} = 10 mA	1, 2, 3	All		0.5	V
		I_{OL} = 8.0 mA	1, 2, 3	All		0.4	V
Input leakage current	I_{LI}	V_{CC} = 5.5 V, GND $\le V_{IN} \le V_{CC}$	1, 2, 3	All		5.0	µA
Output leakage current	I_{LO}	V_{CC} = 5.5 V, $\overline{CS}$ = V_{IH}, GND $\le V_{OUT} \le V_{CC}$	1, 2, 3	All		5.0	µA
Operating power current supply	I_{CC1}	V_{CC} = 5.5 V, $\overline{CS}$ = V_{IL}, f = 0 1/, outputs open, $\overline{WE}$, An, and Dn = 2.2 V	1, 2, 3	All		80	mA
Dynamic operating current	I_{CC2}	V_{CC} = 5.5 V, $\overline{CS}$ = 0 V, f = f_{MAX} 1/, $\overline{WE}$ = 3.0 V, Outputs open, An and Dn toggling between 0 V and 3.0 V	1, 2, 3	01, 02, 03		80	mA
				04		90	
				05		100	
Standby power supply current (TTL levels)	I_{SB1}	V_{CC} = 5.5 V, $\overline{CS} \ge$ 3.0 V, f = f_{MAX} 1/, $\overline{WE}$ = 3.0 V, Outputs open, An and Dn toggling between 0 V and 3.0 V	1, 2, 3	01, 02		20	mA
				03, 04		25	
				05		30	
Full standby power supply current (CMOS levels)	ISB2	V_{CC} = 5.5 V, $\overline{CS} \ge$ 5.3 V, f = 0 1/, $V_{IN} \ge$ 5.3 V or $\le$ 0.2 V	1, 2, 3	All		0.3	mA
V_{CC} for data retention	V_{DR}	$\overline{CS} \ge V_{CC}$ -0.2 V; $V_{IN} \ge V_{CC}$ -0.2 V or $\le$ 0.2 V	1, 2, 3	All	2.0		V
Data retention current: at V_{CC} = 2.0 V	I_{CCDR1}		1, 2, 3	All		100	µA
at V_{CC} = 3.0 V	I_{CCDR2}		1, 2, 3	All		150	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, V_{CC} = 4.5 V to 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Input capacitance	C_{IN}	V_{CC} = 5.0 V, V_{IN} = 0 V f = 1.0 MHz, T_A = +25°C See 4.3.1c	4	All		8.0	pF
Output capacitance	C_{OUT}	V_{CC} = 5.0 V, V_{OUT} = 0 V f = 1.0 MHz, T_A = +25°C See 4.3.1c	4	All		8.0	pF
Read cycle time	t_{RC}	See figures 3 and 4 2/	9,10,11	01	70		ns
				02	55		
				03	45		
				04	35		
				05	25		
Address access time	t_{AA}	See figures 3 and 4 2/	9,10,11	01		70	ns
				02		55	
				03		45	
				04		35	
				05		25	
Output hold from address change	t_{OH}	See figures 3 and 4 2/	9,10,11	All	5.0		ns
Chip select access time	t_{ACS}	See figures 3 and 4 2/	9,10,11	01		70	ns
				02		55	
				03		45	
				04		35	
				05		25	
Chip select to output in low Z	t_{LZ}	See figures 3 and 4 3/ 4/	9,10,11	All	5.0		ns

See footnotes at end of table.

☆ U. S. GOVERNMENT PRINTING OFFICE: 1988—550-547

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 4.5 V to 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Chip deselect to output in high Z	t_{HZ}	See figures 3 and 4 3/ 4/	9,10,11	01		30	ns
				02		25	
				03		20	
				04		15	
				05		10	
Chip select to power-up time	t_{PU}	See figures 3 and 4 2/ 3/	9,10,11	All	0		ns
Chip deselect to power-down time	t_{PD}	See figures 3 and 4 2/ 3/	9,10,11	01		60	ns
				02		50	
				03		40	
				04		35	
				05		25	
Read command set-up time	t_{RCS}	See figures 3 and 4 2/	9,10,11	All	-5.0		ns
Read command hold time	t_{RCH}	See figures 3 and 4 2/	9,10,11	All	-5.0		ns
Write cycle time	t_{WC}	See figures 3 and 5 2/	9,10,11	01	60		ns
				02	50		
				03	40		
				04	30		
				05	20		

See footnotes at end of table.

☆ U. S. GOVERNMENT PRINTING OFFICE: 1988—550-547

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C < T_C < +125°C$ V_{CC} = 4.5 V to 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Chip select to end of write	t_{CW}	See figures 3 and 5 2/	9,10,11	01	60		ns
				02	50		
				03	40		
				04	30		
				05	20		
Address valid to end of write	t_{AW}	See figures 3 and 5 2/	9,10,11	01	60		ns
				02	50		
				03	40		
				04	30		
				05	20		
Address set-up time	t_{AS}	See figures 3 and 5 2/	9,10,11	All	0		ns
Write pulse width	t_{WP}	See figures 3 and 5 2/	9,10,11	01	40		ns
				02	35		
				03	30		
				04	25		
				05	20		
Write recovery time	t_{WR}	See figures 3 and 5 2/	9,10,11	All	0		ns
Data valid to end of write	t_{DW}	See figures 3 and 5 2/	9,10,11	01	25		ns
				02,03	20		
				04	17		
				05	13		
Data hold time	t_{DH}	See figures 3 and 5 2/	9,10,11	All	3.0		ns

See footnotes at end of table.

☆ U. S. GOVERNMENT PRINTING OFFICE: 1988—550-547

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 4.5 V to 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Write enable to output valid	t_{WZ}	See figures 3 and 5 3/ 4/	9,10,11	01		30	ns
				02		25	
				03		20	
				04		13	
				05		7.0	
Output active from end of write	t_{OW}	See figures 3 and 5 3/ 4/	9,10,11	All	0		ns
Chip deselect to data retention time	t_{CDR}	$\overline{CS} \ge V_{CC}$ -0.2 V $V_{IN} \ge V_{CC}$ -0.2 V or $\le$ 0.2 V See figure 6 3/	9,10,11	All	0		ns
Operation recovery time	t_R		9,10,11	All	t_{RC}		ns

1/ At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.

2/ Test conditions assume signal transition times of 5.0 ns or less. Timing is referenced at input and output levels of 1.5 V and input pulse levels of 0 to 3.0 V. Output loading is equivalent to the specified I_{OL}/I_{OH} with a load capacitance of 30 pF.

3/ If not tested, shall be guaranteed to the limits specified in table I.

4/ Test conditions assume signal transition times of 5.0 ns or less. Transition is measured at steady-state high level of -200 mV or steady-state low level of +200 mV on the output from 1.5 V level on the input with a load capacitance of 5.0 pF.

Device types	01 thru 05	
Case outlines	K and L	3
Terminal number	Terminal symbol	
1	A_0	A_0
2	A_1	A_1
3	A_2	A_2
4	A_3	A_3
5	A_4	A_4
6	A_5	A_5
7	A_6	NC
8	A_7	NC
9	D_1	A_6
10	D_2	A_7
11	$\overline{CS}$	D_1
12	GND	D_2
13	$\overline{WE}$	$\overline{CS}$
14	Y_1	GND
15	Y_2	$\overline{WE}$
16	Y_3	Y_1
17	Y_4	Y_2
18	D_3	Y_3
19	D_4	Y_4
20	A_8	D_3
21	A_9	NC
22	A_{10}	NC
23	A_{11}	D_4
24	V_{CC}	A_8
25	---	A_9
26	---	A_{10}
27	---	A_{11}
28	---	V_{CC}

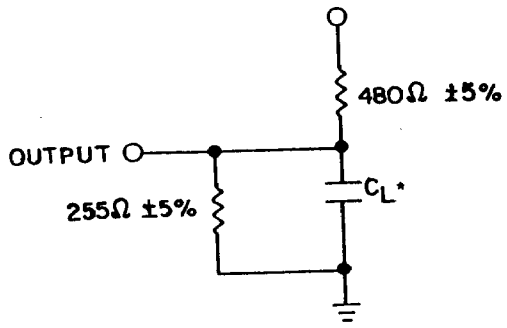
FIGURE 1. Terminal connections.

Device types 01 thru 05

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	High Z	Active

H = Logic 1 state
L = Logic 0 state
X = Don't care
High Z = High impedance state

FIGURE 2. Truth table.

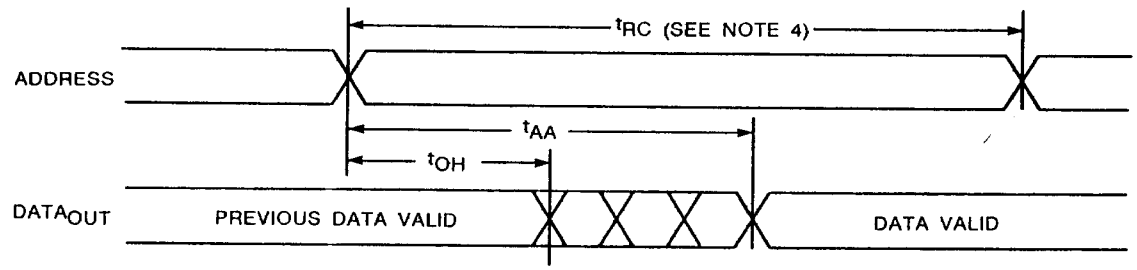


Measurement	*C_L including scope and jig capacitance (Minimum)
t_{HZ}, t_{LZ} t_{WZ}, and t_{OW}	C_L = 5.0 pF
All others	C_L = 30 pF

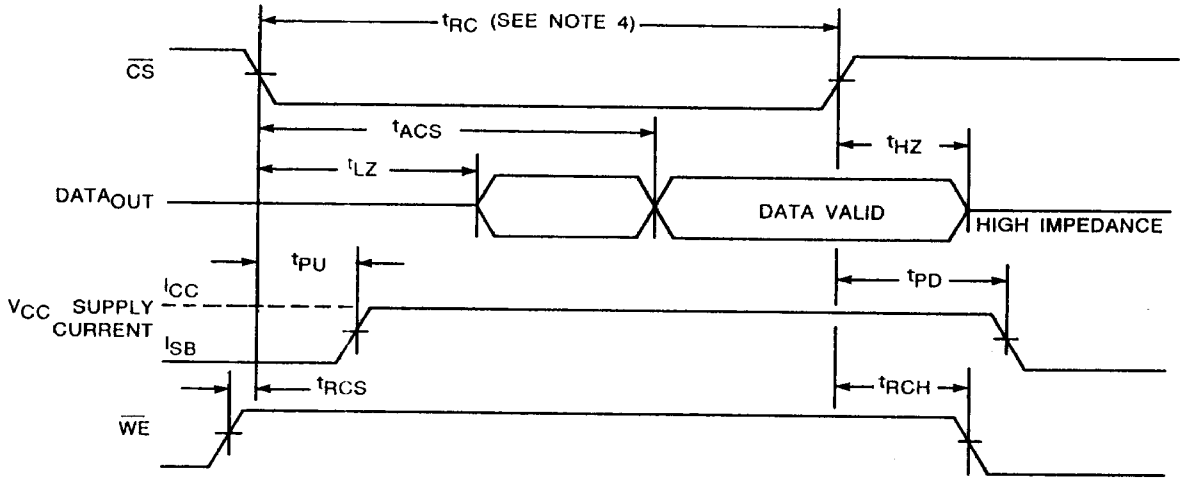
FIGURE 3. Output load circuit.

☆ U.S. GOVERNMENT PRINTING OFFICE: 1987 - 748-129-60913

Read cycle number 1 - $\overline{WE}$ controlled (see notes 1 and 2)



Read cycle number 2 - $\overline{CS}$ controlled (see notes 1 and 3)



NOTES:
1. $\overline{WE}$ is high for read cycle.
2. $\overline{CS}$ is low for read cycle.
3. Address valid prior to or coincident with $\overline{CS}$ low.
4. All read cycle timings are referenced from the last valid address to the first transitioning address.

FIGURE 4. Read cycle timing diagram.

☆U.S. GOVERNMENT PRINTING OFFICE: 1987 - 748-129-60913

Write cycle number 1 - $\overline{WE}$ controlled (see note 1)

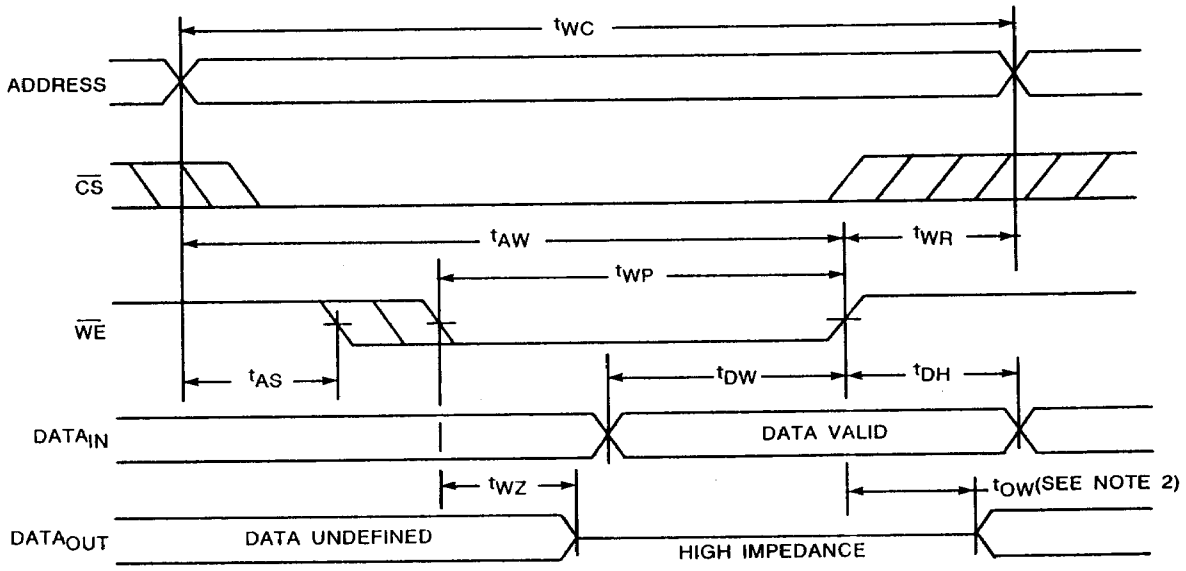
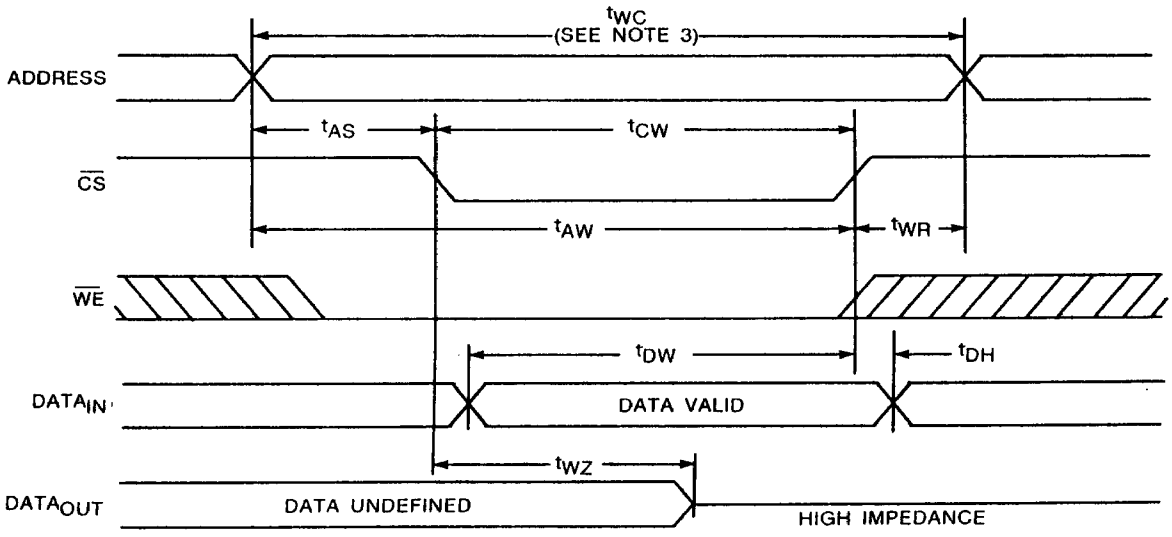


FIGURE 5. Write cycle timing diagram.

Write cycle number 2 - $\overline{CS}$ controlled (see note 1)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the outputs remain in the high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.

FIGURE 5. Write cycle timing diagram - Continued.

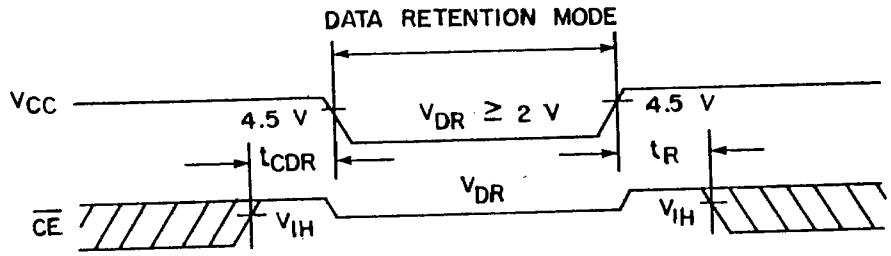


FIGURE 6. Low V_{CC} data retention timing diagram.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial qualification and after process or design changes which may affect capacitance. Sample size is fifteen devices with no failures, and all input and output terminals tested.

d. Subgroups 7 and 8 tests sufficient to verify the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7*,8, 9,10,11
Group A test requirements (method 5005)	1,2,3,4**,7,8, 9,10,11
Groups C and D end-point electrical parameters (method 5005)	2,3,7,8

* PDA applies to subgroups 1 and 7.
** See 4.3.1c.

4.4 Electrostatic discharge sensitivity inspection. Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with method 3015 of MIL-STD-883. The option to categorize as ESD sensitive without performing the test is not allowed. Only those device types that pass ESDS testing at 2000 V or greater shall be considered as conforming to the requirements of this drawing. ESDS testing shall be measured only for initial inspection and after process or design changes which may affect ESDS classification.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8861101LX	61772	IDT71682LA70DB
5962-8861101KX	61772	IDT71682LA70EB
5962-88611013X	61772	IDT71682LA70LB
5962-8861102LX	61772	IDT71682LA55DB
5962-8861102KX	61772	IDT71682LA55EB
5962-88611023X	61772	IDT71682LA55LB
5962-8861103LX	61772	IDT71682LA45DB
5962-8861103KX	61772	IDT71682LA45EB
5962-88611033X	61772	IDT71682LA45LB
5962-8861104LX	61772	IDT71682LA35DB
5962-8861104KX	61772	IDT71682LA35EB
5962-88611043X	61772	IDT71682LA35LB
5962-8861105LX	61772	IDT71682LA25DB
5962-8861105KX	61772	IDT71682LA25EB
5962-88611053X	61772	IDT71682LA25LB

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
61772	Integrated Device Technology, Incorporated 3236 Scott Boulevard Santa Clara, CA 95052

011119