MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC8T26A
(MC6880A)

QUAD THREE-STATE BUS TRANSCEIVER

This quad three-state bus transceiver features both excellent MOS or MPU compatibility, due to its high impedance PNP transistor input, and high-speed operation made possible by the use of Schottky diode clamping. Both the −48 mA driver and −20 mA receiver outputs are short-circuit protected and employ three-state enabling inputs.

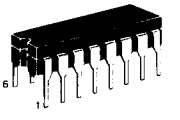
The device is useful as a bus extender in systems employing the M6800 family or other comparable MPU devices. The maximum input current of 200 μA at any of the device input pins assures proper operation despite the limited drive capability of the MPU chip. The inputs are also protected with Schottky-barrier diode clamps to suppress excessive undershoot voltages.

The MC8T26A is identical to the NE8T26A and it operates from a single +5 V supply.

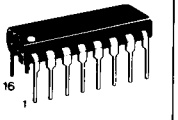
- High Impedance Inputs
- Single Power Supply
- High Speed Schottky Technology
- Three-State Drivers and Receivers
- Compatible with M6800 Family Microprocessor

QUAD THREE-STATE BUS TRANSCEIVER

MONOLITHIC SCHOTTKY INTEGRATED CIRCUITS

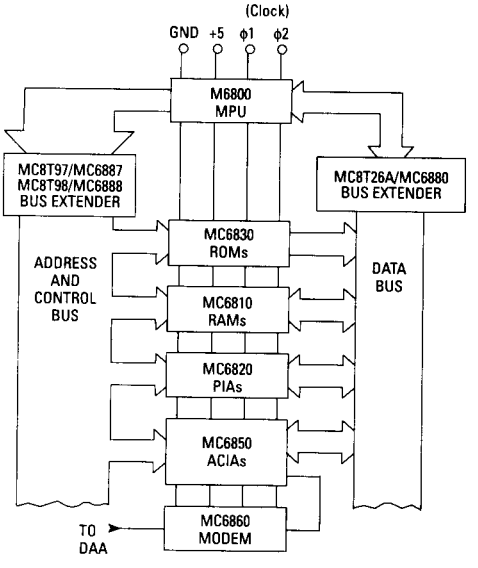


L SUFFIX
CERAMIC PACKAGE
CASE 620

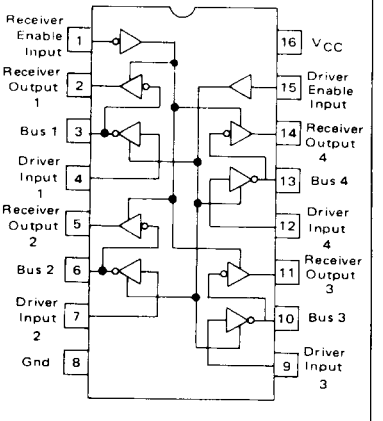


P SUFFIX
PLASTIC PACKAGE
CASE 648

MICROPROCESSOR BUS EXTENDER APPLICATION



PIN CONNECTIONS — MC8T26A (MC6880A)



ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MC8T26AL	MC6880AL	0 to +75°C	Ceramic DIP
MC8T26AP	MC6880AP		Plastic DIP

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Voltage	V_I	5.5	Vdc
Junction Temperature Ceramic Package Plastic Package	T_J	 175 150	°C
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (4.75 V ≤ V_{CC} ≤ 5.25 V and 0°C ≤ T_A ≤ 75°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current — Low Logic State (Receiver Enable Input, $V_{IL(RE)}$ = 0.4 V) (Driver Enable Input, $V_{IL(DE)}$ = 0.4 V) (Driver Input, $V_{IL(D)}$ = 0.4 V) (Bus (Receiver) Input, $V_{IL(B)}$ = 0.4 V)	 $I_{IL(\overline{RE})}$ $I_{IL(DE)}$ $I_{IL(D)}$ $I_{IL(B)}$	 – – – –	 – – – –	 -200 -200 -200 -200	µA
Input Disabled Current — Low Logic State (Driver Input, $V_{IL(D)}$ = 0.4 V)	$I_{IL(D)\ DIS}$	–	–	-25	µA
Input Current-High Logic State (Receiver Enable Input, $V_{IH(RE)}$ = 5.25 V) (Driver Enable Input, $V_{IH(DE)}$ = 5.25 V) (Driver Input, $V_{IH(D)}$ = 5.25 V) (Receiver Input, $V_{IH(B)}$ = 5.25 V)	 $I_{IH(\overline{RE})}$ $I_{IH(DE)}$ $I_{IH(D)}$ $I_{IH(B)}$	 – – – –	 – – – –	 25 25 25 100	µA
Input Voltage — Low Logic State (Receiver Enable Input) (Driver Enable Input (Driver Input) (Receiver Input)	 $V_{IL(\overline{RE})}$ $V_{IL(DE)}$ $V_{IL(D)}$ $V_{IL(B)}$	 – – – –	 – – – –	 0.85 0.85 0.85 0.85	V
Input Voltage — High Logic State (Receiver Enable Input) (Driver Enable Input) (Driver Input) (Receiver Input)	 $V_{IH(\overline{RE})}$ $V_{IH(DE)}$ $V_{IH(D)}$ $V_{IH(B)}$	 2.0 2.0 2.0 2.0	 – – – –	 – – – –	V
Output Voltage — Low Logic State (Bus Driver) Output, $I_{OL(B)}$ = 48 mA) (Receiver Output, $I_{OL(R)}$ = 20 mA)	 $V_{OL(B)}$ $V_{OL(R)}$	 – –	 – –	 0.5 0.5	V
Output Voltage — High Logic State (Bus (Driver) Output, $I_{OH(B)}$ = −10 mA) (Receiver Output, $I_{OH(R)}$ = −2.0 mA) (Receiver Output, $I_{OH(R)}$ = −100 µA, V_{CC} = 5.0 V)	 $V_{OH(B)}$ $V_{OH(R)}$	 2.4 2.4 3.5	 3.1 3.1 –	 – – –	V
Output Disabled Leakage Current — High Logic State (Bus Driver) Output, $V_{OH(B)}$ = 2.4 V) (Receiver Output, $V_{OH(R)}$ = 2.4 V)	 $I_{OHL(B)}$ $I_{OHL(R)}$	 – –	 – –	 100 100	µA
Output Disabled Leakage Current — Low Logic State (Bus Output, $V_{OL(B)}$ = 0.5 V) (Receiver Output, $V_{OL(R)}$ = 0.5 V)	 $I_{OLL(B)}$ $I_{OLL(R)}$	 – –	 – –	 −100 −100	µA
Input Clamp Voltage (Driver Enable Input $I_{ID(DE)}$ = −12 mA) (Receiver Enable Input $I_{IC(RE)}$ = +12 mA) (Driver Input $I_{IC(D)}$ = −12 mA)	 $V_{IC(DE)}$ $V_{IC(RE)}$ $V_{IC(D)}$	 – – –	 – – –	 -1.0 -1.0 -1.0	V
Output Short Circuit Current, V_{CC} = 5.25 V, Note 1 (Bus (Driver) Output) (Receiver Output)	 $I_{OS(B)}$ $I_{OS(R)}$	 -50 -30	 – –	 -150 -75	mA
Power Supply Current (V_{CC} = 5.25 V)	I_{CC}	–	–	87	mA

Note 1. Only one output may be short-circuited at a time.

7

SWITCHING CHARACTERISTICS (Unless otherwise noted, specifications apply at $T_A = 25^oC$ and $V_{CC} = 5.0$ V)

Characteristic	Symbol	Figure	Min	Max	Unit
Propagation Delay Time from Receiver (Bus) Input to High Logic State Receiver Output	$t_{PLH(R)}$	1	–	14	ns
Propagation Delay Time from Receiver (Bus) Input to Low Logic State Receiver Output	$t_{PHL(R)}$	1	–	14	ns
Propagation Delay Time from Driver Input to High Logic State Driver (Bus) Output	$t_{PLH(D)}$	2	–	14	ns
Propagation Delay Time from Driver Input to Low Logic State Driver (Bus) Output	$t_{PHL(D)}$	2	–	14	ns
Propagation Delay Time from $\overline{\text{Receiver Enable}}$ Input to High Impedance (Open) Logic State Receiver Output	$t_{PLZ(RE)}$	3	–	15	ns
Propagation Delay Time from $\overline{\text{Receiver Enable}}$ Input to Low Logic Level Receiver Output	$t_{PZL(RE)}$	3	–	20	ns
Propagation Delay Time from Driver Enable Input to High Impedance Logic State Driver (Bus) Output	$t_{PLZ(DE)}$	4	–	20	ns
Propagation Delay Time from Driver Enable Input to Low Logic State Driver (Bus) Output	$t_{PZL(DE)}$	4	–	25	ns

7

FIGURE 1 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY FROM BUS (RECEIVER) INPUT TO RECEIVER OUTPUT, $t_{PLH(R)}$ AND $t_{PHL(R)}$

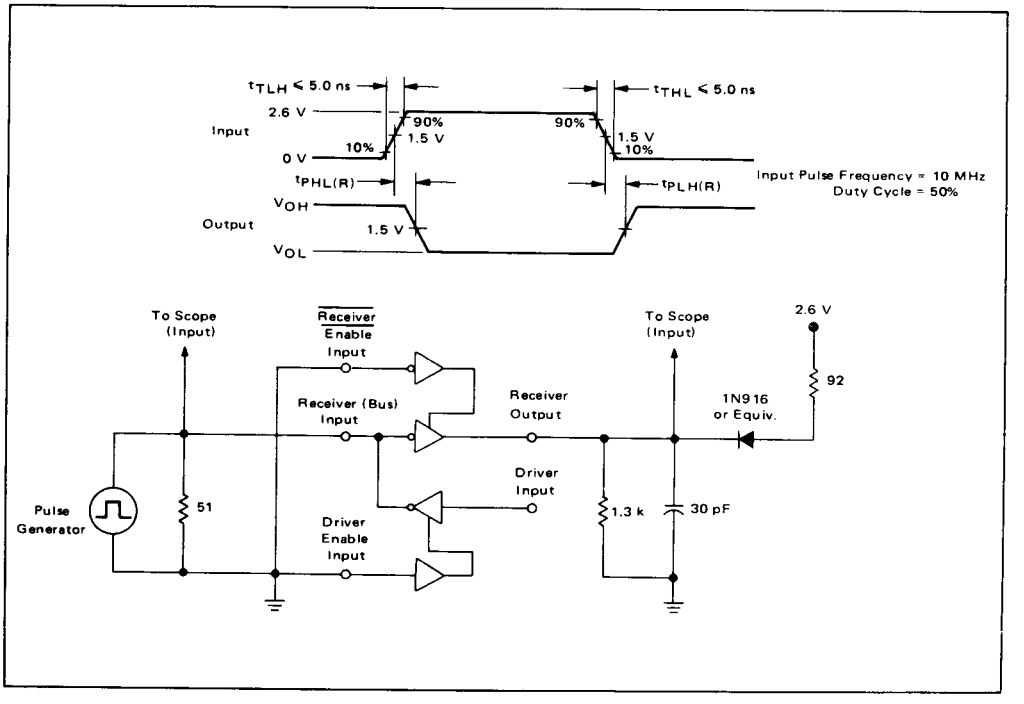


FIGURE 2 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM DRIVER INPUT TO BUS (DRIVER) OUTPUT, $t_{PLH(D)}$ AND $t_{PHL(D)}$

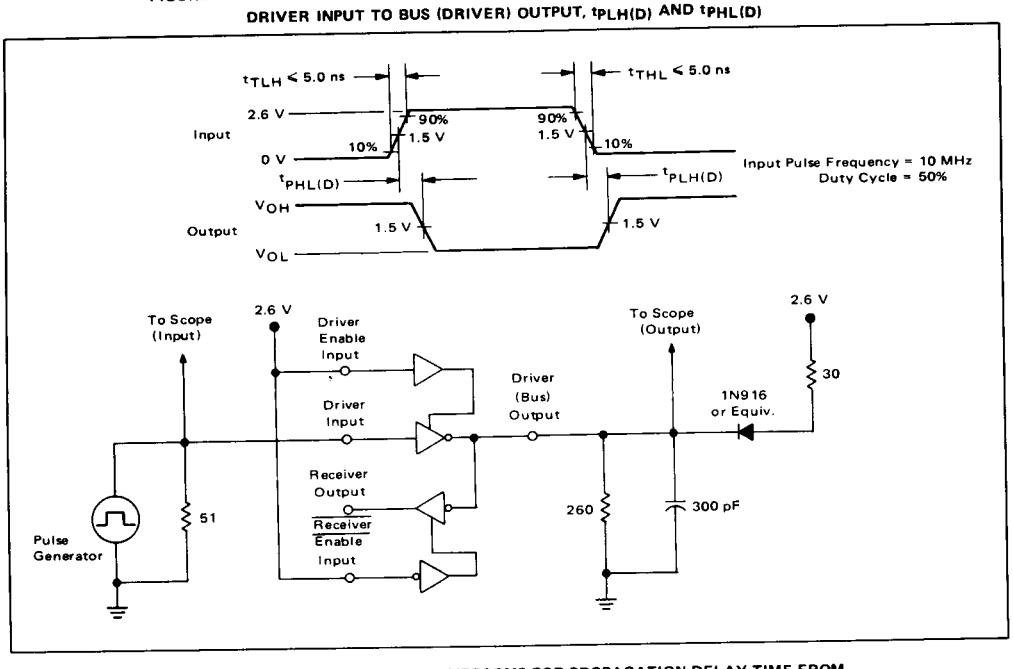


FIGURE 3 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM RECEIVER ENABLE INPUT TO RECEIVER OUTPUT, $t_{PLZ(RE)}$ AND $t_{PZL(RE)}$

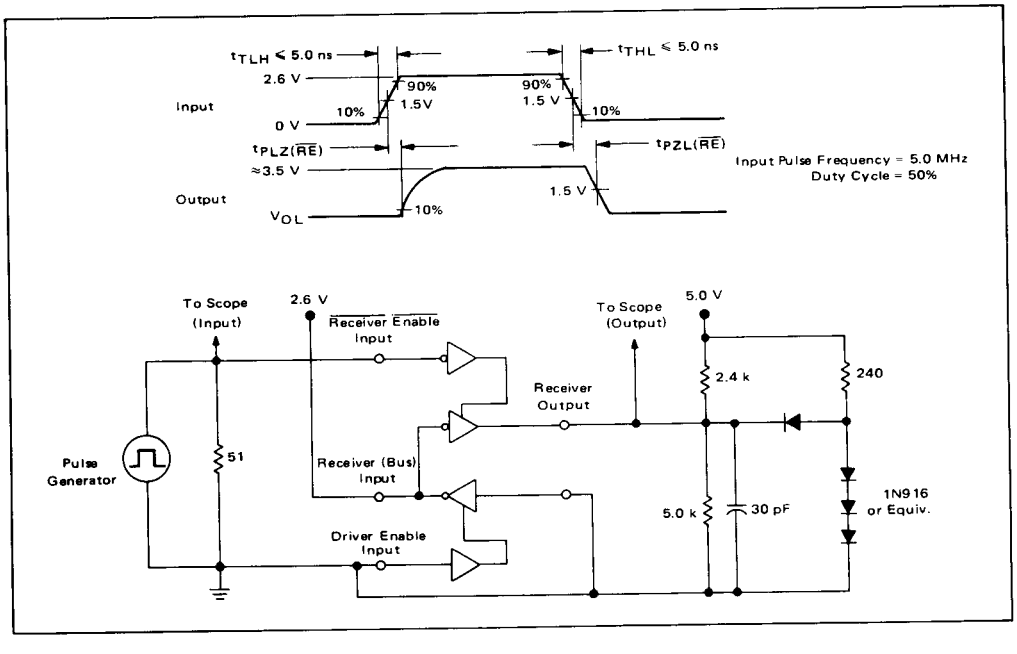


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FIGURE 4 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIMES FROM DRIVER ENABLE INPUT TO DRIVER (BUS) OUTPUT, $t_{PLZ(DE)}$ AND $t_{PZL(DE)}$

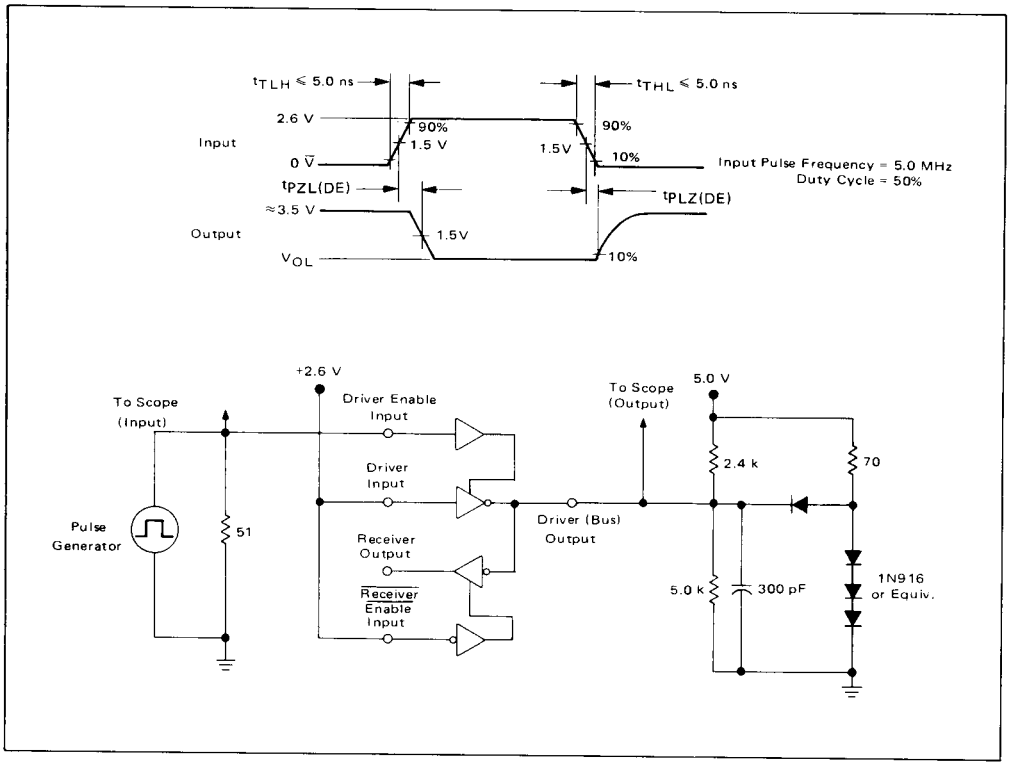

FIGURE 5 – BIDIRECTIONAL BUS APPLICATIONS